

SEMICONDUCTOR PACKAGE AND METHOD OF MANUFACTURING THE SAME

TECHNICAL FIELD

[0001] The inventive concept relates to a semiconductor package and a method of manufacturing the semiconductor package, and more particularly, to a semiconductor package including an interposer and a method of manufacturing the semiconductor package.

BACKGROUND

[0002] In accordance with the rapid development of the electronics industry and user demands, electronic devices have become more compact and multi-functional. Accordingly, the need for miniaturization and multi-functionality of semiconductor chips used in electronic devices is also increasing. For this purpose, semiconductor chips having fine pitch connection terminals are required, and fine-sized electrode pads are required to mount high-capacity semiconductor chips within the limited structure of a semiconductor package. For this reason, a structure and method for electrically connecting a connection terminal to a fine-sized electrode pad included in a semiconductor package are required.

SUMMARY

[0003] The inventive concept provides a semiconductor package with improved electrical characteristics and a method of manufacturing the semiconductor package.

[0004] The technical problems to be solved by the inventive concept are not limited to the problems mentioned above, and other problems not mentioned will be clearly understood by those skilled in the art from the description below.

[0005] According to an aspect of the inventive concept, there is provided a semiconductor package including an interposer, a semiconductor chip disposed on the interposer, an under bump metal (UBM) pad disposed between the interposer and the semiconductor chip and including an upper UBM pad and a lower UBM pad, and a connection member disposed between the UBM pad and the semiconductor chip, wherein the connection member is in contact with side surfaces of the UBM pad and the interposer.

[0006] According to another aspect of the inventive concept, there is provided a method of manufacturing a semiconductor package including forming an interposer, forming a UBM pad on the interposer, forming a plating layer on the UBM pad, and attaching a connection member

onto the UBM pad, wherein the plating layer is in contact with side surfaces of the UBM pad.

[0007] According to another aspect of the inventive concept, there is provided a method of manufacturing a semiconductor package including forming an interposer, forming a UBM pad on the interposer, mounting a semiconductor chip on the UBM pad, and molding the semiconductor chip, wherein the mounting of the semiconductor chip on the UBM pad includes forming a plating layer on the UBM pad, and attaching a connection member onto the UBM pad, the plating layer is in contact with side surfaces of the UBM pad.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] Embodiments will be more clearly understood from the following detailed description taken in conjunction with the accompanying drawings in which:

[0009] FIG. 1 is a cross-sectional view illustrating a semiconductor package according to an embodiment;

[0010] FIG. 2 is an enlarged cross-sectional view of area A of FIG. 1, according to an embodiment;

[0011] FIG. 3 is an enlarged cross-sectional view of area A of FIG. 1, according to an embodiment;

[0012] FIG. 4 is an enlarged cross-sectional view of area A of FIG. 1, according to an embodiment;

[0013] FIG. 5 is an enlarged cross-sectional view of area A of FIG. 1, according to an embodiment;

[0014] FIG. 6 is an enlarged cross-sectional view of area A of FIG. 1, according to an embodiment;

[0015] FIG. 7 is an enlarged cross-sectional view of area A of FIG. 1, according to an embodiment; and

[0016] FIGS. 8, 9, 10, 11, 12, 13, 14 and 15 are cross-sectional views illustrating a method of manufacturing a semiconductor package, according to an embodiment.

DETAILED DESCRIPTION OF THE EMBODIMENTS

[0017] Hereinafter, embodiments of the inventive concept will be described in detail with reference to the attached drawings. The same reference numerals are used for the same components in the drawings, and redundant descriptions thereof are omitted.

[0018] FIG. 1 is a cross-sectional view illustrating a semiconductor package 10 according to an embodiment. FIG. 2 is an enlarged cross-sectional view of area A of FIG. 1 according to an embodiment.

[0019] Referring to FIGS. 1 and 2, the semiconductor package 10 includes an interposer 100, an under bump metal (UBM) structure 140, a connection member 150, an external connection terminal 160, a semiconductor chip 200, and a molding layer 300.

[0020] When the semiconductor chip 200 is miniaturized and/or the number of input/output terminals increases, the semiconductor package 10 has a limitation in accommodating all external connection terminals 160 which are input/output terminals within a main surface of the semiconductor chip 200. Therefore, a Fan-Out Wafer Level Package (FO-WLP) or Fan-Out Panel Level Package (FO-PLP) structure including the external connection terminal 160 is applied to the semiconductor package 10 by extending the interposer 100 to the molding layer 300 that forms an outer circumferential surface of the semiconductor chip 200.

[0021] In addition, the semiconductor package 10 among FO packages may be implemented using a chip-last manufacturing method of firstly forming the interposer 100 on a carrier substrate, and then mounting the semiconductor chip 200 on the formed interposer 100.

[0022] The interposer 100 may electrically connect different semiconductor chips 200 to each other. In the specification, the interposer 100 is shown as a redistribution layer (RDL) interposer, but the interposer 100 may include various types of interposers, such as a silicon interposer and/or an organic interposer. Hereinafter, the case where the interposer 100 is an RDL interposer, that is, the redistribution structure 100, will be described as an example.

[0023] The redistribution structure 100 may be disposed on a lower portion of the semiconductor package 10. The redistribution structure 100 may transmit an electrical signal of the semiconductor chip 200 to the external connection terminal 160. To the contrary, the redistribution structure 100 may transmit the electrical signal received by the external connection terminal 160 to the semiconductor chip 200. Alternatively, the redistribution structure 100 may transmit electrical signals between semiconductor chips 200. The interposer 100 may electrically connect different semiconductor chips 200 to each other.

[0024] The redistribution structure 100 may include a redistribution insulating layer 110, a redistribution line pattern 120, and a redistribution via pattern 130. The redistribution structure 100 may be formed as a single or multiple metal wiring layers. For example, the redistribution structure 100 may include copper (Cu), nickel (Ni), gold (Au), chromium (Cr), titanium (Ti), or palladium (Pd), or an alloy thereof. In some embodiments, the redistribution structure 100 may be formed using an electroplating process.

[0025] The redistribution insulating layer 110 may be formed as a single layer or multiple layers. The redistribution insulating layer 110 may include an insulating material, for example, photo-imageable dielectric (PID) resin, and may further include photosensitive polyimide and/or an inorganic filler. All layers of the redistribution insulating layer 110 may include the same material, or at least one layer thereof may include a different material.

[0026] Although not shown in FIGS. 1 and 2, the semiconductor package 10 may further include a protective layer that protects pads on an upper surface and/or a lower surface of the redistribution structure 100.

[0027] The redistribution line pattern 120 and the redistribution via pattern 130 may transmit electrical signals and/or heat within the redistribution structure 100. The redistribution line pattern 120 may be formed inside the redistribution insulating layer 110 and may extend in a horizontal direction (X direction and/or Y direction). The redistribution via pattern 130 may electrically connect the redistribution line patterns 120 spaced apart in a vertical direction (Z direction) and may extend in the vertical direction (Z direction). The redistribution line pattern 120 and the redistribution via pattern 130 may each include metal such as copper (Cu), aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), indium (In), molybdenum (Mo), manganese (Mn), cobalt (Co), tin (Sn), nickel (Ni), magnesium (Mg), rhenium (Re), beryllium (Be), gallium (Ga), ruthenium (Ru), or an alloy thereof, but are not limited thereto.

[0028] The redistribution line pattern 120 and the redistribution via pattern 130 may be formed using a plating method. For example, the redistribution line pattern 120 and the redistribution via pattern 130 may be formed using a plating method such as immersion plating, electroless plating, or electroplating.

[0029] In some embodiments, a plurality of redistribution via patterns 130 may each have a tapered shape with a horizontal width decreasing and extending from the top to the bottom. That is, the plurality of redistribution via patterns 130 may each have a horizontal width decreasing further away from the semiconductor chip 200 in the vertical direction (Z direction).

[0030] In the specification, a direction parallel to the main surface of the redistribution structure 100 may be referred to as the horizontal direction (X direction and/or Y direction), and a direction perpendicular to the horizontal direction (X direction and/or Y direction) may be referred to as the vertical direction (Z direction).

[0031] The UBM structure 140 may be formed on the redistribution structure 100. The UBM structure 140 may be located in an opening of the redistribution structure 100. The UBM structure 140 may be in contact with the uppermost redistribution line pattern 120 and/or the uppermost redistribution via pattern 130. In FIGS. 1 and 2, the UBM structure 140 is shown as

being in contact with the redistribution line pattern 120, but the UBM structure 140 may be in contact with the redistribution via pattern 130. As will be described below, the UBM structure 140 and the connection member 150 may electrically connect the redistribution line pattern 120 and the redistribution via pattern 130 to the semiconductor chip 200.

[0032] The UBM structure 140 may include an adhesion layer 142, a seed layer 143, a lower UBM pad 144, and an upper UBM pad 146. The lower UBM pad 144 and the upper UBM pad 146 may be collectively referred to as a UBM pad 147.

[0033] The adhesion layer 142 and the seed layer 143 may be disposed between the UBM pad 147 and the redistribution line pattern 120 and/or the redistribution via pattern 130. The seed layer 143 may be disposed on the adhesion layer 142. The adhesion layer 142 and the seed layer 143 may be disposed on a lower portion of the UBM structure 140 and may be formed to conformally extend. Specifically, the adhesion layer 142 may be formed to conformally extend to a part of the upper surface of the redistribution structure 100. In addition, the seed layer 143 may be formed to conformally extend to at least a part of each of a lower surface of the lower UBM pad 144, a side surface of the lower UBM pad 144, and a lower surface of the upper UBM pad 146.

[0034] The adhesion layer 142 may strengthen the adhesion between the redistribution structure 100 and the UBM pad 147. For example, the adhesion layer 142 may include metal including at least one selected from titanium (Ti), titanium tungsten (TiW), nickel vanadium (NiV), and chromium (Cr), or an alloy thereof. The seed layer 143 may act as a seed when forming the UBM pad 147. The seed layer 143 may provide a path through which current may flow when the UBM pad 147 is formed through an electroplating process, and allow the UBM pad 147 to be formed on the seed layer 143. The seed layer 143 may include metal including at least one selected from copper (Cu), aluminum (Al), silver (Ag), tin (Sn), gold (Au), nickel (Ni), lead (Pb), and titanium (Ti) or an alloy thereof.

[0035] In the inventive concept, the seed layer 143 and the UBM pad 147 include different materials so that an interface is present therebetween, but, in another embodiment, when the seed layer 143 and the UBM pad 147 include the same material, the seed layer 143 and the UBM pad 147 may be integrally formed because no interface is present therebetween.

[0036] The UBM pad 147 may include a lower UBM pad 144 disposed adjacent to a lower portion of the UBM structure 140 and an upper UBM pad 146 disposed adjacent to an upper portion of the UBM structure 140. An upper surface of the upper UBM pad 146 may have a flat shape.

[0037] The lower UBM pad 144 may be in contact with the seed layer 143 and the upper UBM pad 146. In more detail, at least a part of each of lower and side surfaces of the lower UBM pad 144 may be in contact with the seed layer 143. In addition, at least a part of the upper surface of the lower UBM pad 144 may be in contact with the upper UBM pad 146.

[0038] The upper UBM pad 146 may be in contact with the lower UBM pad 144 and the connection member 150. In more detail, at least a part of a lower surface of the upper UBM pad 146 may be in contact with the lower UBM pad 144, and at least a part of each of the upper and side surfaces of the upper UBM pad 146 may be in contact with the connection member 150.

[0039] The UBM pad 147 may have a reverse T-shape. That is, a first width W1, which is a horizontal width of the lower UBM pad 144, may be less than a second width W2, which is a horizontal width of the upper UBM pad 146.

[0040] In the specification, the lower UBM pad 144 and the upper UBM pad 146 are merely formal divisions for explanation purpose, and the lower UBM pad 144 and the upper UBM pad 146 may be integrally formed. In another embodiment, the lower UBM pad 144 and upper UBM pad 146 may be formed separately.

[0041] In addition, the connection member 150 may be disposed on the UBM structure 140. The connection member 150 may be a solder bump. The UBM structure 140 and the connection member 150 may electrically connect the redistribution line pattern 120 and the redistribution via pattern 130 to the semiconductor chip 200.

[0042] The connection member 150 may be in contact with each of the redistribution structure 100, the UBM structure 140, and a chip pad 240 of the semiconductor chip 200. In more detail, the connection member 150 may be in contact with at least a part of each of an upper surface of the uppermost redistribution insulating layer 110, a side surface of the adhesion layer 142, a side surface of the seed layer 143, and a side surface of the UBM pad 147. The reason why the connection member 150 has such a shape will be explained in more detail with reference to FIGS. 8 to 15 illustrating a method of manufacturing the semiconductor package 10.

[0043] The connection member 150 is formed in contact with at least a part of the side surface of the UBM structure 140, and thus, electrical connectivity between the connection member 150 and the UBM structure 140 may be increased. Accordingly, a contact area between the UBM structure 140 and the connection member 150 increases and wetting is enhanced, and thus, the semiconductor package 10 may implement a fine bump and/or fine pad pitch.

[0044] A plurality of external connection terminals 160 may be disposed on the lower surface of the redistribution structure 100. The external connection terminal 160 may transmit an

electrical signal of the semiconductor chip 200 to the outside of the semiconductor package 10. To the contrary, the external connection terminal 160 may transmit the electrical signal of the outside of the semiconductor package 10 to the semiconductor chip 200. Through the external connection terminal 160, the semiconductor package 10 may be electrically connected to a main board (e.g., a printed circuit board (PCB)) of an electronic device on which the semiconductor package 10 is mounted. The external connection terminal 160 may include a solder bump and/or a solder ball. The redistribution structure 100 may be electrically connected to the external connection terminal 160 through the lowermost redistribution line pattern 120.

[0045] Although not shown in FIG. 1, a pad in direct contact with the external connection terminal 160 may also have a shape similar to that of the UBM structure 140.

[0046] The semiconductor chip 200 may be disposed on the connection member 150. The semiconductor chip 200 may include a semiconductor substrate 220 and a chip pad 240. The semiconductor chip 200 may be a logic chip or a memory chip. The logic chip may be, for example, a microprocessor, analog device, or digital signal processor. In addition, the memory chip may be a volatile memory chip such as Dynamic Random Access Memory (DRAM) or Static Random Access Memory (SRAM), or may be a non-volatile memory chip such as Phase-change Random Access Memory (PRAM), Magnetoresistive Random Access Memory (MRAM), Resistive Random Access Memory (RRAM), or Ferroelectric Random Access Memory (FeRAM). In some embodiments, the semiconductor chip 200 may be a high bandwidth memory chip. The semiconductor package 10 may include a plurality of semiconductor chips 200.

[0047] The semiconductor chip 200 may be understood as a concept including a semiconductor device including an integrated circuit. Specifically, the semiconductor chip 200 may include the semiconductor substrate 220 including an active surface and an inactive surface which face each other. A circuit unit implementing an integrated circuit function of the semiconductor chip 200 may be formed on the active surface of the semiconductor substrate 220 through a semiconductor manufacturing process. That is, on the semiconductor substrate 220, wiring layers such as a conductive wiring, interlayer insulating layers disposed between the wiring layers, and individual unit devices may be formed.

[0048] In addition, the semiconductor chip 200 may include the chip pad 240 formed on the semiconductor substrate 220 and expanding the function of the circuit unit to the outside. The chip pad 240 may have a peripheral portion covered by and a central portion opened by the protective layer formed on the active surface of the semiconductor substrate 220. The protective layer may physically and chemically protect the semiconductor device on the active

side of the semiconductor substrate 220. The protective layer may include, for example, an inorganic insulating material such as silicon oxide, silicon nitride, or silicon oxynitride, an organic insulating material such as an insulating polymer, or an insulating material including a combination thereof.

[0049] For example, the chip pad 240 may have a polygonal shape such as a square, hexagon, or octagon, or a circular or oval shape. The chip pad 240 may have a certain size or more to withstand electrical and mechanical stress. The connection member 150 may be disposed on a lower portion of the chip pad 240.

[0050] In the specification, a lower surface of a component of the semiconductor package 10, excluding the external connection terminal 160, may be defined as a surface adjacent to the external connection terminal 160 among two surfaces of the component spaced apart in the vertical direction (Z direction), and a surface opposite to an upper surface of the component may be defined as the lower surface of the component. In addition, a surface in contact between the redistribution structure 100 and the external connection terminal 160 may be defined as the upper surface of the external connection terminal 160, and a surface opposite to the upper surface of the external connection terminal 160 may be defined as the lower surface of the external connection terminal 160.

[0051] The molding layer 300 covering at least a part of each of the UBM structure 140, the connection member 150, and the semiconductor chip 200 may be formed on the redistribution structure 100. The molding layer 300 may protect the semiconductor chip 200 from external influences such as contamination and/or shock. For example, the molding layer 300 may include epoxy mold compound, resin, etc. In addition, the molding layer 300 may be formed by processes such as compression molding, lamination, and screen printing. In some embodiments, the molding layer 300 may cover only the side surface of the semiconductor chip 200 so that the upper surface of the semiconductor chip 200 is exposed to the outside. The molding layer 300 may configure the appearance of the semiconductor package 10, and the redistribution structure 100 may be expanded and disposed by using the molding layer 300.

[0052] In a general semiconductor package, a connection member only is in contact with an upper surface of a UBM structure and does not contact side surfaces thereof. Therefore, the electrical connectivity between the UBM structure and the connection member is relatively low, causing a problem in which the electrical reliability of a semiconductor package is relatively low.

[0053] On the other hand, in the semiconductor package 10 of the inventive concept, the connection member 150 is in contact with at least a part of each of the upper and side surfaces

of the UBM structure 140, and thus, the electrical connectivity between the UBM structure 140 and the connection member 150 may be relatively high. Accordingly, the wetting of the connection member 150 is improved, and thus, the electrical reliability of the semiconductor package 10 may be relatively high.

[0054] FIGS. 3 and 4 are enlarged cross-sectional views of area A of FIG. 1 according to an embodiment. The embodiment of FIGS. 3 and 4 is described with reference to FIGS. 1 and 2 together.

[0055] Referring to FIGS. 3 and 4, a UBM structure 140a of FIG. 3 may include the adhesion layer 142, the seed layer 143, the lower UBM pad 144, the upper UBM pad 146, and a first additional plating layer 148. In addition, a UBM structure 140b of FIG. 4 may include the adhesion layer 142, the seed layer 143, the lower UBM pad 144, the upper UBM pad 146, the first additional plating layer 148, and a second additional plating layer 149. The adhesion layer 142, the seed layer 143, the lower UBM pad 144, and the upper UBM pad 146 of FIGS. 3 and 4 are substantially the same as the adhesion layer 142, the seed layer 143, the lower UBM pad 144, and the upper UBM pad 146 of the UBM structure 140 of FIGS. 1 and 2, respectively, and thus, herein, the first additional plating layer 148 and the second additional plating layer 149 are mainly described.

[0056] The first additional plating layer 148 and/or the second additional plating layer 149 may function as a barrier layer. The first additional plating layer 148 and/or the second additional plating layer 149 may be disposed between the UBM pad 147 and the connection member 150. The first additional plating layer 148 and/or the second additional plating layer 149 may be disposed between the upper UBM pad 146 and the connection member 150. The first additional plating layer 148 and the second additional plating layer 149 may be sequentially stacked on the upper UBM pad 146.

[0057] The first additional plating layer 148 and the second additional plating layer 149 may each include a conductive material such as copper (Cu), aluminum (Al), silver (Ag), tin (Sn), gold (Au), nickel (Ni), lead (Pb), titanium (Ti), or an alloy thereof. The first additional plating layer 148 and the second additional plating layer 149 may include different materials. In another embodiment, the first additional plating layer 148 and the second additional plating layer 149 may include the same material.

[0058] The first additional plating layer 148 and/or the second additional plating layer 149 are disposed between the UBM pad 147 and the connection member 150, and thus, the connection member 150 may be in contact with side surfaces of the UBM pad 147 and spaced apart from an upper surface of the UBM pad 147. That is, the UBM pad 147 may be in contact with an

upper surface of the first additional plating layer 148 and/or an upper surface of the second additional plating layer 149.

[0059] In FIGS. 3 and 4, one and two plating layers are shown to be disposed between the UBM pad 147 and the connection member 150, respectively, but the inventive concept is not limited thereto. For example, three or more plating layers may be disposed between the UBM pad 147 and the connection member 150.

[0060] FIGS. 5 and 6 are enlarged cross-sectional views of area A of FIG. 1 according to an embodiment. The embodiment of FIGS. 5 and 6 is described with reference to FIGS. 1 and 2 together.

[0061] Referring to FIGS. 5 and 6, a UBM structure 140c of FIG. 5 may include the adhesion layer 142, the seed layer 143, the lower UBM pad 144, and an upper UBM pad 146a. In addition, a UBM structure 140d of FIG. 6 may include the adhesion layer 142, the seed layer 143, the lower UBM pad 144, and an upper UBM pad 146b. The adhesion layer 142, the seed layer 143, and the lower UBM pad 144 of FIGS. 5 and 6 are substantially the same as the adhesion layer 142, the seed layer 143, and the lower UBM pad 144 of the semiconductor package 10 of FIGS. 1 and 2, respectively, and thus, herein, the upper UBM pads 146a and 146b are mainly described.

[0062] An upper surface of the upper UBM pad 146a of FIG. 5 may have an upwardly convex shape, and an upper surface of the upper UBM pad 146b of FIG. 6 may have a downwardly convex shape. That is, the upper surface of the upper UBM pad 146a of FIG. 5 may include a convexly rounded curved surface 146aR, and the upper surface of the upper UBM pad 146b of FIG. 6 may include a concavely rounded curved surface 146bR. This may be a feature resulting from a process of forming each of the upper UBM pads 146a and 146b.

[0063] The shapes of the upper UBM pads 146a and 146b are not limited thereto and may be modified in various ways. For example, the upper surfaces of the upper UBM pads 146a and 146b may each have a concave-convex shape. That is, at least a part of the upper surfaces of the upper UBM pads 146a and 146b may not be a flat shape.

[0064] FIG. 7 is an enlarged cross-sectional view of area A of FIG. 1 according to an embodiment. The embodiment of FIG. 7 is described with reference to FIGS. 1 and 2 together.

[0065] Referring to FIG. 7, a UBM structure 140e may include an adhesion layer 142a, a seed layer 143a, the lower UBM pad 144, and an upper UBM pad 146c. The first width W1, which is the horizontal width of the lower UBM pad 144, may be greater than a second width W2a, which is a horizontal width of the upper UBM pad 146c. In another embodiment, the first width

W1, which is the horizontal width of the lower UBM pad 144, may be equal to the second width W2a, which is the horizontal width of the upper UBM pad 146c.

[0066] When the first width W1 is equal to the second width W2a and/or the first width W1 is greater than the second width W2a, the adhesion layer 142a and the seed layer 143a may be spaced apart from the upper UBM pad 146c. That is, the adhesion layer 142a may not be in contact with the upper UBM pad 146c. The adhesion layer 142a may be in contact with at least a part of each of lower and side surfaces of the lower UBM pad 144. In addition, the connection member 150 may be in contact with the redistribution structure 100, the UBM structure 140e, and the molding layer 300. In more detail, the connection member 150 may be in contact with the redistribution insulating layer 110, the adhesion layer 142a, the lower UBM pad 144, and/or the upper UBM pad 146c.

[0067] FIGS. 8 to 15 are cross-sectional views illustrating a method of manufacturing a semiconductor package according to an embodiment. The method of FIGS. 8 to 15 is described with reference to FIGS. 1 to 7.

[0068] Referring to FIG. 8, the redistribution structure 100 including the redistribution insulating layer 110, the redistribution line pattern 120, and the redistribution via pattern 130 may be formed on a first carrier substrate CS1.

[0069] The first carrier substrate CS1 may support the redistribution structure 100 and may include a material having stability with respect to a semiconductor process. For example, the first carrier substrate CS1 may include glass or aluminum oxide. In order for the first carrier substrate CS1 to stably support the redistribution structure 100, a first adhesion film (not shown) may be disposed between the first carrier substrate CS1 and the redistribution structure 100.

[0070] The redistribution line pattern 120 and the redistribution via pattern 130 may be formed by forming the redistribution insulating layer 110 including a photosensitive insulating material on the first carrier substrate CS1, and performing an exposure process and a development process on the photosensitive insulating material. After at least a part of the redistribution insulating layer 110 may be removed through an etching process, the redistribution line pattern 120 and the redistribution via pattern 130 may be formed through a plating process. The redistribution line pattern 120 may extend in the horizontal direction (X direction and/or Y direction) inside the redistribution insulating layer 110, and the redistribution via pattern 130 may extend in the vertical direction (Z direction) inside the redistribution insulating layer 110. The redistribution line pattern 120 and the redistribution via pattern 130 may be formed by stacking metal and/or metal alloy on a seed layer.

[0071] For example, the redistribution insulating layer 110 may include an insulating material, such as PID resin, and may further include photosensitive polyimide and/or inorganic filler, but is not limited thereto. The redistribution line pattern 120 and the redistribution via pattern 130 may each include metal such as copper (Cu), aluminum (Al), tungsten (W), titanium (Ti), tantalum (Ta), indium (In), molybdenum (Mo), manganese (Mn), cobalt (Co), tin (Sn), nickel (Ni), magnesium (Mg), rhenium (Re), beryllium (Be), gallium (Ga), ruthenium (Ru), or an alloy thereof, but are not limited thereto.

[0072] By repeating this process multiple times, the redistribution structure 100 may be formed. Thereafter, a plurality of first openings OP1 may be formed by removing at least a part of the upper portion of the redistribution structure 100. Each of the plurality of first openings OP1 may expose at least a part of an upper surface of the uppermost redistribution line pattern 120 and/or the uppermost redistribution via pattern 130 to the outside. In FIG. 8, a part of the upper surface of the redistribution line pattern 120 is shown as being exposed by the first opening OP1, but a part of the upper surface of the redistribution via pattern 130 may be exposed by the first opening OP1.

[0073] In addition, in FIG. 8, the upper surface of the redistribution line pattern 120 is shown to be exposed by removing at least a part of an upper portion of the redistribution insulating layer 110, but the upper surface of the redistribution line pattern 120 may be exposed by adding a protective layer (not shown) on the redistribution insulating layer 110 and then, removing at least a part of the protective layer. In this case, the protective layer may include an inorganic insulating material, an organic insulating material, or an insulating material including a combination thereof.

[0074] Referring to FIG. 9, a preliminary adhesion layer 142p and a preliminary seed layer 143p are formed on a resultant of FIG. 8. The preliminary adhesion layer 142p and the preliminary seed layer 143p may be conformally formed on the resultant of FIG. 8. At least a part of each of the preliminary adhesion layer 142p and the preliminary seed layer 143p may be disposed inside the first opening OP1 of FIG. 8. The preliminary adhesion layer 142p may include metal including at least one selected from titanium (Ti), titanium tungsten (TiW), nickel vanadium (NiV), and chromium (Cr), or an alloy thereof. The preliminary seed layer 143p may include metal including at least one selected from copper (Cu), aluminum (Al), silver (Ag), tin (Sn), gold (Au), nickel (Ni), lead (Pb), and titanium (Ti) or an alloy thereof.

[0075] The preliminary adhesion layer 142p may increase an adhesion force between the redistribution structure 100 and the UBM pad 147. The preliminary seed layer 143p may be a seed for forming the lower UBM pad 144 and the upper UBM pad 146. For example, when the

lower UBM pad 144 and the upper UBM pad 146 are formed through an electroplating process, the preliminary seed layer 143p may provide a path through which current may flow so that the lower UBM pad 144 and the upper UBM pad 146 may be formed on an upper portion of the preliminary seed layer 143p.

[0076] The preliminary adhesion layer 142p and the preliminary seed layer 143p may be disposed inside the first opening OP1 of FIG. 8 to form a second opening OP2. In a subsequent process, the lower UBM pad 144 may be formed in the second opening OP2.

[0077] Referring to FIG. 10, a mask pattern MP is formed on the preliminary seed layer 143p. The mask pattern MP may expose at least a part of the preliminary seed layer 143p. The part of the preliminary seed layer 143p exposed by the mask pattern MP may correspond to a part where the UBM pad 147 is formed in the subsequent process. As the mask pattern MP is formed, a third opening OP3 may be formed. In a subsequent process, the UBM pad 147 may be formed inside the second opening OP3.

[0078] Referring to FIG. 11, the UBM pad 147 may be formed inside the third opening OP3 of FIG. 10. The UBM pad 147 may be formed on the preliminary seed layer 143p. The UBM pad 147 may include the lower UBM pad 144 and the upper UBM pad 146. The UBM pad 147 may have a reverse-T shape in which a horizontal width of the upper UBM pad 146 is greater than a horizontal width of the lower UBM pad 144.

[0079] To form the UBM pad 147, electroplating may be performed. For example, the UBM pad 147 may include a conductive material such as copper (Cu), aluminum (Al), silver (Ag), tin (Sn), gold (Au), nickel (Ni), lead (Pb), titanium (Ti), or an alloy thereof. The UBM pad 147 may be formed to partially fill an area defined by the mask pattern MP without completely filling the area. That is, a height of the UBM pad 147 may be formed to be lower than a height of the mask pattern MP.

[0080] Referring to FIG. 12, the mask pattern MP of FIG. 11 may be removed by performing ashing and stripping processes. In addition, the adhesion layer 122 and the seed layer 123 may be formed by removing at least a part of each of the preliminary adhesion layer 122p of FIG. 11 and the preliminary seed layer 123p of FIG. 11 by dry etching and/or wet etching. Side surfaces of the upper UBM pad 146 may be aligned in the vertical direction (Z direction) with side surfaces of each of the adhesion layer 122 and the seed layer 123.

[0081] The adhesion layer 122 and the seed layer 123 may be disposed between the redistribution structure 100 and the UBM pad 147. The adhesion layer 122 may be in contact with at least a part of each of the redistribution insulating layer 110 and the redistribution line pattern 120. The seed layer 123 may be in contact with at least a part of the lower surface of

the lower UBM pad 144, the side surfaces of the lower UBM pad 144, and the lower surface of the upper UBM pad 146.

[0082] Referring to FIG. 13, a plating layer PL covering at least a part of each of the upper surface and the side surfaces of the upper UBM pad 146 is formed. In order for the plating layer PL to cover the side surfaces of the adhesion layer 122, the side surfaces of the seed layer 123, and the side surfaces of the upper UBM pad 146, the plating layer PL may be formed after the mask pattern MP is removed.

[0083] The plating layer PL may include a conductive material such as copper (Cu), aluminum (Al), silver (Ag), tin (Sn), gold (Au), nickel (Ni), lead (Pb), titanium (Ti), or an alloy thereof. The plating layer PL may be formed using an electroless plating method. For example, the plating layer PL may be formed using an immersion plating method. When the plating layer PL is formed using an electroless plating method, a thickness of the plating layer PL may be reduced, and a manufacturing process may be simple, and thus, the plating layer PL may be efficiently formed. In addition, when the plating layer PL is formed using an electroless plating method, electrical noise may be reduced and process reliability may be increased.

[0084] Although not shown in the drawing, surface treatment may be performed on the upper UBM pad 146 before the plating layer PL is formed.

[0085] Although not shown in FIG. 13, when the first additional plating layer 148 and/or the second additional plating layer 149 is disposed between the upper surface of the upper UBM pad 146 and the plating layer PL, the UBM pad 147a or 147b of FIG. 3 or FIG. 4 may be formed.

[0086] Referring to FIG. 14, the semiconductor chip 200 is mounted on a resultant of FIG. 13, and the molding layer 300 is formed on the redistribution structure 100.

[0087] First, the connection member 150 may be mounted on the UBM pad 147. The connection member 150 in contact with the semiconductor chip 200 may be attached onto the plating layer PL through a reflow process. As described above, the plating layer PL is formed on the upper surface and the side surfaces of the upper UBM pad 146, and thus, the connection member 150 may also be in contact with the upper surface and the side surfaces of the upper UBM pad 146. In addition, the connection member 150 may be in contact with the upper surface of the redistribution structure 100, the adhesion layer 142, and the seed layer 143. Accordingly, a contact surface between the connection member 150 and the UBM pad 147 increases, and thus, the electrical characteristics of the semiconductor package 10 may be improved.

[0088] In a process of attaching the connection member 150 onto the UBM pad 147, the plating layer PL may diffuse into the connection member 150. Accordingly, the UBM pad 147 and the connection member 150 may be in contact with each other, and the connection member 150 may include the material of the plating layer PL. For example, when the plating layer PL includes gold (Au), the connection member 150 may also include gold (Au).

[0089] The semiconductor chip 200 may be an individualized semiconductor die, or may be a sub-package in which the semiconductor die is molded. The semiconductor chip 200 is mounted so that the active surface on which the chip pad 240 is formed faces downward, so that the chip pad 240 of the semiconductor chip 200 may be aligned with the upper surface of the UBM pad 147.

[0090] A plurality of semiconductor chips 200 may be mounted. Some of the plurality of semiconductor chips 200 may be logic chips, and the others may be memory chips.

[0091] In a process of electrically connecting the connection member 150 to the semiconductor chip 200, a gap may be formed between the connection member 150 and the semiconductor chip 200. Because the gap may cause a problem in the reliability of connection between the connection member 150 and the semiconductor chip 200, an underfill (not shown) may be injected and hardened to reinforce the connection.

[0092] By the underfill, the semiconductor chip 200 is more stably fixed on the connection member 150, and despite a difference in thermal expansion coefficient between the connection member 150 and the semiconductor chip 200, the connection member 150 and the semiconductor chip 200 are not electrically separated. In some cases, the molding layer 300 may be directly filled into the gap between the connection member 150 and the semiconductor chip 200, and in this case, the underfill may not be necessary.

[0093] The molding layer 300 may cover the side and upper surfaces of the semiconductor chip 200 on the redistribution structure 100. In some embodiments, the molding layer 300 may cover only the side surfaces of the semiconductor chip 200 so that the upper surface of the semiconductor chip 200 is exposed to the outside. The molding layer 300 may serve to protect the semiconductor chip 200 from external influences such as shock. For example, the molding layer 300 may include epoxy mold compound, resin, etc.

[0094] Referring to FIG. 15, a second carrier substrate CS2 may be attached onto the molding layer 300 to face the first carrier substrate CS1, and the first carrier substrate CS1 of FIG. 14 may be removed.

[0095] The second carrier substrate CS2 may be substantially the same as the first carrier substrate CS1 in FIG. 14. In order to facilitate attachment of the second carrier substrate CS2,

a second adhesion film (not shown) may be formed between the second carrier substrate CS2 and the molding layer 300. The adhesion film may be in a liquid form or a gel form that may be easily deformed at a certain pressure.

[0096] Thereafter, after turning over a resultant, the external connection terminal 160 may be formed on the lower surface of the redistribution structure 100. The external connection terminal 160 may be formed through a reflow process. The external connection terminal 160 may be formed on the lower surface of the redistribution structure 100 so that the semiconductor package 10 of FIG. 1 may be formed.

[0097] In a general semiconductor package manufacturing method, a plating layer is disposed on an upper surface of a UBM pad, and side surfaces of the UBM pad are not in contact with a connection member.

[0098] On the other hand, in the method of manufacturing the semiconductor package of the inventive concept, the plating layer PL may be in contact with the side surfaces of the UBM pad 147, and the connection member 150 may be in contact with the side surfaces of the UBM pad 147. Accordingly, the contact area between the UBM pad 147 and the connection member 150 may increase, and thus, the electrical characteristics of the semiconductor package 10 may be improved.

[0099] While the inventive concept has been particularly shown and described with reference to embodiments thereof, it will be understood that various changes in form and details may be made therein without departing from the spirit and scope of the following claims.

WHAT IS CLAIMED IS:

1. A semiconductor package comprising:
an interposer;
a semiconductor chip disposed on the interposer;
an under bump metal (UBM) pad disposed between the interposer and the semiconductor chip and comprising an upper UBM pad and a lower UBM pad; and
a connection member disposed between the UBM pad and the semiconductor chip,
wherein the connection member is in contact with side surfaces of the UBM pad and the interposer.
2. The semiconductor package of claim 1, further comprising: an adhesion layer and a seed layer disposed between the lower UBM pad and the interposer,
wherein the connection member is in contact with the adhesion layer or the seed layer.
3. The semiconductor package of claim 2, wherein side surfaces of the lower UBM pad, side surfaces of the adhesion layer, and side surfaces of the seed layer are aligned in a vertical direction.
4. The semiconductor package of any one of claims 1 to 3, wherein a horizontal width of the upper UBM pad is wider than a horizontal width of the lower UBM pad.
5. A method of manufacturing a semiconductor package, the method comprising:
forming an interposer;
forming an under bump metal (UBM) pad on the interposer;
forming a plating layer on the UBM pad; and
attaching a connection member onto the UBM pad,
wherein the plating layer is in contact with side surfaces of the UBM pad.
6. The method of claim 5, wherein the plating layer is in contact with the interposer.
7. The method of claim 5 or claim 6, wherein the forming of the UBM pad includes:

forming an adhesion layer and a seed layer on the interposer;
forming a mask pattern on the seed layer; and
forming a pad on the seed layer, and
wherein the forming of the plating layer is performed after removing the mask pattern.

8. The method of any one of claims 5 to 7, wherein the forming of the plating layer is performed by an electroless plating method.

9. A method of manufacturing a semiconductor package, the method comprising:
forming an interposer;
forming an under bump metal (UBM) pad on the interposer;
mounting a semiconductor chip on the UBM pad; and
molding the semiconductor chip,
wherein the mounting of the semiconductor chip on the UBM pad includes
forming a plating layer on the UBM pad; and
attaching a connection member onto the UBM pad,
the plating layer is in contact with side surfaces of the UBM pad.

10. The method of claim 9, wherein the connection member includes a material of the plating layer.