CLAIMS:

1. A processor comprising:

a plurality of cores, wherein each of the plurality of cores comprises a multi-threaded core to concurrently execute a plurality of threads; ~~and~~

a control circuit to concurrently enable at least one of the plurality of cores to operate in a single-threaded mode and at least one other of the plurality of cores to operate in a multi-threaded mode; and

a configuration storage to store an enable indicator for each of the plurality of cores to indicate whether the core is enabled to operate in the multi-threaded mode, and wherein the enable indicator for each of the plurality of cores is statically configured by a manufacturer of the processor.

~~2. The processor of claim 1, further comprising a configuration storage to store an enable indicator for each of the plurality of cores to indicate whether the core is enabled to operate in the multi-threaded mode.~~

~~3~~2. The processor of claim ~~2~~1, wherein the configuration storage comprises a fuse storage.

~~4. The processor of claim 2, wherein the configuration storage is to be written by firmware.~~

~~5. The processor of claim 4, wherein the firmware comprises a user selection interface to enable a user to select a number of the plurality of cores to be enabled for the multi-threaded mode.~~

~~6~~3. The processor of claim ~~2~~1, further comprising a configuration register to store a selective multi-threading indicator to indicate whether the control circuit is enabled to concurrently enable operation of the processor in the single-threaded mode and the multi-threaded mode.

~~74~~74. The processor of claim ~~21~~1, further comprising:

a power controller to control power consumption of the processor; and

a memory to store a bit mask based on the enable indicator for each of the plurality of cores, wherein the power controller is to communicate at least a first portion of the bit mask to a first microcode engine of a first core to cause the first microcode engine to configure the first core to operate in the single-threaded mode, and communicate at least a second portion of the bit mask to a second microcode engine of a second core to cause the second microcode engine to configure the second core to operate in the multi-threaded mode.

~~85~~5. The processor of claim ~~74~~4, wherein the first microcode engine is to disable one or more multi-threading structures of the first core in response to the first portion of the bit mask.

~~96~~6. The processor of claim 1, further comprising a power controller, wherein the power controller is to enable a first core to operate at a turbo mode frequency, the first core enabled to operate in the single-threaded mode, wherein the turbo mode frequency comprises a first baseline turbo mode frequency for the single-threaded mode, the first baseline turbo mode frequency greater than a second baseline turbo mode frequency for the multi-threaded mode.

~~107~~7. At least one computer readable storage medium having stored thereon instructions, which if performed by a machine cause the machine to perform a method comprising:

receiving, in a controller of a processor having a plurality of cores, a selection of an asymmetric multi-threading configuration of the processor in which at least one first core is enabled to operate in a multi-threaded mode and at least one second core is enabled to operate in a single-threaded mode;

communicating first configuration information from the controller to a first engine of the at least one first core to cause the first engine to configure the at least one first core for the multi-threaded mode; and

communicating second configuration information from the controller to a first engine of the at least one second core to cause the first engine of the second core to configure the at least one second core for the single-threaded mode; and

the received selection of the asymmetric multi-threading configuration of the processor comprises an enable indicator for each of the plurality of cores to indicate whether the core is enabled to operate in the multi-threaded mode, and wherein the enable indicator for each of the plurality of cores is statically configured by a manufacturer of the processor.

~~11. The at least one computer readable storage medium of claim 10, wherein the method further comprises receiving the selection of the asymmetric multi-threading configuration from a user via a user interface of a basic input/output system to enable the user to identify a number of the plurality of cores to operate in the multi-threaded mode and a number the plurality of cores to operate in the single-threaded mode.~~

~~12. The at least one computer readable storage medium of claim 10, wherein the method further comprises receiving the selection of the asymmetric multi-threading configuration from a basic input/output system based on the selection of the asymmetric multi-threading configuration by an original equipment manufacturer.~~

~~13~~8. The at least one computer readable storage medium of claim 10, wherein the method further comprises:

enabling the at least one first core to operate at a first operating frequency; and enabling the at least one second core to operate at a turbo mode frequency, the turbo mode frequency greater than the first operating frequency.

~~14~~9. The at least one computer readable storage medium of claim 10, wherein the method further comprises:

determining that the processor has sufficient power and thermal headroom; and

in response to determining that the processor has sufficient power and thermal headroom, enabling the at least one second core to operate at a second turbo mode frequency greater than a maximum turbo mode frequency at which the at least one first core can operate.

~~15~~10. A system comprising:

a processor comprising:

a plurality of cores, wherein each of the plurality of cores comprises a multi-threaded core to concurrently execute a plurality of threads; and

a control circuit to concurrently enable, based at least in part on selective multi-threaded configuration information, a first core of the plurality of cores to operate in a single-threaded mode and a second core of the plurality of cores to operate in a multi-threaded mode; and

a configuration storage to store an enable indicator for each of the plurality of cores to indicate whether the core is enabled to operate in the multi-threaded mode, and wherein the enable indicator for each of the plurality of cores is statically configured by a manufacturer of the processor.

~~a non-volatile memory coupled to the processor to store a basic input/output system (BIOS), the BIOS including:~~

~~a first region to store the selective multi-threaded configuration information to identify a first subset of the plurality of cores to be enabled for the single-threaded mode and a second subset of the plurality of cores to be enabled for the multi-threaded mode; and~~

~~first code to cause the selective multi-threaded configuration information to be communicated to the processor.~~

~~16. The system of claim 15, wherein the BIOS further comprises second code to generate a user interface to enable a user to identify a number of the plurality of cores to be enabled for the single-threaded mode and a number of the plurality of cores to be enabled for the multi-threaded mode.~~

~~17. The system of claim 15, wherein the processor further comprises a configuration storage to store an enable indicator for each of the plurality of cores to indicate whether the core is enabled to operate in the multi-threaded mode.~~

~~18. The system of claim 17, wherein the BIOS further comprises a third code to write the enable indicator for each of the plurality of cores based on the selective multi-threaded configuration information.~~

~~19.~~11 The system of claim ~~17~~10, wherein the processor further comprises a memory to store a bit mask based on the enable indicator for each of the plurality of cores, wherein a first microcode engine of the first core is to enable the first core for the single-threaded mode based on a first portion of the bit mask, and a second microcode engine of the second core is to enable the second core for the multi-threaded mode based on a second portion of the bit mask.

~~20~~12. The system of claim ~~15~~10, wherein the processor further comprises a power controller to enable the first core to operate at a turbo mode frequency, wherein the turbo mode frequency comprises a first baseline turbo mode frequency for the single-threaded mode, the first baseline turbo mode frequency greater than a second baseline turbo mode frequency for the multi-threaded mode.