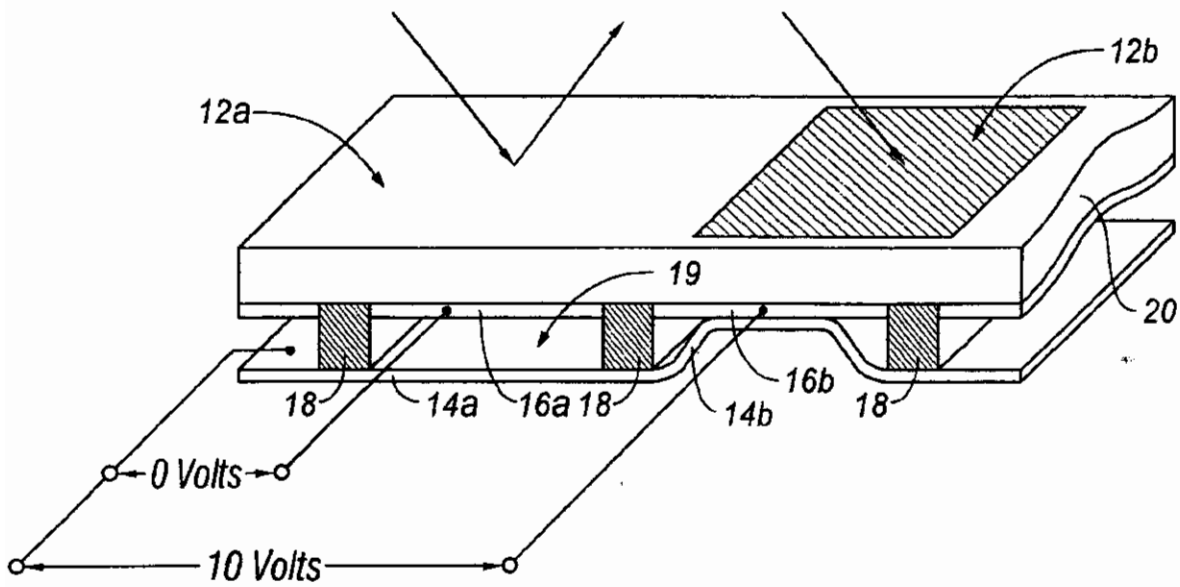

FIG. 1

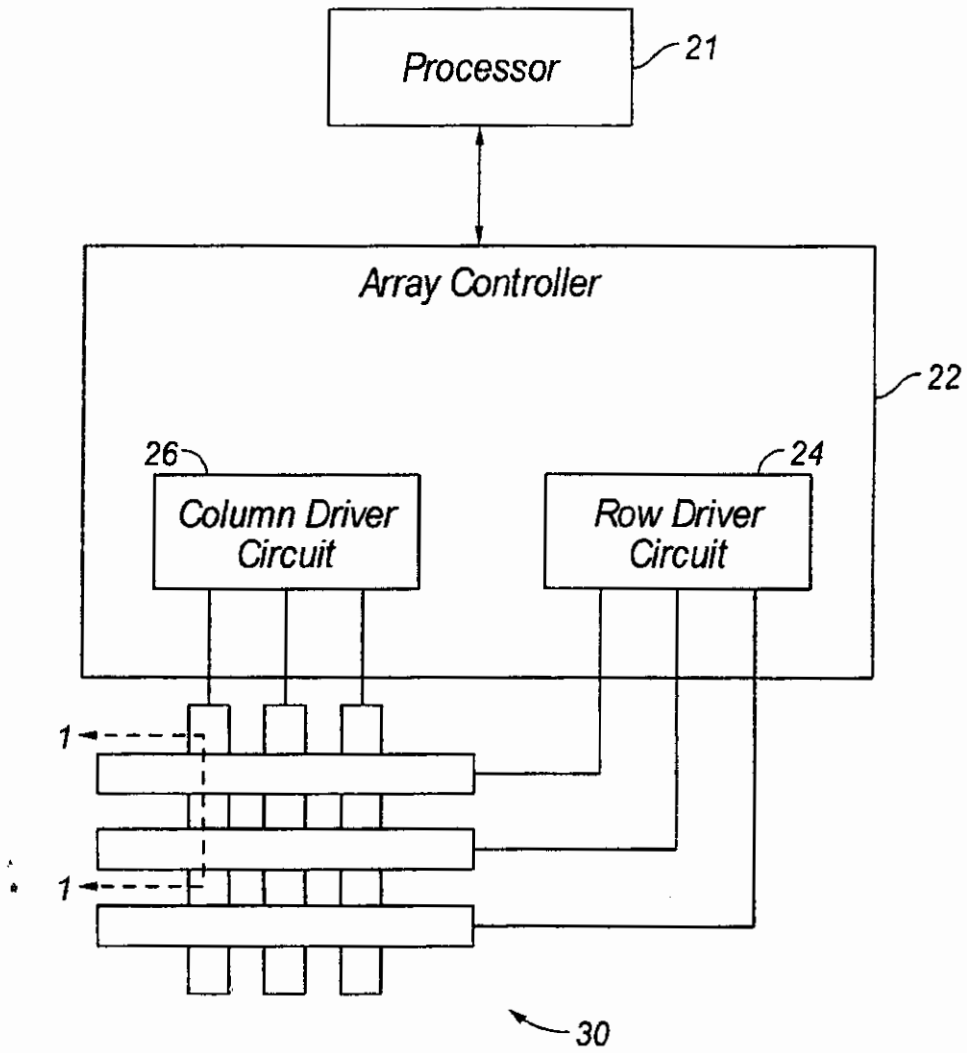
Processor
21
Array Controller
22
26
Column Driver Circuit
24
Row Driver Circuit
1
1
30

FIG. 2

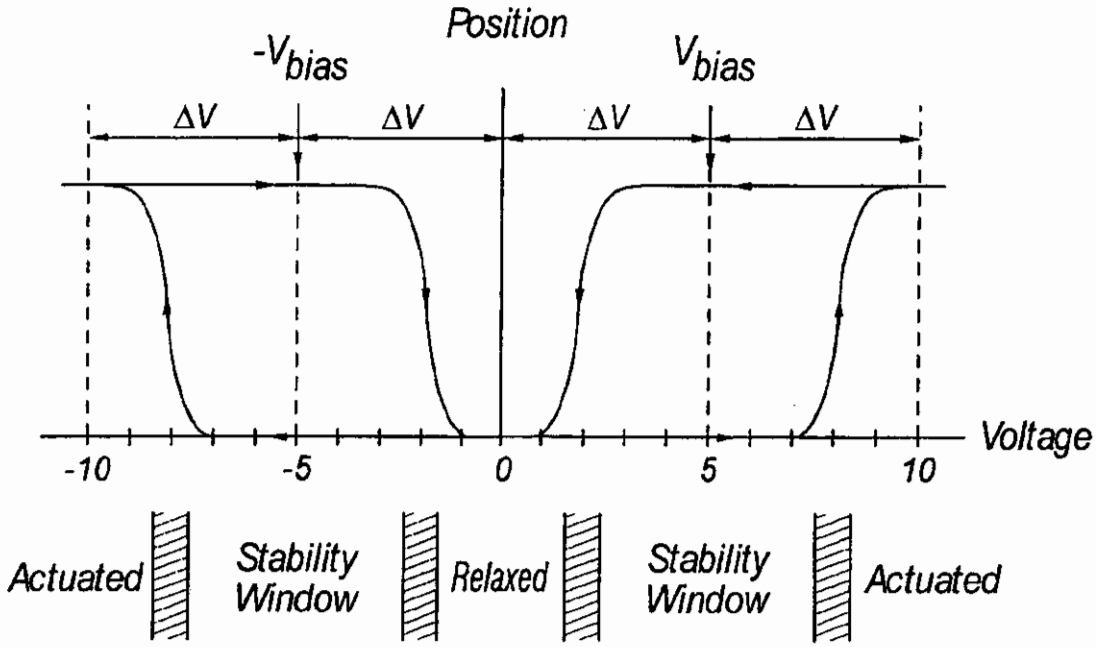

FIG. 3

Row Output Signals	Column Output Signals: $+V_{bias}$	Column Output Signals: $-V_{bias}$
0	Stable	Stable
$+\Delta V$	Relax	Actuate
$-\Delta V$	Actuate	Relax

FIG. 4

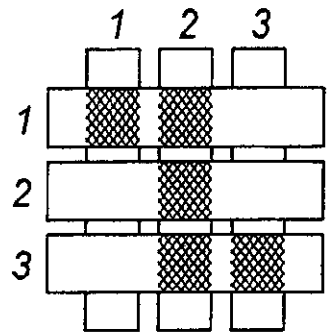
1
2
3
1
2
3

FIG. 5A

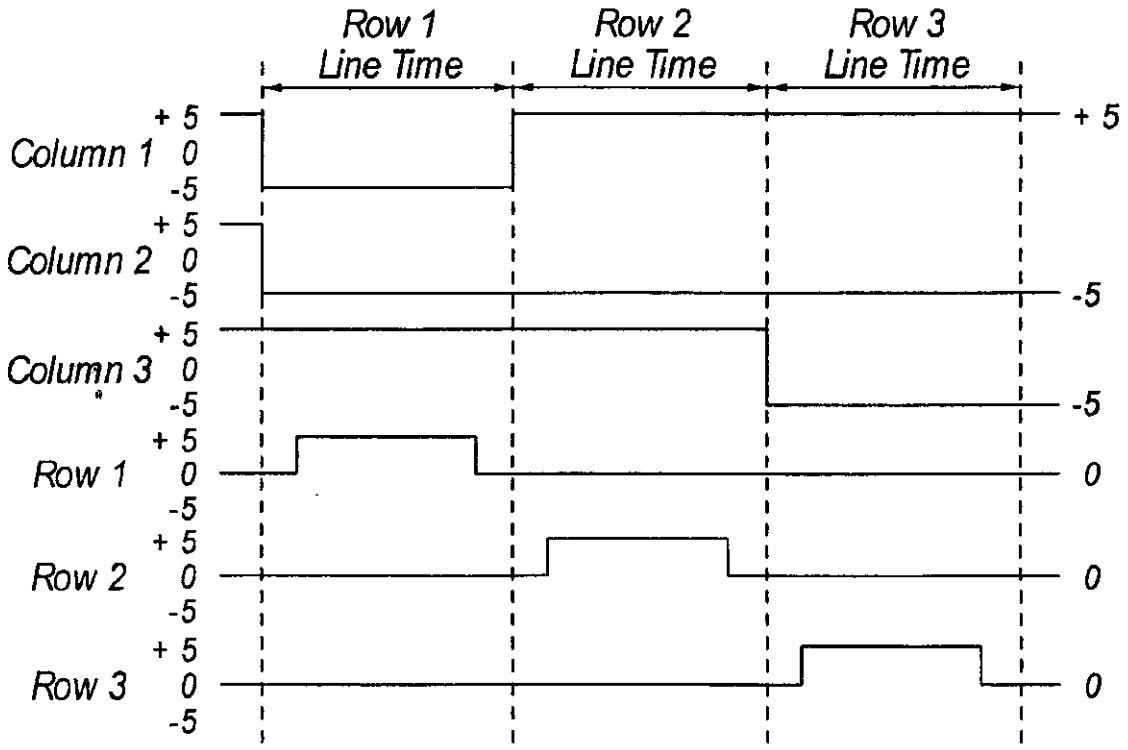
Row 1 Line Time
Row 2 Line Time
Row 3 Line Time
Column 1
Column 2
Column 3
Row 1
Row 2
Row 3
+ 5
0
-5
+ 5
-5
-5
0
0
0

FIG. 5B

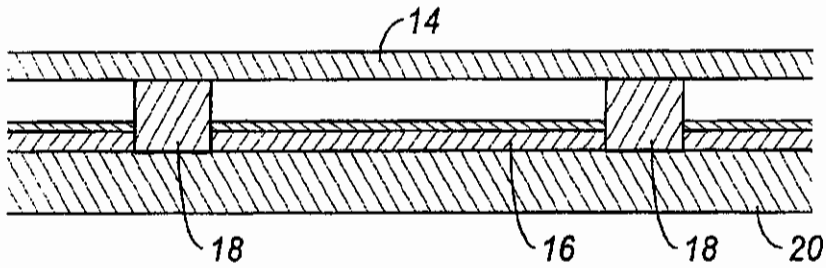

FIG. 6A

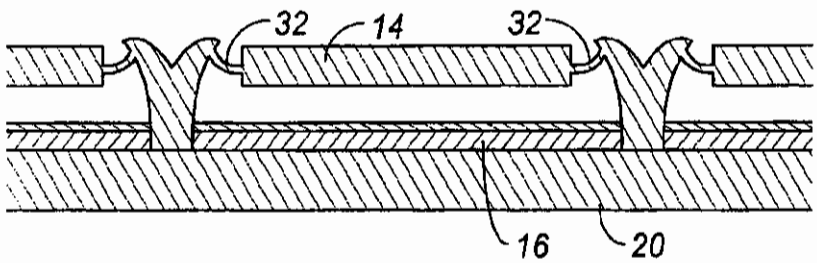

FIG. 6B

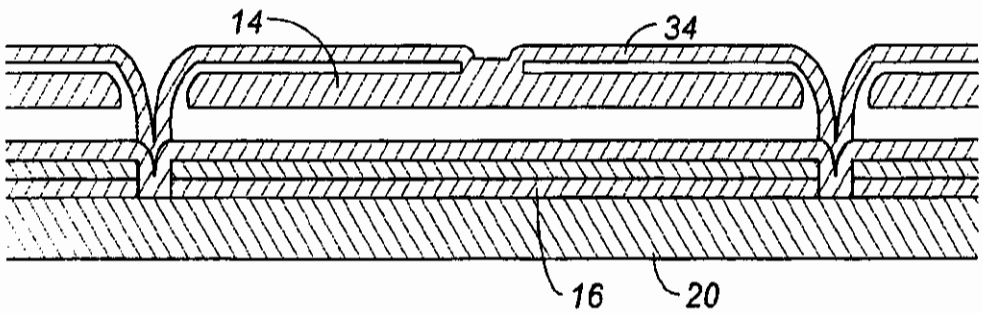

FIG. 6C

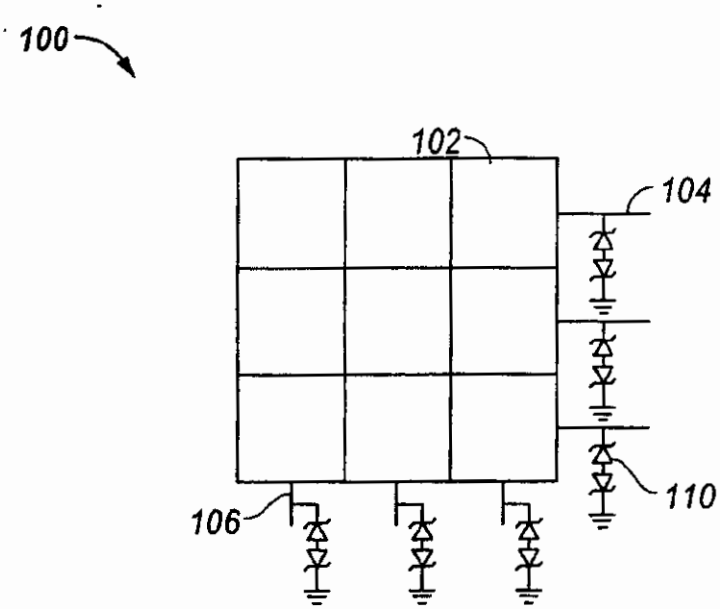

FIG. 7

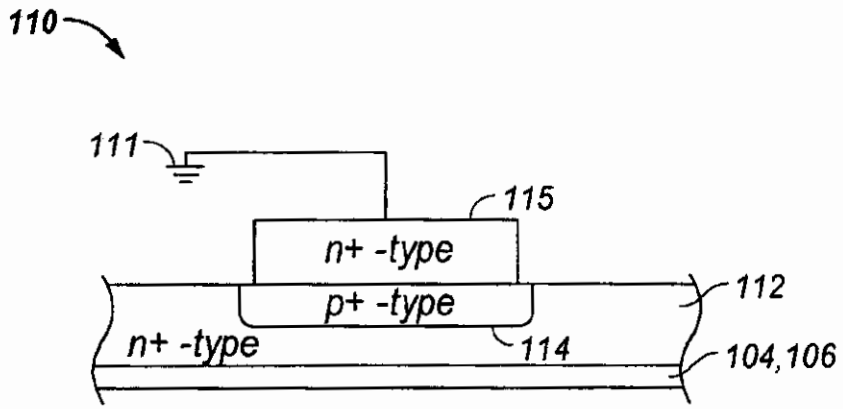

FIG. 8

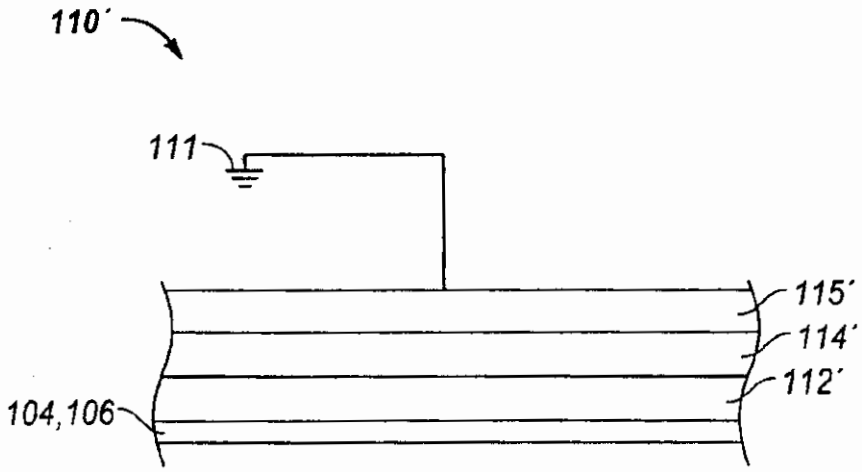

FIG. 9

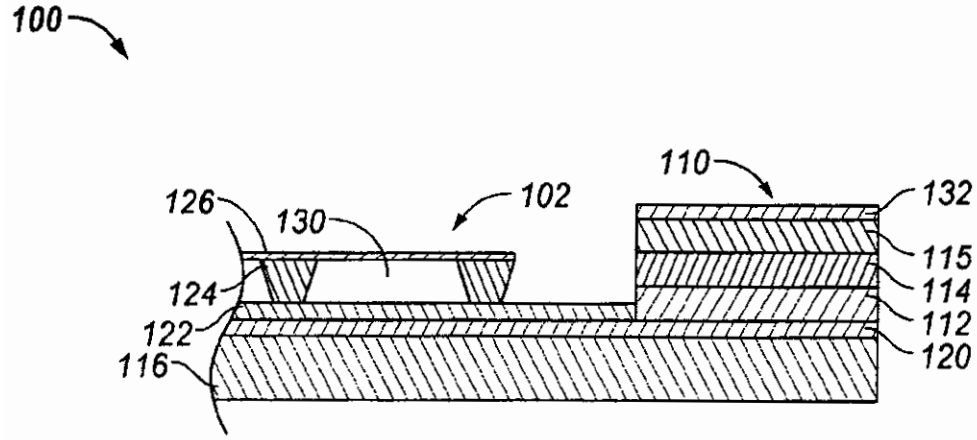
100
110
102
126
130
132
115
124
114
122
112
116
120

FIG. 10

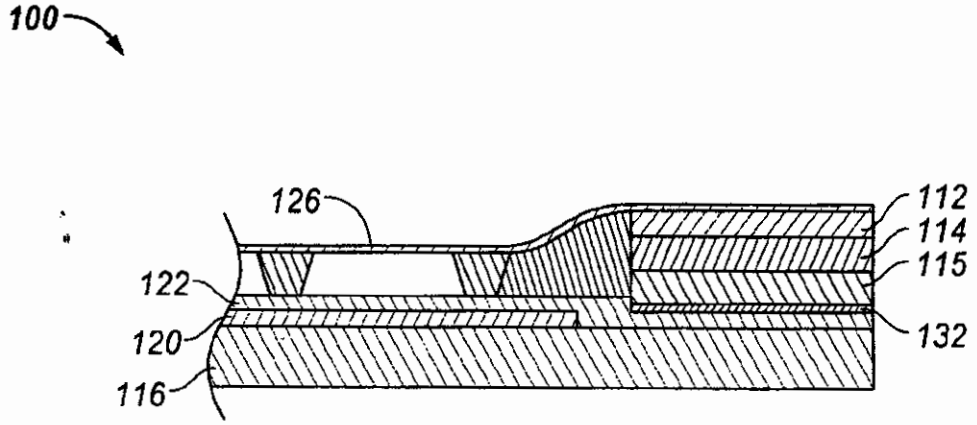
100
126
112
114
122
115
120
132
116

FIG. 11



FIG. 12A

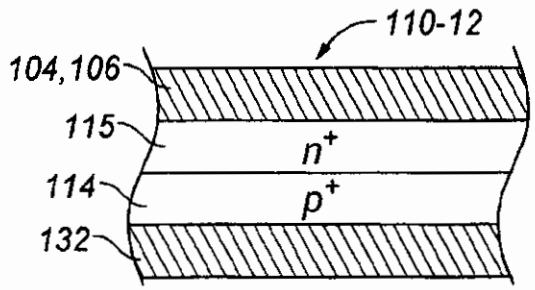

FIG. 12B

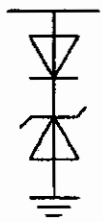

FIG. 13A

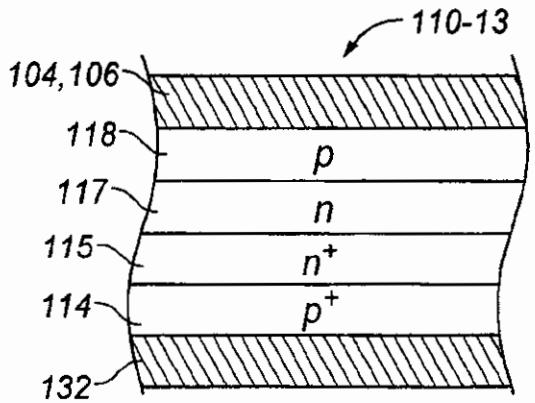

FIG. 13B

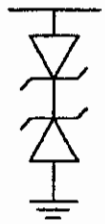

FIG. 14A

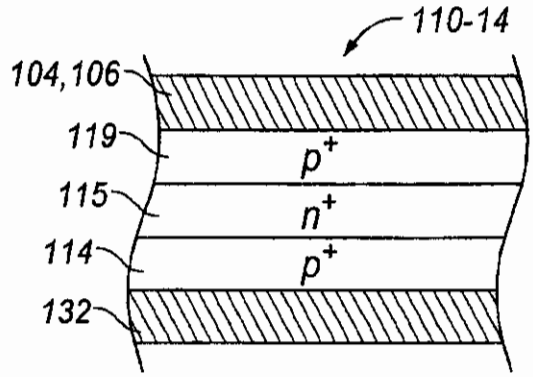

FIG. 14B

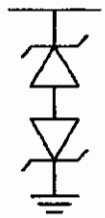

FIG. 15A

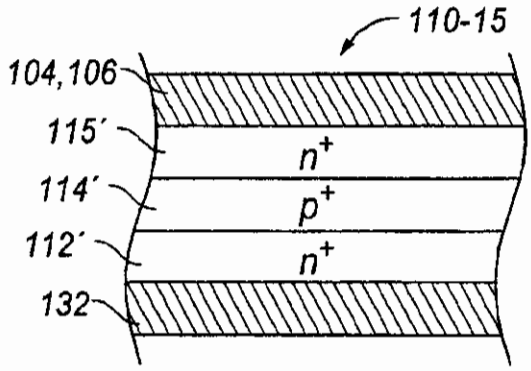

FIG. 15B

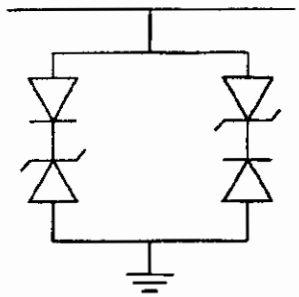

FIG. 16A

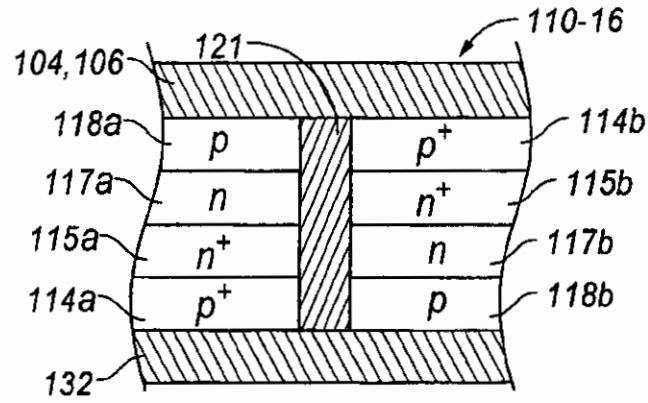

FIG. 16B

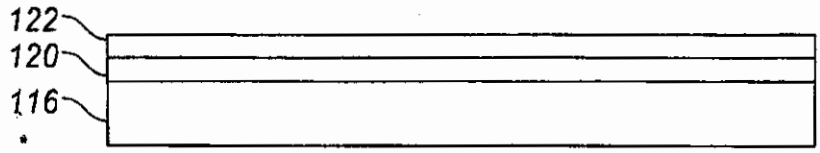

FIG. 17A

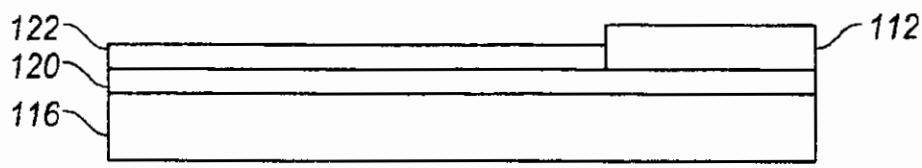

FIG. 17B

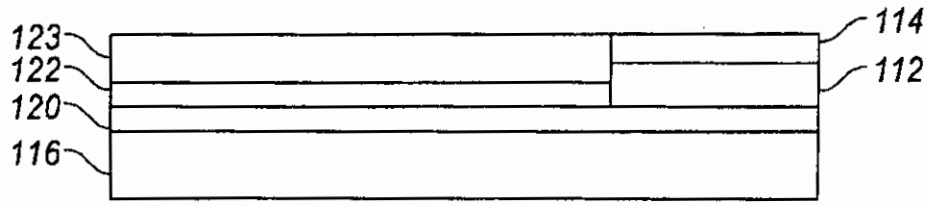

FIG. 17C

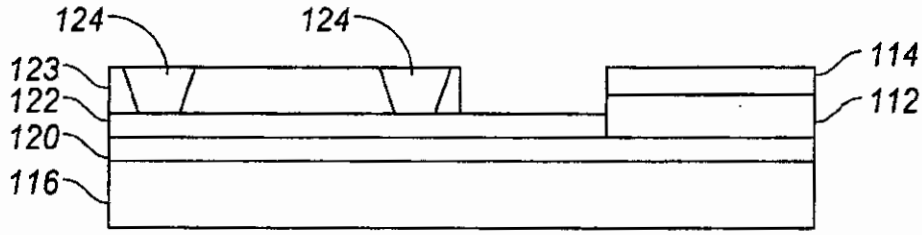

FIG. 17D

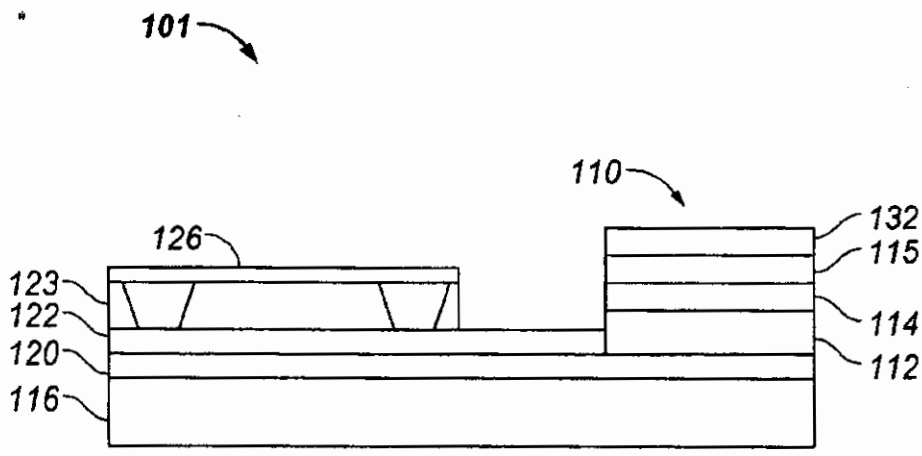

FIG. 17E

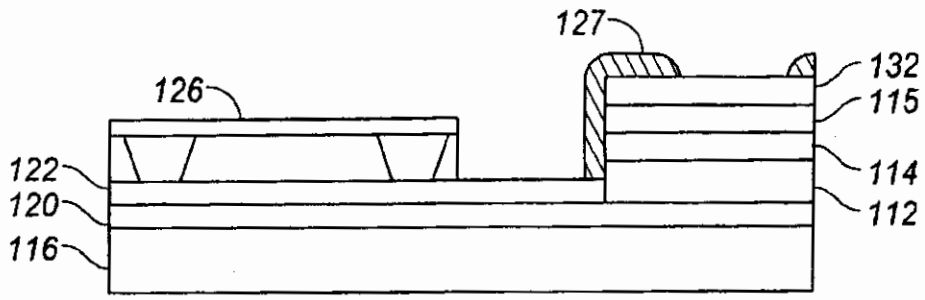

FIG. 17F

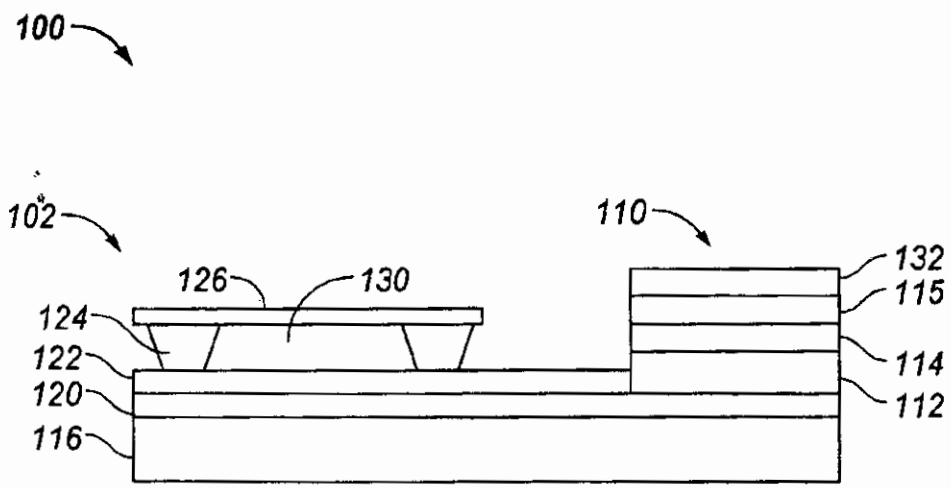

FIG. 17G

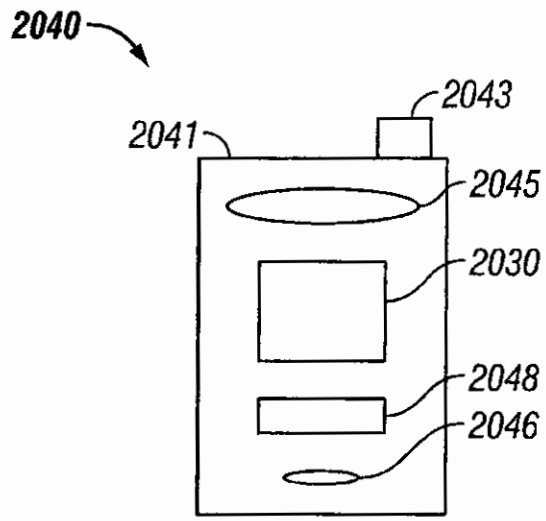

FIG. 18A

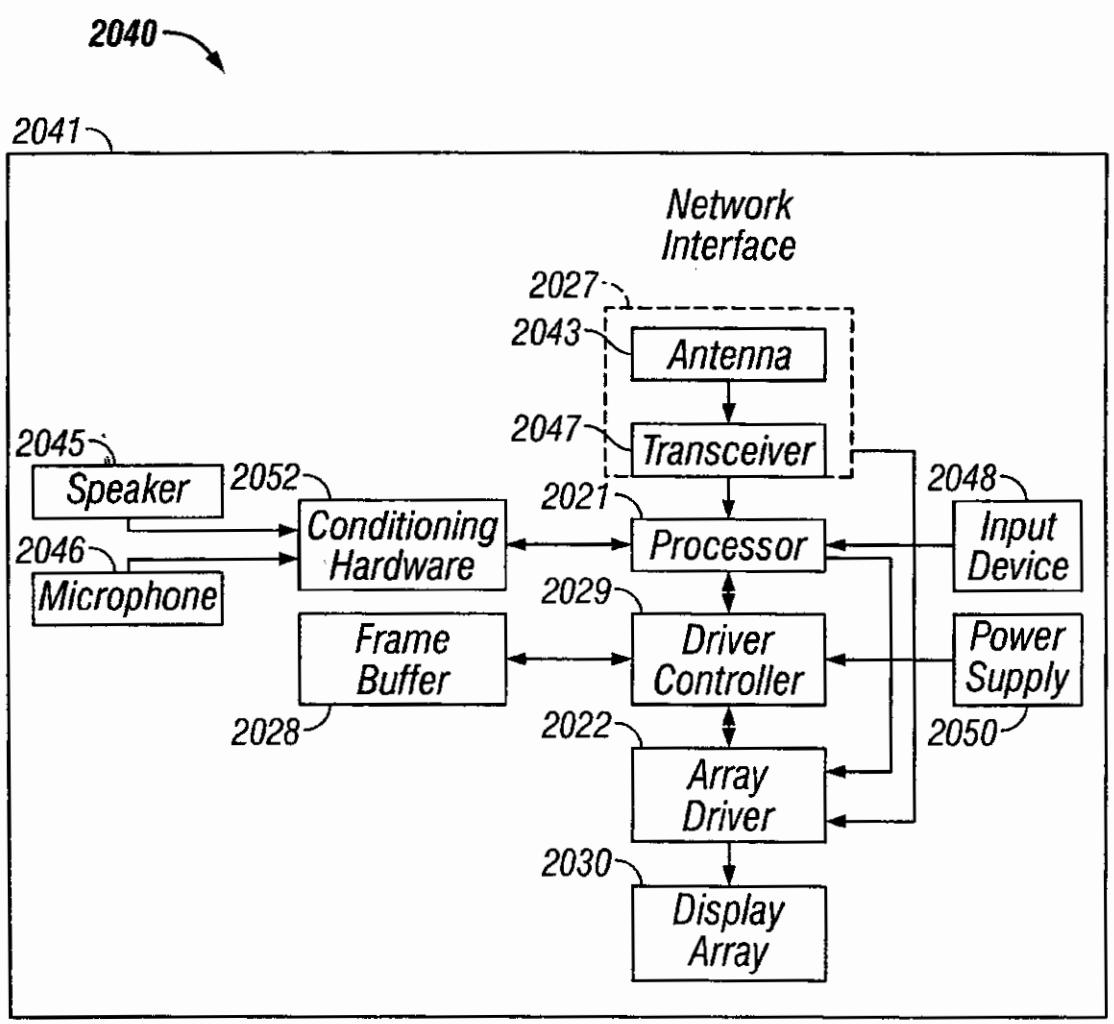

FIG. 18B