THERMALLY ENHANCED SEMICONDUCTOR PACKAGE AND METHOD OF PRODUCING THE SAME

BACKGROUND OF THE INVENTION

Field of the Invention

[01] The present invention relates to a thermally enhanced package for a semiconductor chip and a method of forming the same. It includes, but is not limited to, a package with an integrated heat sink for ball grid arrays (PBGAs and FBGAs), multi chip modules (MCMs) and quad flat nonleaded packages (QFNs).

Description of the Related Art

[02] The quest to increase functionality and chip speeds is a continuous ongoing effort by every chip designer in the Semiconductor industry. The increase in signal speeds in the chips poses considerable challenges for thermal management. Higher signal speeds and higher functionality leads to higher junction temperatures. To keep the junction temperatures low, various thermal solutions are available.

[03] Plastic Ball grid array (PBGA) packages are encapsulated individually. Therefore, one thermal solution is a drop-in heat sink that is embedded during encapsulation. However, drop-in heat sinks take-up space within the package, posing constraints in the placement of active chips and other devices. For example, figure 2 shows a cross-sectional view of a PBGA package that includes a drop-in heat sink 4.

[04] Highly mass produced laminate based packages such as fine pitch BGAs (FBGAs), are arrayed and are molded in panel form and singulated to produce individual FBGA packages. Arrayed packages don't allow space for individual drop-in heat sinks and it is not economical to waste substrate real estate to have individual drop-in heat sinks for FBGA. Therefore, some

approaches to deal with thermal management include the use of arrayed heat sinks with connecting down sets. However, these types of heat sinks have quality issues such as mold flash during the molding process. These quality issues lead to both aesthetic and as well as thermal performance problems.

[05] Other known methods of incorporating heat sinks into packages also have several disadvantages. For example, they include multiple process steps which increase production time and costs. In addition, the heat sinks can be misaligned. Also, heat sinks can be easily peeled-off.

[06] One of the current methods of producing a thermally enhanced semiconductor package is by attaching the heat sink 1 onto top surface of the fully molded semiconductor package by means of an adhesive layer 3 as shown in figure 1. However, this method provides an inconsistent adhesive coverage when the heat sink is attached, which might lead to easy removal of the heat sink. Other issues encountered with this method include controlling the amount of adhesive 3 needed to attach the heat sink 1 to the molded surface 2. Excessive adhesive 3 can cause bleed out, which ultimately contaminates the package edges or the contact pads. Insufficient adhesive coverage can also cause large gaps that adversely affect thermal performance. Finally, attaching heat sink 1 after singulation is not economically viable considering the mass scale production requirements of the package.

[07] One object of the present invention is to provide a method of packaging an embedded heat sink semiconductor package whereby the semiconductor package has good thermal characteristics and can be assembled with a simple manufacturing process.

[08] Another object of the present invention is to provide a heat sink structure that provides a vertical cushioning effect during molding.

[09] Another object of the present invention is to provide a heat sink structure that created a lifting force that keeps the heat sink structure engaged with the release film during molding.

[10] Another object of the present invention is to provide a heat sink structure that inhibits mold flash on the heat sinks.

[11] Another object of the present invention is to provide a package that includes a notch of encapsulant around the corner of the package to act as an interlock for the heat sink, enhancing the holding strength between the heat sink and cured encapsulant.

[12] Some of the innovativeness of this package is that it can be applied to any arrayed, lead frame based or laminate based packages which are molded on one side of the substrate. The heat sink can be any thermally conductive material (for example, copper).

SUMMARY OF THE INVENTION

[13] This invention includes a heat sink structure for use in a semiconductor package that includes a ring structure with down sets and a heat sink connected to the ring structure. The down sets can be slanted or V-shaped.

[14] The heat sink structure may include a plurality of heat sinks, including the plurality of heat sinks being arranged in an array. Also, the heat sink structure may include a plurality of heat sink arrays.

[15] The heat sink structure may include etched tie bars that connect the heat sink to the ring structure and alignment holes for aligning the heat sink and substrate.

[16] The invention also includes a method of manufacturing a semiconductor package that includes inserting a substrate with an attached semiconductor chip in a first mold portion, placing a heat sink structure on top of a portion of the substrate, placing a mold release film onto a second mold portion, clamping a second mold portion onto a portion of the heat sink structure, injecting an encapsulant into a mold cavity, wherein the encapsulant surrounds portions of the substrate, semiconductor chip and heat sink structure, curing the encapsulant, whereby the heat sink structure adheres to the encapsulant, removing the encapsulated assembly from the mold and singulating the encapsulated assembly to form a semiconductor package.

[17] The method may also include using a vacuum to force the mold release film onto the second mold portion.

[18] The method may also include attaching solder balls to the substrate and aligning the substrate with attached semiconductor chip and heat sink structure in the first mold portion through the use of guide pins.

[19] The method may also include singulating the encapsulated package through a down set or etched tie bar.

[20] When the method is used the down sets may create a lifting force when the encapsulant is injected in the mold cavity, may provide a cushioning effect and may keep the heat sink on the heat sink structure engaged with said mold release film while said encapsulant is being injected in to the mold cavity.

[21] The method may also include attaching a high temperature tape on a bottom portion of the substrate wherein the high temperature tape will fit into a relief slot in the first mold portion.

[22] The invention also includes a semiconductor package that includes a semiconductor chip attached to a substrate, an encapsulant covering portions of the semiconductor chip and substrate and comprising a top surface, and a heat sink in direct contact with the entire top surface of the encapsulant. The heat sink becomes adhered to the top surface of the encapsulant as the encapsulant cures and a notch at a top corner of semiconductor package is filled with the encapsulant.

[23] The notch may be defined by a side of the heat sink and a down-set or by a side of the heat sink and a tie bar and acts as an interlock for the heat sink, enhancing the holding strength between the heat sink and cured encapsulant.

[24] The package may also include solder balls connected to the substrate and the semiconductor chip being wire bonded to the substrate.

[25] The package may include a substrate that is a laminate structure or a metal lead-frame structure. In addition, the semiconductor package may be a ball grid array package, a quad flat nonleaded package or is a multi chip module package.

BRIEF DESCRIPTION OF THE DRAWINGS

[26] Many aspects of the invention can be better understood with reference to the following drawings. The components in the drawings are not necessarily to scale, emphasis instead being placed upon clearly illustrating the principles of the present invention. Moreover, in the drawings, like reference numerals designate corresponding parts throughout the several views.

[27] Figure 1 illustrates a conventional method of producing the thermally enhanced semiconductor package.

[28] Figure 2 illustrates another conventional method of producing a thermally enhanced semiconductor package.

[29] Figures 3-9 illustrate a method according to the present invention of producing a thermally enhanced semiconductor package.

[30] Figure 10 illustrates an embodiment of a thermally enhanced semiconductor package.

[31] Figures 11-12 illustrate another method according to the present invention of producing a thermally enhanced semiconductor package.

[32] Figures 13 and 14 show top views of 2x2 array and 3x3 array of heat sinks.

[33] Figure 15 shows a partial plan view of a heat sink frame carrier.

[34] Figure 16 shows a flash free molded package with a heat sink 203.

[35] Figure 17 shows a completely assembled thermally enhanced semiconductor package with an embedded heat sink.

[36] Figure 18 shows an example of a mold release film being forced up against the top mold portion by a vacuum and conforming to the mold cavity.

[37] Figures 19 and 20 show cross-sectional views of 2x2 and 3x3 array heat sinks.

[38] Figures 21 and 22 show an assembly concept of a QFN package with an integrated heat sink.

DETAILED DESCRIPTION OF THE ILLUSTRATIVE NON-LIMITING EMBODIMENTS OF THE INVENTION

[39] Hereinafter, the present invention will be described in detail by way of exemplary embodiments with reference to the drawings. The described exemplary embodiments are intended to assist in the understanding of the invention, and are not intended to limit the scope of the invention in any way. Throughout the drawings for explaining the exemplary embodiments, those components having identical functions carry the same reference numerals for which duplicate explanations will be omitted.

[40] A non-limiting embodiment of a method for thermally enhancing a semiconductor package is described below. First, as shown in figure 3, a chip 101 is attached to a substrate 102. Substrate 102, can be a laminate structure or metal lead-frame. Item 100 represents the substrate and attached chip assembly. Several methods may be used to attach the chip to the substrate. For example, epoxy dispense/print and chip attach or a pre-taped chip can be directly attached to the substrate. In addition, the chip 101 may be wire bonded to the substrate. However, the present invention is not limited to wire bonded chips. For example, it could apply to flip chips, and the like.

[41] Next, as shown in figure 4, substrate and attached chip assembly 100 is loaded onto a bottom mold portion 103. The substrate 102 may contain alignment holes through which guide pins 104 are inserted. Other known alignment methods could also be used.

[42] In figure 5, heat sink structure 105, which includes heat sink 105a, rail/frame carrier 105b and down-set 105c is placed on top of the substrate 102. Heat sink structure 105 can be in a strip form. Heat sinks are metal structures capable of absorbing heat from the chip and dissipating heat to the environment. To ensure proper alignment between heat sink structure 105

and substrate 102, the heat sink structure may also contain alignment holes through which the same set of guide pins 104 are inserted. Other known alignment methods could also be used.

[43] As shown in figure 6, top mold portion 107 and bottom mold portion 103 are then closed to start the encapsulation process. Top mold portion 107 is clamped on heat sink structure rail 105b.

[44] A mold release film 106 can be inserted between the top mold portion 107 and the heat sink 105a. The mold release film protects the surface of the heat sink 105a and prevents contamination from the encapsulation material. Examples of mold release films are ETFE films which can withstand molding temperatures. If a mold release film is used, one method of using it in the mold it to use a vacuum to force the mold release film 106 up against the top mold portion 107 and conform the film to the shape of the cavity. An example of the mold release film being forced up against the top mold portion by a vacuum is shown in figure 18. Other methods may be used to insert the mold release film between the heat sink structure and top mold portion.

[45] During the encapsulation process, an encapsulant 113, such as a thermo set epoxy, is injected into the mold to fill the open spaces and is cured. The bottom of heat sink structure 105 becomes adhered to the top surface of the encapsulant as the encapsulant cures.

[46] Molding with a release film is well known to those of skill in the art; therefore, a detailed explanation is not provided. The only surface the release film that is in contact with the heat sink structure 105 is the portion above the top surface of the heat sink 105a and the other portion above the rail portion 105b that is clamped by the top mold portion 107. The mold release film prevents mold compound flash and ultimately prevents any contamination of the top surface. The mold compound is in contact with all the surfaces except the top surface of the heat sink 105a and the portion above the rail portion 105b that is clamped by the top mold portion 107. As compound cures it adheres to the contacting surfaces.

[47] After the molding process is finished, the mold is opened and the release film is automatically detached. Then a fresh film is propagated for next molding cycle.

[48] Heat sink structure 105 can also be laminated with a protected film 112, in lieu of a mold release film 106. See, for example, figure 7. After the encapsulation process, the protective film is removed.

[49] The top and bottom mold portions are then separated and the encapsulated package 110 is ejected from the mold. After the molding process, the strips undergo a ball mount process, where solder balls are attached on the solder pads of the substrate. Solder balls 108 are attached to the molded substrate 102 by conventional methods. See figure 8. The present invention is also applicable to packages that do not use solder balls, such as lead frame based packages like quad flat non leaded package (QFNs).

[50] Lead frame based packages usually undergo a plating process after molding and prior to singulation.

[51] The molded package 110 is then cut to size by sawing. For example, a singulation blade 109 can be used to dice the desired area. See figure 9. Because the molded package 110 is cut through the down-set 105c and not at the edge of the heat sink 105a, a notch 114 filled with the encapsulant is at the corner of the package. The filled notch at the top corner acts as an interlock for the heat sink, enhancing the holding strength between the heat sink and cured encapsulant.

[52] Figure 10 shows a final semiconductor package 111.

[53] Another embodiment of the present invention includes an integrated heat sink structure. Figure 11 is a cross-sectional view of the integrated heat sink structure. It consists of ring structure 201. The heat sinks 203 are encompassed within the heat sink structure and are connected to the ring structure 201 through half etched tie bars 202. "V" shaped down-sets 204 are created on the ring structure 201. At least one aspect of the innovativeness of the integrated

heat sink is the ability of single feature to have multiple functions. The ring structure 201, apart from carrying the heat sinks, also helps to prevention mold flash by being a barrier to the mold compound flow. Ring structure 201 also includes "V" shaped down-sets 204. The "V" shaped down-sets 204, support the ring structure 201. They also act as connecting links to the frame carrier 200. The "V" shaped down-sets 204 also translate drag force associated with mold compound flow into a vertical force cushioning the heat sink against release film 206 (shown on figure 12).

[54] Figure 12 shows the molding process with integrated heat sinks 203. The molding process is essentially the same as the previous embodiment. The heat sink frame carrier 200 carrying the integrated heat sinks is aligned and loaded on top of the substrate 208. The substrate and heat sink frame carrier 200 may make use of a locating pin 207 on the mold tooling for alignment purposes. Prior to the mold being enclosed, a vacuum may be used to force the mold release film 206 against the top mold portion. See for example, figure 18. Other methods may be used to insert the mold release film between the heat sink structure and top mold portion. As mold is closed, the "V" shaped down sets 204 provide a cushioning effect and keep the heat sinks 203 engaged at all times with the release film 206. During the molding process as the mold compound enters the mold cavity, the flow first hits the ring structure 201 and the "V" shaped down sets 204. The flow induced force on the "V" shaped down-sets 204 creates a lifting force (based on the orientation of the heat sink structure shown in Figure 12), keeping the ring structure 201 and heat sinks 203 always engaged with the release film 206. The ring structure 201 also helps in inhibiting mold flash on the heat sinks 110, by absorbing most of the flow induced forces.

[55] Figure 13 shows a top view of 2x2 array of heat sinks 203. Figure 14 shows a top view of a 3x3 array of heat sinks 203. A common feature of these two array structures is a ring structure 201, encompassing the heat sinks 203. Another advantage of having the ring structure 201 is having only a one time tooling cost on the down-set 204 creations. Irrespective of the array

types of heat sinks 203, 2x2, 3x3 or any array size, each mold cavity size can have only a one time down-set tooling cost. This also helps in standardizing the tooling and processes involved.

[56] Figures 18 and 19 show cross-sectional views of 2x2 and 3x3 array heat sinks. The figures also show one example of the molding concept of 2x2 and 3x3 array heat sinks.

[57] Figure 15 shows a partial plan view of heat sink frame carrier 200, connected to the ring structure 201 through the down-sets 204. The down-sets 204, apart from supporting the heat sinks, provide a vertical cushioning effect during molding. The down-sets 204 also act as connectors to the frame carrier 200. The heat sink carrier frame 200 includes alignment features 210 that are used to locate and align the heat sink strip and the substrate 208 (shown in figure 12) during molding process. Figure 15 also shows an embodiment of a heat sink frame carrier that includes a plurality of heat sink arrays.

[58] Figure 16 shows a flash free molded package with heat sink 203 exposed. After molding, the solder balls 108 are mounted on the package and package singulated along package edge 212 through the tie bars 202. Because the molded package is cut through the tie bars 202 and not at the edge of the heat sink 203, a notch 214 filled with the encapsulant is at the corner of the package. The filled notch at the top corner acts as an interlock for the heat sink, enhancing the holding strength between the heat sink and cured encapsulant. Lead frame based packages do not undergo a solder ball mount process. Rather, lead frame based packages after molding will undergo a plating process prior to singulation. Singulation is done with saw blade 211. Both the ball mount and singulation processes are standard processes know to those of skill in the art in the industry.

[59] Figure 17 shows a complete assembled thermally enhanced semiconductor package with embedded heat sink 203. With the substrate 100 being an insulator, the heat sink 203 greatly enhances the performance of the package by removing the heat generated from the chip 101 and

keeping the junction temperatures low. The integrated heat sink design and the proposed method enable a cost effective way of mass producing thermally enhanced semiconductor package.

[60] Other packages to which the integrated heat sink can be applied to enhance the thermal performance include QFN and MCM packages. QFN packages, like laminate based packages, are molded on one side. Figures 20 and 21 below show an example of the assembly concept of a QFN package with an integrated heat sink.

[61] Most of the QFN lead-frames 210 shown in figure 21 have high temperature tape 211 at the bottom of the strip to prevent any mold compound flash. After molding, the high temperature tape is de-taped, the molded strips are plated, then sawed. So for high thermal performance an integrated heat sink is dropped in the mold prior to molding. Figure 19 shows a QFN frame 210, being loaded on to the bottom mold chase surface 212. The mold chase surface 212, has a relief slot for the high temperature tape 211 of the lead frame 210. The lead frame is located using the locating pin 213. The same locating pin 213 is also used to locate the heat sink during molding. Other known alignment methods may also be used.

[62] It should be emphasized that the above-described embodiments of the present invention are merely possible examples of implementations, merely set forth for a clear understanding of the principles of the invention. Many variations and modifications may be made to the above-described embodiment(s) of the invention without departing substantially from the spirit and principles of the invention. All such modifications and variations are intended to be included herein within the scope of this disclosure and the present invention and protected by the following claims.

WHAT IS CLAIMED IS:

1. A method of manufacturing a semiconductor package comprising:

inserting a substrate with an attached semiconductor chip in a first mold portion;

placing a heat sink structure on top of a portion of the substrate;

placing a mold release film onto a second mold portion;

clamping the second mold portion onto a portion of the heat sink structure;

injecting an encapsulant into a mold cavity formed by the first and second mold portions, wherein the encapsulant surrounds portions of the substrate, semiconductor chip and heat sink structure;

curing the encapsulant, whereby the heat sink structure adheres to the encapsulant;

removing the encapsulated assembly from the mold;

singulating the encapsulated assembly to form a semiconductor package.

2. The method of claim 1 wherein a vacuum is used to force the mold release film onto the second mold portion.

3. The method of claim 1 wherein the substrate with attached semiconductor chip and heat sink structure are aligning in the first mold portion.

4. The method of claim 3 wherein the substrate and heat sink structure are aligned through the use of guide pins.

5. The method of claim 1 wherein the heat sink structure comprises a ring structure and a heat sink.

6. The method of claim 5 wherein the heat sink is connected to the ring structure by etched tie bars.

7. The method of claim 6 wherein the encapsulated package is singulated through an etched tie bar.

8. The method of claim 1 wherein the heat sink structure comprises down sets.

9. The method of claim 8 wherein said down sets comprise slanted elements.

10. The method of claim 8 wherein said down sets are V-shaped.

11. The method of claim 8 wherein said down sets create a lifting force when the encapsulant is injected in the mold cavity.

12. The method of claim 8 wherein the encapsulated package is singulated through a down-set.

13. The method of claim 1 wherein heat sink structure comprises down sets that provide a cushioning effect and keep a heat sink on said heat sink structure engaged with said mold release film while said encapsulant is being injected in to the mold cavity.

14. The method of claim 1 wherein said substrate has a plurality of attached semiconductor chips.

15. The method of claim 1 wherein the heat sink structure comprises a ring structure with a plurality of heat sinks.

16. The method of claim 15 wherein the plurality of heat sinks are arranged in an array.

17. The method of claim 16 wherein the heat sink structure comprising a plurality of heat sink arrays.

18. The method of claim 1 wherein the semiconductor package is a ball grid array package.

19. The method of claim 1 wherein the semiconductor package is a quad flat nonleaded package.

20. The method of claim 1 wherein the semiconductor package is a multi chip module package.

21. The method of claim 1 further comprising attaching a high temperature tape on a bottom portion of the substrate.

22. The method of claim 21 wherein the high temperature tape fits into a relief slot in the first mold portion.

23. The method of claim 1 further comprising attaching solder balls to the substrate.

24. A semiconductor package comprising:

a semiconductor chip attached to a substrate;

an encapsulant covering portions of the semiconductor chip and substrate and comprising a top surface; and

a heat sink in direct contact with the entire top surface of the encapsulant;

wherein the heat sink becomes adhered to the top surface of the encapsulant as the encapsulant cures;

wherein a notch at a top corner of semiconductor package is filled with the encapsulant' and

wherein notch acts as an interlock for the heat sink.

25. The package of claim 24, wherein said notch is defined by a side of the heat sink and a down-set.

26. The package of claim 24, wherein said notch is defined by a side of the heat sink and a tie bar.

27. The package of claim 24, further comprising solder balls connected to the substrate.

28. The package of claim 24, wherein the semiconductor chip is wire bonded to the substrate.

29. The package of claim 24, wherein the substrate is a laminate structure.

30. The package of claim 24, wherein the substrate is a metal lead-frame structure.

31. The package of claim 24, wherein the semiconductor package is a ball grid array package.

32. The package of claim 24, wherein the semiconductor package is a quad flat nonleaded package.

33. The package of claim 24, wherein the semiconductor package is a multi chip module package.