CLAIMS

What is claimed is:

1. A method for fabricating an SRAM integrated circuit (IC), comprising:

depositing photoresist on a first oxide layer overlying a silicon substrate;

forming a pattern of locations, using said photoresist, for the formation of two pull up transistors, two pull down transistors, and two pass gate transistors on said oxide layer;

anisotropically etching U-shaped channels in said oxide layer corresponding to said pattern;

isotropically etching U-shaped channels in said silicon layer to form saddle-shaped fins in the silicon;

depositing a second oxide layer over said saddle-shaped fins; and

depositing a first metal layer on said second oxide layer.

2. The method of claim 1, further comprising:

forming gate electrodes and local interconnections coupling one of the pull up transistors and one of the pull down transistors to a node between the other of the pull up transistors and pull down transistors and to a source/drain of one of the pass gate transistors.

3. The method of claim 1, wherein depositing photoresist comprises depositing said photoresist over both an active area and a logic area of said SRAM IC.

4. The method of claim 1 further comprising photolithographically patterning said photoresist.

5. The method of claim 1, further comprising removing said photoresist from said active region prior to said anisotropic etching.

6. The method of claim 1, wherein said anisotropic etching comprises STI recess etching of said first oxide layer.

7. The method of claim 1, further comprising forming both n-FET and p-FET transistors.

8. The method of claim 7, wherein said method comprises forming a low leakage SRAM.

9. The method of claim 8, wherein depositing said first metal layer comprises depositing a single metal species.

10. The method of claim 7, wherein said method comprises forming a high performance SRAM.

11. The method of claim 10, wherein depositing said first metal layer comprises depositing two separate metal work functions.

12. A method of claim 1, further comprising:

forming replacement gates in the logic region of said SRAM IC; and

forming FET caps in the active area of said SRAM IC.

13. The method of claim 1, further comprising forming a contact metal layer over said pull up transistors, said pull down transistors, and said pass gate transistors.

14. The method of claim 13, further comprising;

planarizing said contact metal layer to form: gate electrodes; source/drain contacts; contacts to nodes that couple the pass gate transistors, common nodes between pull up and pull down transistors, and cross coupled gate electrodes; and contacts for coupling the pull up transistors to a first potential node and the pull down transistors to a second potential node.

15. The method of claim 14, wherein said first potential node corresponds to V_{DD}, and said second potential node corresponds to V_{SS}.

16. The method of claim 13, further comprising depositing a barrier layer over said transistors prior to depositing said metal contact layer.

17. The method of claim 16, wherein depositing said barrier layer comprises depositing titanium nitride, and depositing said metal contact layer comprises depositing tungsten.

18. An SRAM cell made by the method of claim 1.

19. An SRAM integrated circuit comprising:

two buried pull up FINFET transistors;

two buried pull down FINFET transistors;

two buried pass gate FINFET transistors;

a first cross couple contact configured to electrically interconnect a first one of said pull up transistors, a first one of said pull down transistors, and a first one of said pass gate transistors; and

a second cross couple contact configured to electrically interconnect a second one of said pull up transistors, a second one of said pull down transistors, and a second one of said pass gate transistors;

wherein each of said buried FINFET transistors are U-shaped.

20. The SRAM IC of claim 19, wherein each of said U-shaped FINFET transistors are saddle shaped.

CLAIMS

1. A method for fabricating an SRAM integrated circuit (IC), comprising:

depositing photoresist on a first oxide layer overlying a silicon substrate;

forming a pattern of locations, using said photoresist, for the formation of two pull up transistors, two pull down transistors, and two pass gate transistors on said first oxide layer;

anisotropically etching U-shaped channels in said first oxide layer corresponding to said pattern;

isotropically etching U-shaped channels in said silicon substrate to form saddle-shaped fins in the silicon; depositing a second oxide layer over said saddle-shaped fins; and

depositing a first metal layer on said second oxide layer.

2. The method of claim 1, further comprising:

forming gate electrodes and local interconnections coupling one of the pull up transistors and one of the pull down transistors to a node between the other of the pull up transistors and pull down transistors and to a source/drain of one of the pass gate transistors.

3. The method of claim 1, wherein depositing photoresist comprises depositing said photoresist over both an active area and a logic area of said SRAM IC.

4. The method of claim 1 further comprising photolithographically patterning said photoresist.

5. The method of claim 1, further comprising removing said photoresist from said active region prior to said anisotropic etching.

6. The method of claim 1, wherein said anisotropic etching comprises STI recess etching of said first oxide layer.

7. The method of claim 1, further comprising forming both n-FET and p-FET transistors.

8. The method of claim 7, wherein said method comprises forming a low leakage SRAM.

9. The method of claim 8, wherein depositing said first metal layer comprises depositing a single metal species.

10. The method of claim 7, wherein said method comprises forming a high performance SRAM.

11. The method of claim 10, wherein depositing said first metal layer comprises depositing two separate metal work functions.

12. A method of claim 1, further comprising: forming replacement gates in the logic region of said SRAM IC; and forming FET caps in the active area of said SRAM IC.

13. The method of claim 1, further comprising forming a contact metal layer over said pull up transistors, said pull down transistors, and said pass gate transistors.

14. A method for fabricating an SRAM integrated circuit (IC), comprising:

depositing photoresist on a first oxide layer overlying a silicon substrate;

forming a pattern of locations, using said photoresist, for the formation of two pull up transistors, two pull down transistors, and two pass gate transistors on said oxide layer;

anisotropically etching U-shaped channels in said oxide layer corresponding to said pattern;

isotropically etching U-shaped channels in said silicon layer to form saddle-shaped fins in the silicon; depositing a second oxide layer over said saddle-shaped fins;

depositing a first metal layer on said second oxide layer;

forming a contact metal layer over said pull up transistors, said pull down transistors, and said pass gate transistors; and

planarizing said contact metal layer to form: gate electrodes; source/drain contacts; contacts to nodes that couple the pass gate transistors, common nodes between pull up and pull down transistors, and cross coupled gate electrodes; and contacts for coupling the pull up transistors to a first potential node and the pull down transistors to a second potential node.

15. The method of claim 14, wherein said first potential node corresponds to V_{DD}, and said second potential node corresponds to V_{SS}.

16. The method of claim 14, further comprising depositing a barrier layer over said transistors prior to depositing said metal contact layer.

17. The method of claim 16, wherein depositing said barrier layer comprises depositing titanium nitride, and depositing said metal contact layer comprises depositing tungsten.

18. An SRAM cell made by the method of claim 14.

19. An integrated circuit (IC) fabricated in accordance with any one of claims 1-17.