

PATENT SPECIFICATION

(11) 1 247 892

DRAWINGS ATTACHED



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- (21) Application No. 45991/68 (22) Filed 27 Sept. 1968
(31) Convention Application No. 675 819 (32) Filed 17 Oct. 1967 in
(33) United States of America (US)
(45) Complete Specification published 29 Sept. 1971
(51) International Classification H 01 I 11/14
(52) Index at acceptance

H1K 217 223 22Y 235 312 413 415 41Y 422 42X 472 474
482 507 51Y 581

(54) SEMICONDUCTOR MEMORY DEVICE

(71) We, R.C.A. CORPORATION, formerly known as Radio Corporation of America, a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor memory devices and more particularly to a semiconductor device in which charge storage is employed to modify its electrical characteristics.

According to the invention the semiconductor device includes a body of semiconductive material of given conductivity type having a surface, said body including a structure having a controllable electrical characteristic responsive to electrical charge outside said body in the vicinity of said surface, a first layer of insulating material on said surface, and means for applying an electrical field across said insulating material, said first layer having a thickness not exceeding 25Å which thickness is less than the tunneling distance for charge carriers from said body under the influence of a predetermined electrical field in said first layer, and a second layer of material including means for confining charge carriers therewithin. Two states of the device are represented by the presence or absence of charge in the second layer, and may be sensed by measuring an electrical characteristic of the semiconductor device. Only one device per bit of information to be stored is required. The decay rate of the stored information is sufficiently long for most memory applications and the switching speeds are good.

Figure 1 is a cross sectional view of one embodiment of the present memory device;

Figure 2 is a cross sectional view of another embodiment of this device;

Figure 3 is a cross sectional view through a third embodiment of this device;

Figure 4 is a plot of capacitance against applied voltage, illustrating the bistable character of each of these embodiments;

Figures 5 to 9 are energy level diagrams illustrating the manner in which the present devices are believed to operate; and

Figure 10 is a circuit diagram showing one suitable memory circuit in which the devices of Figures 1 and 2 are useful.

One embodiment of the present memory device is an enhancement type insulated gate field-effect transistor 10, as shown in Figure 1. The transistor 10 includes a body 12 of semiconductive material of given conductivity type, such as P type silicon, which has an upper surface 14. Adjacent to the surface 14 are spaced regions 15 and 16 of conductivity type opposite to that of the body 12, which constitute source and drain regions, respectively, for the transistor 10. Contacts 18 and 20 are formed on the surface 14 in ohmic contact with the regions 15 and 16.

Overlying the channel space between the regions 15 and 16 is a structure which comprises the gate and charge storing elements of the transistor 10. The first layer adjacent to the surface 14 in the space between the regions 15 and 16 is a thin layer 22 of insulating material, such as silicon dioxide, which has a thickness less than the tunneling distance for charge carriers from the body 12 under the influence of an electric field of predetermined strength across the layer 22 in the direction normal to the surface 14. For field strengths which can be achieved at efficient voltage levels, the layer 22 should not exceed 25Å in thickness.

Disposed on the layer 22 is a layer 24 of a material which can accept charge carriers which tunnel through the layer 22 and confine them to localized sites adjacent the interface between the layers 22 and 24. In this example, the layer 24 is a layer of silicon nitride, which is itself

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an insulator. On the silicon nitride layer 24 is a metallic electrode 26 adapted to establish an electric field across the layers 24 and 22. Leads 28, 30, and 32, schematically shown, serve to connect the electrodes 18, 26 and 20 to external circuitry.

The transistor 10 may be fabricated by known techniques. For example, the source and drain regions 15 and 16 may be formed by selectively masking the surface 14 and diffusing conductivity modifying substances through spaced portions of the surface 14 into the body 12. The silicon dioxide layer may be formed by thermally oxidizing the surface of the body 12 or by the pyrolytic decomposition of an organic siloxane compound such as tetraethoxysilane on the surface 14. The silicon nitride layer may be deposited by heating the body 12 in an atmosphere of silane, SiH_4 , and ammonia.

In the operation of the transistor 10, the application of a negative pulse of about 1 msec. duration to the gate electrode 26, relative to the source region 15, sets the device to one of its two states by storing positive charge in the layer 24. This charge remains after the termination of the pulse and acts to lower the threshold voltage of the transistor 10. A positive pulse of about 1 $\mu\text{sec.}$ duration on the gate electrode 26 will set the device to the other of its states by removing the stored positive charge and thereby increasing the threshold voltage of the transistor 10. The mechanism by which this transfer of charge is believed to take place will be explained below.

Another embodiment of the present memory device is a transistor, generally indicated by the numeral 40 in Figure 2, which is similar to the transistor 10 in that it is an enhancement type field-effect transistor. The transistor 40 includes a body 42 of P type conductivity which has a surface 44. Source and drain regions 45 and 46 are at spaced locations adjacent to the surface 44.

The transistor 40 differs from the transistor 10 in the construction of the gating structure. The transistor 40 employs a thin layer 52 of insulating material such as silicon dioxide which is similar to the layer 22 of the transistor 10. A metallic layer 54, which can accept and confine charge carriers which tunnel from the body 42, is deposited on the insulating layer 52. The metallic layer 54 may be conductive or semiconductive, and may be, for example, a deposited layer of polycrystalline silicon. A thin layer 56 of insulating silicon dioxide is disposed on the layer 54 and a metallic electrode 57 overlies the silicon dioxide layer 56.

The transistor 40 operates in substantially the same manner as the transistor 10.

In Figure 3, a third embodiment of the present device is illustrated as a diode 60 the electrical characteristics of which can be modified by charge storage elements similar to those described above. The diode 60 has a body 62 of semiconductive material which has a major surface 64. A region 65 of conductivity type opposite to that of the body 62 defines a PN junction 66, the peripheral boundary of which intersects the surface 64. Contacts 68 and 70 are provided in ohmic contact with the body 62 and the region 65, respectively.

Overlying the boundary of the junction 66 is an annular gating structure which is in cross section, in this example, similar to the gating structure of the transistor 10. In particular, there is a thin layer of insulating material 72, such as silicon dioxide, a layer 74 of charge storing material such as silicon nitride, and a gate electrode 76. The gating structure of the diode 60 may also be made like that of the transistor 40.

In the operation of the diode 60, storage of charge in or removal of charge from the layer 74 will vary the electrical characteristics of the device in a controllable manner. For example, the reverse breakdown voltage or the capacitance of the diode 60 can be shifted between two values.

In general, the memory action of any of the embodiments of the present device can be demonstrated by measuring the capacitance of the parallel plate system constituted by the gate electrode and the semiconductor as the plates thereof and the insulating and charge storing layers as the dielectric thereof. When the gate potential is varied, this capacitance changes in the manner illustrated in Figure 4, i.e., with a pronounced hysteresis loop. If the applied voltage is made sufficiently negative, the capacitance will switch to the higher state and will remain in that state after the removal of the negative voltage pulse. If the gate is made sufficiently positive, the capacitance is switched to the lower condition.

It is believed that charge enters and leaves the charge storing layers 24, 54, and 74 of the three devices described above by tunneling through the insulating layer which is adjacent to the semiconductor. The charge may be retained within the gate structure by traps (slow surface states) located in the material of the charge storing layers adjacent to the silicon dioxide interface.

Figures 5 to 9 illustrate the operation of the transistor 10. Figure 5 shows the energy band situation in the transistor 10 with no voltage applied to the gate electrode 26 thereof. The traps under consideration are suggested by the small squares which lie in the silicon nitride layer near its interface

with the silicon dioxide layer and just below the Fermi level, which is indicated by the dashed line E_t .

Figure 6 shows the effect of an applied negative voltage which is large enough to raise the traps under consideration to a level at or near the level of the conduction band edge in the silicon. Under these conditions, electrons can leave the traps by tunneling to the conduction band of the silicon, provided that the silicon dioxide layer is not so thick as to eliminate the probability of tunneling. After the electrons leave the traps, the traps remain positively charged. Traps further within the silicon nitride layer, even though they may be raised to energy levels much higher than the conduction band edge in the silicon, do not contribute to this charge transfer because the probability of tunneling decreases very rapidly with distance. Traps much below the Fermi level need not be considered because they are not elevated enough by the applied voltage. Traps above the Fermi level would be permanently charged and therefore could not contribute electrons to the silicon.

Figure 7 illustrates the situation after removal of the pulse applied in Figure 6. The traps remain in the silicon nitride layer in a positively charged state, and attract electrons to the surface of the silicon by the field effect. The threshold voltage of the device is consequently reduced because a lower positive voltage can now turn the device "on".

The result of a positive pulse is illustrated in Figures 8 and 9. Here, electrons can tunnel from the conduction band in the silicon into the conduction band of the nitride and subsequently recombine with the traps to neutralize them. When the positive voltage on the gate is relaxed, the transistor has been returned to the state of higher threshold voltage as suggested in Figure 9.

The present device may be used in a memory circuit such as the circuit 80 illustrated in Figure 10. The circuit 80 is a coincident voltage memory employing an enhancement type field-effect transistor such as that illustrated in either Figure 1 or Figure 2 as the memory element thereof. A typical circuit may include as many as 64 by 64 elements but, for convenience, only four elements are illustrated in Figure 10.

The circuit 80 includes a plurality of row conductors 81 and a plurality of column conductors 82 which are employed to select a particular element and to write the desired information into the element. Row conductors 84 provide gate voltage for the memory transistors and conductors 85

and 86 are employed to read the stored information.

One element of the circuit 80 is illustrated at 88 within the dotted box. The element 88 includes a transistor 90, which is a conventional N channel enhancement type insulated gate field-effect transistor, used as a selecting switch, and a transistor 92, which is an N channel enhancement type memory unit such as the transistor 10 or the transistor 40. The transistors 90 and 92 are connected in series between a row conductor 81 and an output row conductor 85, as shown. The gate of the transistor 90 is connected to a column conductor 82. The gate of the transistor 92 is connected to a row conductor 84. A resistor is connected between the row conductors 85 and 86 and the output voltage from the element 88 is measured on terminals 96 and 98, on the conductors 85 and 86 respectively.

In the operation of the memory, logical "1" is stored in the transistor 92 when charge is present in the gate structure thereof. Logical "0" is stored when no charge is present. When the memory is quiescent, the various conductors are biased at the following voltages. The column conductor 82 is biased at -2 volts; the row conductor 81 is at +10 volts; the row conductor 84 is at +8 volts; and the row conductor 86 is at +10 volts. The row conductor 85 is unconnected. Under these conditions, both the transistors 90 and 92 are "off" because the voltage on their gates is low with respect to the voltage on their respective source electrodes. The gate structure of the memory transistor 92 may contain charge or not, depending on the previous history of the transistor.

To write a "0" into the element 88, the following voltages are applied. The column conductor 82 is set at -7 volts; and the voltage on the row conductor 81 is set at -12 volts. The row conductor 84 remains biased at +8 volts; the row conductor 86 remains at +10 volts; and the row conductor 85 remains unconnected. Under these voltage conditions, the gate of the transistor 90 is at a voltage which is 5 volts higher than the voltage on the source electrode thereof. This enhances the transistor 90 above the threshold thereof and therefore puts it in its conductive "on" state. As a result, the source of the transistor 92 is effectively connected to the conductor 81 and is at a voltage approximately equal to the -12 volts on the conductor 81. Since the gate of the transistor 92 is still at +8 volts, a much higher voltage, an energy situation such as that illustrated in Figure 8 will exist, so that if charge is present in the gate structure of the transistor 92, it will be neutralized. If no

charge is present, no change is produced. When the quiescent voltages are restored, the element 88 will remain with no charge in the gate structure of the transistor 92, and will therefore store logical "0".

To write a "1" into the element 88, a voltage of +33 volts is applied to the column conductor 82. A voltage of +28 volts is applied to the row conductor 81 and the other row conductors remain at their previous voltages. Under these conditions, the transistor 90 is again on its "on" condition because the voltage on its gate is 5 volts higher than that on its source electrode and, consequently, the voltage on the source electrode of the transistor 92 is approximately at the +28 volt level. Since the gate of the transistor 92 is still at +8 volts, it is now 20 volts more negative than the source and the energy situation of Figure 6 is established. Accordingly, positive charge will be introduced into the gate structure and a logical "1" is stored.

To read the memory, the following voltages are established on the several conductors. The column conductor 82 has +7 volts applied thereto. The row conductor 81 is set at +5 volts and the row conductor 84 is set at +12 volts. The row conductor 86 remains at +10 volts. Under these conditions, the transistor 90 is again "on" because its gate voltage is higher than its source voltage. The transistor 92 will have a voltage somewhere between 5 and 10 volts on its source electrode, depending on the channel conductance of the transistor 90, and will be in the "on" condition because of the relatively high voltage (+12 volts) now on its gate. Current will therefore flow through the resistor 94 in an amount which will depend on the channel conductances of the transistor 90 and of the memory transistor 92, which in turn depends on whether or not charge has been stored in the gate structure of the transistor 92. If charge has been stored, the conductance will be higher, more current will flow, and the voltage as measured across the resistor 94 will therefore be relatively high, indicating the logical "1" condition. If no charge is present, the conductance of the transistor 92 will be lower resulting in the flow of less current through the resistor 94 and a lower voltage as measured across the resistor 94, indicating the logical "0" condition.

The element 88 is read non-destructively because the voltage conditions during the read cycle are not sufficient to alter the stored charge. Accordingly, the memory can be read repeatedly without loss of its stored information. The stored charge will remain even if the quiescent voltages are removed, i.e., even if the power supply to the memory fails.

Similar circuitry can be designed for the diode 60. For this device, the reading circuitry should be adapted to measure the reverse breakdown characteristic of the diode 60 or the capacitance of its junction 66. The selection circuitry may be the same as that of Figure 10.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising: a body of semiconductive material of given conductivity type having a surface, said body including a structure having a controllable electrical characteristic responsive to electrical charge outside said body in the vicinity of said surface, a first layer of insulating material on said surface, and means for applying an electric field across said insulating material, said first layer having a thickness not exceeding 25Å which thickness is less than the tunneling distance for charge carriers from said body under the influence of a predetermined electric field in said first layer, and a second layer of material including means for confining charge carriers therewith.
2. A semiconductor device as defined in claim 1 wherein said semiconductive material is silicon, said first layer is silicon dioxide and said second layer is silicon nitride.
3. A semiconductor device as defined in claim 1 wherein said semiconductive material is silicon, said first layer is silicon dioxide and said second layer is silicon.
4. A semiconductor device as defined in claim 3 wherein said electric field applying means comprises a third layer, of insulating material, on said second layer and a metallic electrode on said third layer.
5. A field-effect semiconductor device according to claim 1 further including a source region and a drain region in said body at spaced locations adjacent to said surface.
6. A field-effect semiconductor device as defined in claim 5 wherein said semiconductive material is silicon, said first layer is silicon dioxide, and said second layer is silicon nitride.
7. A field-effect semiconductor device as defined in claim 5 wherein said semiconductive material is silicon, said first layer is silicon dioxide, and said second layer is silicon.
8. A field-effect semiconductor device as defined in claim 7 wherein said electric field applying means includes a third layer, of insulating material, on said second layer and a metallic electrode on said third layer.
9. A semiconductor device according to claim 1 further characterized by a region of conductivity type opposite to that of said body in said body adjacent to a portion of said surface, whereby a PN junction

charge is present, no change is produced. When the quiescent voltages are restored, the element 88 will remain with no charge in the gate structure of the transistor 92, and will therefore store logical "0".

To write a "1" into the element 88, a voltage of +33 volts is applied to the column conductor 82. A voltage of +28 volts is applied to the row conductor 81 and the other row conductors remain at their previous voltages. Under these conditions, the transistor 90 is again on its "on" condition because the voltage on its gate is 5 volts higher than that on its source electrode and, consequently, the voltage on the source electrode of the transistor 92 is approximately at the +28 volt level. Since the gate of the transistor 92 is still at +8 volts, it is now 20 volts more negative than the source and the energy situation of Figure 6 is established. Accordingly, positive charge will be introduced into the gate structure and a logical "1" is stored.

To read the memory, the following voltages are established on the several conductors. The column conductor 82 has +7 volts applied thereto. The row conductor 81 is set at +5 volts and the row conductor 84 is set at +12 volts. The row conductor 86 remains at +10 volts. Under these conditions, the transistor 90 is again "on" because its gate voltage is higher than its source voltage. The transistor 92 will have a voltage somewhere between 5 and 10 volts on its source electrode, depending on the channel conductance of the transistor 90, and will be in the "on" condition because of the relatively high voltage (+12 volts) now on its gate. Current will therefore flow through the resistor 94 in an amount which will depend on the channel conductances of the transistor 90 and of the memory transistor 92, which in turn depends on whether or not charge has been stored in the gate structure of the transistor 92. If charge has been stored, the conductance will be higher, more current will flow, and the voltage as measured across the resistor 94 will therefore be relatively high, indicating the logical "1" condition. If no charge is present, the conductance of the transistor 92 will be lower resulting in the flow of less current through the resistor 94 and a lower voltage as measured across the resistor 94, indicating the logical "0" condition.

The element 88 is read non-destructively because the voltage conditions during the read cycle are not sufficient to alter the stored charge. Accordingly, the memory can be read repeatedly without loss of its stored information. The stored charge will remain even if the quiescent voltages are removed, i.e., even if the power supply to the memory fails.

Similar circuitry can be designed for the diode 60. For this device, the reading circuitry should be adapted to measure the reverse breakdown characteristic of the diode 60 or the capacitance of its junction 66. The selection circuitry may be the same as that of Figure 10.

WHAT WE CLAIM IS:—

1. A semiconductor device comprising: a body of semiconductive material of given conductivity type having a surface, said body including a structure having a controllable electrical characteristic responsive to electrical charge outside said body in the vicinity of said surface, a first layer of insulating material on said surface, and means for applying an electric field across said insulating material, said first layer having a thickness not exceeding 25Å which thickness is less than the tunneling distance for charge carriers from said body under the influence of a predetermined electric field in said first layer, and a second layer of material including means for confining charge carriers therewith.
2. A semiconductor device as defined in claim 1 wherein said semiconductive material is silicon, said first layer is silicon dioxide and said second layer is silicon nitride.
3. A semiconductor device as defined in claim 1 wherein said semiconductive material is silicon, said first layer is silicon dioxide and said second layer is silicon.
4. A semiconductor device as defined in claim 3 wherein said electric field applying means comprises a third layer, of insulating material, on said second layer and a metallic electrode on said third layer.
5. A field-effect semiconductor device according to claim 1 further including a source region and a drain region in said body at spaced locations adjacent to said surface.
6. A field-effect semiconductor device as defined in claim 5 wherein said semiconductive material is silicon, said first layer is silicon dioxide, and said second layer is silicon nitride.
7. A field-effect semiconductor device as defined in claim 5 wherein said semiconductive material is silicon, said first layer is silicon dioxide, and said second layer is silicon.
8. A field-effect semiconductor device as defined in claim 7 wherein said electric field applying means includes a third layer, of insulating material, on said second layer and a metallic electrode on said third layer.
9. A semiconductor device according to claim 1 further characterized by a region of conductivity type opposite to that of said body in said body adjacent to a portion of said surface, whereby a PN junction



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which terminates in said surface is formed, said first layer being in overlying relation to the termination of said junction.

5 10. A semiconductor device as defined in claim 9 wherein said semiconductor material is silicon, said first layer is silicon dioxide, and said second layer is silicon nitride.

10 11. A semiconductor device as defined in claim 9 wherein said semiconductor material is silicon, said first layer is silicon dioxide, and said second layer is silicon.

12. A semiconductor device as defined in claim 11 wherein said electric field applying means comprises a third layer, of insulating material, on said second layer, and a metallic electrode on said third layer. 15

For the Applicants:
MATTHEWS, HADDAN & CO.,
Haddan House,
33 Elmfield Road,
Bromley, Kent. BR1 1SU.

Printed for Her Majesty's Stationery Office by Burgess & Son (Abingdon), Ltd.—1971.
Published at The Patent Office, 25 Southampton Buildings, London, WC2A 1AY,
from which copies may be obtained.

