TITLE:

VERTICAL THIN FILM TRANSISTOR AND MANUFACTURING METHOD THEREOF

ABSTRACT

A vertical thin film transistor includes first, second, and third semiconductor layers, a sacrificed layer, a first gate, source, and drain electrodes. The first semiconductor layer is disposed on a substrate and has first heavily doped and extension portions. The sacrificed layer covers the extension portion and exposes the first heavily doped portion. The second semiconductor layer is disposed on the sacrificed layer and has a second heavily doped portion. The third semiconductor layer covers and is in contact with portions of the first and second heavily doped portions and a sidewall of the sacrificed layer. In a direction perpendicular to the substrate, the second heavily doped portion is overlapped with the extension portion, the first gate electrode is overlapped with the second heavily doped and extension portions and the third semiconductor layer. The source and drain electrodes are electrically connected to the first and second heavily doped portions, respectively.

FIG. 1