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COMPLETE SPECIFICATION

Memory Storage Unit employing Insulated Gate Field Effect Transistors

We, RADIO CORPORATION OF AMERICA, a Corporation organized under the laws of the State of Delaware, United States of America; of 30, Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to memory storage units employing field effect transistors.

According to one aspect, the present invention provides a memory storage unit comprising a plurality of field effect transistors each having a source and a drain defining the ends of a conduction path, and an insulated gate: first, third and sixth ones of said transistors being of one conductivity type and second, fourth and fifth ones of said transistors being of the opposite conductivity type: said first and second transistors having their conduction paths serially connected in a first branch circuit with their drains connected together: said third and fourth transistors having their conduction paths serially connected in a second branch circuit with their drains connected together: a connection between the gates of the first and second transistors: a connection between the gates of the third and fourth transistors: a connection between the drains of the first and second transistors to a point common to the gates of the third and fourth transistors: the fifth transistor having its conduction path connected between a point common to the drains of the third and fourth transistors and a point common to the gates of the first and second transistors: a first input terminal: the sixth transistor having its conduction path connected between said

first input terminal and the gates of the first and second transistors: and a second input terminal connected to the gates of said fifth and sixth transistors.

According to another aspect, the present invention provides a memory comprising: a plurality of groups of memory elements, each memory element including: an insulated gate field effect transistor bistable circuit having an input point, and an insulated gate field effect input transistor having a drain connected to the input point, a source and a gate: a like plurality of control lines, one for each of said groups of memory elements: a plurality of signal input lines: means connecting the gates of all input transistors in the same group to the control line associated with that group: and means connecting the source of each input transistor of said group to a different one of said signal input lines.

According to yet another aspect, the present invention provides a memory storage unit comprising first and second insulated gate field effect transistors each having a source, a drain and a gate, first and second circuit branches connected in parallel to each other and across a source of operating potential, the first branch including the source-drain path of the first transistor and a load connected in series therewith, the second branch including the source-drain of the second transistor and a load connected in series therewith, means cross-coupling the drains of the first and second transistors to the gates of the second and first transistors, respectively, in order to form a bistable circuit, and an input terminal: a third insulated gate field effect transistor having a source, a drain and a gate: means connecting the source-drain path of the third transistor between said input terminal and the gate of the first

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transistor, said input terminal and the gate of the first transistor, said input terminal being adapted to receive information signals from a source of input signals; with the gate of the third transistor being adapted to receive first control signals which are substantially concurrent with said information signals and which are effective to render said third transistor source-drain path conductive; where the source-drain path of the third transistor, in the absence of such a control signal is substantially non-conductive.

The invention will now be described with reference to the accompanying drawings, in the several Figures of which like reference numerals denote like components, and in which:

Figure 1 is a schematic diagram of a memory storage unit embodying the invention and suitable for use in a word-organized memory system;

FIGURE 2 is a set of voltage waveforms useful in describing the operations of the memory storage unit of FIGURE 1;

FIGURE 3 is a diagram of a word-organized memory, in elementary form, that may comprise a plurality of memory storage units of the type illustrated in FIGURE 1;

FIGURE 4 is a diagram, in elementary form, of a coincident voltage memory system that may comprise a plurality of the memory storage units of the type illustrated in FIGURE 5; and

FIGURE 5 is a schematic diagram of a coincident voltage memory storage unit embodying the invention.

Insulated gate field effect transistors have characteristics which render them useful in practicing the present invention.

Two known types of insulated gate field effect transistors are the thin-film transistor (TFT) and the metal-oxide semiconductor (MOS).

In the memory storage unit of FIGURE 1, a first insulated gate field effect transistor 10a of the n-type conductivity has its source 12a connected to a point of reference potential, indicated by the conventional symbol for circuit ground, and has its drain 14a connected directly to the drain 24a of a second insulated gate field effect transistor 20a of p-type conductivity. A junction point 44 is common to the drains 14a and 24a. The source 22a of second transistor 20a is connected to a junction point 29. A current responsive device 28, to be described, is connected between junction point 29 and the positive terminal of a source 30 of V volts operating potential, which may be, for example, a battery, having its negative terminal grounded. In a like manner, the conduction paths of a third insulated gate field effect transistor

10b of n-type conductivity and a fourth insulated gate field effect transistor 20b of p-type conductivity are serially connected in a separate circuit branch between circuit ground and the junction point 29, whereby the current responsive device 28 is connected in the supply line common to the two circuit branches.

The gates 16a, 26a of the first and second transistors 10a and 20a are connected directly together by negligible impedance means, i.e., means offering negligible impedance. The gates 16b, 26b of the third and fourth transistors 10b and 20b also are connected together by negligible impedance means and are cross-coupled by negligible impedance means to the drains 14a, 24a of the first and second transistors 10a and 20a. A fifth insulated gate field effect transistor 20c of p-type conductivity has its conduction path connected in the cross-coupling path between the drains 14b, 24b of the third and fourth transistors 10b and 20b and the gates 16a, 26a of the first and second transistors 10a and 20a.

A sixth insulated gate field effect transistor 10c of n-type conductivity has its conduction path connected between an input terminal 32 and a point common to the gates 16a, 26a of the first and second transistors. Input signals from a first input source 36, labelled "Digit Source," are applied between input terminal 32 and circuit ground. The gates 16c, 26c of the fifth and sixth transistors 20c and 10c are connected in common to a second input terminal 38, and signals from a second signal source 40, labelled "Word Source," are applied between second input terminal 38 and circuit ground. The signal sources 36 and 40 normally supply voltages of ground potential at the first and second input terminals 32, 38 respectively, and are individually and selectively operable to switch the voltages at those terminals to +V volts, the same value as the voltage provided by the bias source 30.

The conductivity (inverse of resistance) of the conduction path in an enhancement type insulated gate field effect transistor is low when the gate and source have the same value of voltage. The transistor then is biased "off," and only a small leakage current flows between source and drain. When the gate voltage is more positive than the source voltage in an n-type unit, or more negative in a p-type unit, the transistor is biased "on," and the conductivity of the conduction path increases by an amount determined by the difference in potential between gate and source. In the FIGURE 1 circuit, therefore, first transistor 10a is biased "on" and second transistor 20a is biased "off" when the voltage at gates 16a and 26a has a value of +V



volts. The only steady state current flow through the transistors 10a and 20a for this condition is due to leakage current in second transistor 20a, and the value of this current may be of the order of only a few microamperes giving rise to only a very small steady state power dissipation. On the other hand, when the voltage applied at gates 16a and 26a is zero, first transistor 10a is biased "off" and second transistor 20a is biased "on." Only the leakage current for first transistor 10a flows through the transistors 10a and 20a for this steady state condition.

In either steady state condition, first and second transistors 10a and 20a function essentially as a voltage divider. When first transistor 10a is "on" and second transistor 20a is "off," the voltage at junction 44 is essentially zero due to the high impedance condition of second transistor 20a relative to the relatively low impedance of first transistor 10a. When first transistor 10a is "off" and second transistor 20a is "on," the voltage at junction 44 has a value of approximately +V volts. As will be described, the voltage at junction 46 is zero when the voltage at junction 44 is +V volts, and vice versa. The state of the memory element could be sensed by sampling the voltage at either of the junctions 44 and 46 when a signal is applied tending to reset the memory element to a reference one of the two stable states. The disadvantage of such a sensing technique is that the voltage sensing device would have the effect of adding a large capacitance between either of the junctions 44 or 46 and circuit ground. This is especially true in the case of an array or group of memory elements all coupled to a common voltage sensing device. Since this large load capacitance would have to discharge and charge to the full V volts, the effect of the capacitance would be to slow down the switching speed of the memory element, and the memory cycle time. For the aforementioned reasons, it would be preferable to employ a current sensing technique to sense the state of the memory element or elements.

Insulated gate field effect transistors have certain characteristics that may be taken advantage of to achieve current sensing of the memory elements when the transistors are connected in a complementary symmetry arrangement. An insulated gate field effect transistor has a first capacitance between its source and drain, a second capacitance between its gate and source, and some small capacitance between its gate and drain. In FIGURE 1, it can be seen that the capacitance between the gate 16b and source 12b of the third transistor 10b is in parallel with the capacitance across the drain 14a and source 12a of the first transistor 10a.

The capacitor C_1 , as shown in dotted lines, represents the sum of these two capacitances together with the capacitance of any load (not shown) that might be connected between junction 44 and ground, and any stray capacitance that may appear between these points. In like manner, capacitor C_2 represents the sum of the gate 26b to source 22b capacitance of fourth transistor 20b, the drain 24a to source 22a capacitance of second transistor 20a, and stray capacitance appearing between junctions 44 and 29. Capacitor C_3 represents the capacitance between source 12a and gate 16a of first transistor 10a, and capacitor C_4 represents the capacitance between source 22a and gate 26a of second transistor 20a.

When the memory element is switched to the reference state from the other stable state, the voltage at junction 44 changes value. As a result thereof, certain ones of the capacitances $C_1 \dots C_4$ charge and others discharge, with the result that a transient current flows in the common path from voltage source 30 to junction point 29 and in the common connection from junction point 31 to circuit ground. This transient current may be sensed by the current response device 28 connected between junction 29 and the voltage source. Alternatively, the current sensor 28 may be connected in the common path between circuit ground and the source 12a and 12b of the first and third transistors 10a and 10b. For example, the sensor 28 could be connected between junction 31 and ground. Details of the current sensing technique will be clearer from the following detailed description of the memory element's operation.

Assume that at a time t_1 the steady state of the memory element is such that the voltage at junction 44 is at ground potential (Row A, FIGURE 2). This voltage, cross-coupled to gates 16b and 26b, biases fourth transistor 20b "on," and biases third transistor 10b "off." The voltage at junction 46 is essentially +V volts (Row B, FIGURE 2). Word source 40 supplies a voltage of ground potential at input terminal 38 at this time (Row C, FIGURE 2). With +V volts at its drain 22c and zero volts at its gate 26c, fifth transistor 20c is biased "on" and presents a relatively low impedance cross-coupling path between junction 46 and the gates 16a, 26a of the first and second transistors 10a and 20a, whereby the +V volts at junction 46 is coupled to the latter gates.

With +V volts applied at these gates 16a, 26a, second transistor 20a is biased "off," first transistor 10a is biased "on," and the voltage at junction 44 is maintained at ground potential. The memory element may be considered to be storing a binary



"1" bit of information under these conditions, i.e., when the voltages at junctions 44 and 46 are zero and $+V$ volts, respectively. Sixth transistor 10c is biased off at this time by the ground potential applied at its gate 16c and zero applied to source 12c (Row D, FIGURE 2).

Information stored in the memory element is read out when word source 40 supplies a signal or level of $+V$ volts at the second input terminal 38. In FIGURE 2, Row C, this signal 50a is shown as being applied starting at time t_1 . The effect of raising the voltage at second input terminal 38 to $+V$ volts is twofold. First, the input signal 50a biases fifth transistor 20c "off" to essentially open the cross-coupling path

16a, 26a of the first and second transistors between output terminal 46 and the gates

Second, raising the input voltage at second input terminal 38 turns "on" sixth transistor 10c; since the voltage at the gate 16c then is at $+V$ volts while the voltage at the source 12c is at ground potential (Row D, FIGURE 2). The conduction path of sixth transistor 10c then has a very low impedance path, whereby the ground potential at input terminal 32 appears at the drain electrode 14c and also at the gates 16a, 26a of the first and second transistors.

First transistor 10a turns "off" and second transistor 20a turns "on" when the voltage at gates 16a and 26a falls to ground potential. The voltage at junction 44 then rises to $+V$ volts (Row A, FIGURE 2). This positive voltage, applied at the gates 16b, 26b of the third and fourth transistors, turns "off" fourth transistor 20b and biases "on" third transistor 10b. The voltage at junction 46 then falls to ground potential (Row B, FIGURE 2). Fifth transistor 20c remains biased off by the word signal 50a, whereby the voltage at output terminal 46 is not coupled through the transistor 20c to the gates 16a, 26a of the first and second transistors. The memory element now is in the reset state and is storing a binary "0".

The state of the memory element prior to readout may be sampled at either of the junctions 44 or 46 by sensing for a change in voltage thereat when the word signal 50a is applied at t_1 . As will become apparent below, a change in voltage occurs when the word signal 50a is applied only if the memory element was storing a binary "1" immediately prior to the application of word signal 50a. However, it is much preferable in most instances to employ current sensing, for reasons previously stated. Current sensing is accomplished as follows.

Prior to t_1 , the voltage at the gates 16a and 26a is $+V$ volts and the voltage at junction 44 is zero. Capacitances C_1 and C_2 are charged to V volts in the polarity direction indicated at the left side of these capa-

citances in FIGURE 1. Capacitances C_1 and C_2 are uncharged. When the word signal 50a is applied at t_1 , the voltage at gates 16a and 26a changes from $+V$ volts to zero, and the voltage at junction 44 changes from zero to $+V$ volts as first transistor 10a turns "off" and second transistor 20a turns "on." During the switching transient, capacitors C_1 and C_2 discharge and capacitances C_1 and C_2 charge to V volts in the polarity direction indicated to the right of these capacitances in FIGURE 1. The paths for the charge and discharge currents are of importance to the current sensing operation.

Current, in the conventional sense, for charging capacitance C_1 flows from the positive terminal of voltage source 30 through current sensor 28 and the source 22a-drain 24a path of "on" transistor 20a to the top plate of the capacitance C_1 , and from the bottom plate of C_1 to the negative terminal of voltage source 30 via common lead 33 and circuit ground. This current is labelled " IC_1 " in FIGURE 1. Capacitance C_2 discharges directly through the source 22a-drain 24a path of "on" transistor 20a. Capacitance C_2 discharges through the drain 14c-source 12c path of "on" transistor 10c and the digit source 36. Current for charging C_1 flows from the positive terminal of voltage source 30 and through the current sensor 28 to the top plate of C_1 , and from the bottom plate of C_1 through "on" transistor 10c, digit source 36 and common lead 33 to ground and thence to negative terminal of voltage source 30. This current is labelled " IC_2 " in FIGURE 1.

In summary of the above, positive charge currents IC_1 and IC_2 flow through the current sensor 28 and through the common lead 33 when the memory element is switched from the "1" state to the "0" or reset state by the word signal 50a. These currents are of very short duration due to the low impedance charge paths. However, the total transient current may have an appreciable amplitude. Current spikes on the order of 6 milliamperes have been measured flowing through the current sensor 28 in an actual operative circuit. The output signal provided by the current sensor 28 during the transient current may be sampled during the switching period according to known techniques.

The time interval t_1 to t_2 (FIGURE 2) may be designated the "read period" since the information stored in the memory element is read-out during this period under control of the word source 40. Any new information to be written into the memory element may be entered during a "write" period following the read period. If it is desired to store a binary "0" bit, the digit



source 36 continues to supply a voltage of ground potential at input terminal 32 during the write period. If a binary "1" bit is to be stored, digit source 36 changes state to supply a voltage of +V volts at input terminal 32. In order to enter a binary "1" bit in the memory element, word source 40 also must supply a signal of +V volts, since otherwise sixth transistor 10c would be biased "off" and the signal from the digit source 36 would not be coupled to the memory element. Word source 40, therefore, is operated during both "read" and "write," and supplies the same voltage input during both these periods. This is a distinct advantage in a memory system since the word source and logic may be of simpler construction than one of the type used in the usual memory application wherein different polarity signals are required for read and write. Also, a single signal such as 50a (Row C, FIGURE 2) can be used for both read and write, reducing the total memory time cycle.

Consider that a binary "1" bit is to be written into the memory element. At time t_1 , the digit source 36 supplies a signal 60a of +V volts at input terminal 32 (Row D, FIGURE 2). Word source 40 also is supplying a voltage of +V volts at this time (Row C, FIGURE 2). Sixth transistor 10c then has +V volts applied at both its source 12c and its gate 16c; the drain 14c initially is at ground potential. A TFT or an MOS unit is bi-directional, and the source and drain are "interchangeable" in the sense that the "source" can operate as either the source or drain, depending on bias conditions. In such a unit, the transistor is biased "on" when the gate voltage is positive relative to the voltage at either the "source" or "drain" in an n-type transistor. Accordingly, for the input conditions in this example, sixth transistor 10c is biased "on" at t_1 since the gate voltage is +V volts and the "drain" is at ground potential.

With sixth transistor 10c in the "on" condition, the transistor provides a low impedance path between the gates 16a, 26a of the first and second transistors 10a and 20a and the input terminal 32. The voltage at gates 16a and 26a rises from ground potential to +V volts as the source 12c-drain 14c capacitance charges and capacitances C_1 and C_2 charge and discharge, respectively. When the +V volt value is reached, sixth transistor 10c turns "off." However, if the voltage at drain 14c should tend to fall in value, sixth transistor 10c would turn on again to maintain the drain 14c voltage at +V volts.

When the voltage at gates 16a, 26a is changed from ground potential to +V volts at t_1 , second transistor 20a turns "off,"

first transistor 10a turns "on" and the voltage at junction 44 falls to ground potential (Row A, FIGURE 2). Capacitances C_1 and C_2 discharge and charge, respectively. Current flows through the current sensor 28 during the switching transient, but the output of the sensor 28 is not sampled during this period in a memory application. When the voltage at junction 44 falls to zero, third transistor 10b turns "off," fourth transistor 20b turns "on" and the voltage at junction 46 rises to +V volts (Row B, FIGURE 2). A binary "1" now is stored in the memory element. Word signal 50a terminates at t_1 and the voltage at the gates 26c, 16c of the fifth and sixth transistors falls to zero volts. Fifth transistor 20c then turns "on" and sixth transistor 10c is held "off." The +V volts at output terminal 46 is coupled through the low impedance conduction path of the fifth transistor 20c to the gates 16a, 26a of the first and second transistors, keeping these transistors biased "on" and "off," respectively, and maintaining the memory element 9a in the binary "1" storage state.

Digit source 36 changes state at t_1 to terminate the digit signal 60a. It should be noted that word signal 50a terminates before digit signal 60a. If it did not, the voltage at input terminal 32 could fall to ground potential while the gate 16c voltage of sixth transistor 10c was at +V volts. Sixth transistor 10c would be biased "on," ground potential would be applied at the gates 16a, 26a of the first and second transistors, and the memory element would become reset, with a resulting loss of the stored information.

A second read period commences at time t_1 with the application of a second word signal 50b of +V volts applied at input terminal 38 (Row C, FIGURE 2). The memory element responds to this signal 50b in the same manner it responded to the first word signal 50a since a "1" is stored in the element prior to t_1 . Briefly stated, fifth transistor 20c turns "off," sixth transistor 10c turns "on" and applies ground potential at the gates 16a and 26a of the first and second transistors 10a and 20a to turn these transistors "off" and "on" respectively. As the voltage at junction 44 rises to +V volts (Row A, FIGURE 2) third transistor 10b turns "on," fourth transistor 20b turns "off" and the voltage at junction 46 falls to ground potential (Row B, FIGURE 2). During the switching transient, capacitances C_1 and C_2 charge, the charge current flowing through the current sensor 28. The output of the sensor 28 may be sampled (by means not shown) during the transient period.

The gates 16a, 26a of the first and second transistors are at ground potential during



the transient period.

The gates 16a, 26a of the first and second transistors are at ground potential during the read period by virtue of the "on" condition of the sixth transistor 10c and the ground potential applied at input terminal 32. Assume that it is desired to store a binary "0" in the memory element during the write period. The memory element is already in the reset state and storing a binary "0." No digit signal is supplied by the digit source 36 during the write period. Consequently, sixth transistor 10c continues to furnish a low impedance path between input terminal 32 and the gates 16a, 26a, whereby the gates remain at ground potential. Word signal 50b terminates at a time t_2 (Row C, FIGURE 2).

The memory element now is in the reset state, and the gates 16a, 26a of the first and second transistors are at ground potential. The next read period commences at t_3 with the application of a word signal 50c (Row C, FIGURE 2) applied at input terminal 38 from the word source 40. Word signal 50c biases "on" sixth transistor 10c. The voltage at input terminal 32 is at ground potential at this time (Row D, FIGURE 2). However, the voltage at drain 14c of the sixth transistor 10c is already at ground potential, whereby there is no change in voltage at the gates 16a, 26a of the first and second transistors 10a and 20a. Since these latter transistors do not change operating states, there is no change in voltage at either of the junctions 44 and 46 (Rows A and B, FIGURE 2). Consequently, there is no change in the state of the charge on any of the capacitances $C_1, \dots, C_n$ and no transient charge current flows through the current sensor 28. Hence, no output signal is produced by the current sensor 28.

In summary, the application of a word signal results in a transient current flow through the current sensor only when the memory element is storing a binary "1" bit of information. Accordingly, an output signal from the sensor during the read period indicates storage of a binary "1" bit. The absence of an output signal indicates storage of a binary "0" bit. Advantage is taken of this feature in the word-organized memory of FIGURE 3.

The memory of FIGURE 3 comprises a large number of memory planes, of which only the first and n^{th} planes 70-1 and 70n are shown for convenience. In general, the number of planes may be equal to the number of bits in a word. Each plane has a group or array of memory elements for storing the information bits of like significance of a large number of words, and each of the different bits of a word is stored in a memory element in a different plane. For

example, dashed box 72-1 in the first plane 70-1 may contain the memory element for storing the first bit of information in the k^{th} word, and dashed box 72n in plane 70n may contain the memory element for storing the n^{th} bit of information in the k^{th} word. The other memory elements of the planes 70-1 and 70n are omitted for clarity of drawing, but it will be understood that each of the remaining elements in the first plane 70-1 stores the first bit of a different word, and each of the remaining elements in the plane 70n stores the n^{th} bit of a different word.

Each memory element is assumed to be of the type shown in FIGURE 1, except as noted hereinafter, and there may be an array of m -by- m elements in each plane, whereby m^2 words may be stored in

All of the memory elements, one in each plane, associated with the same word are connected to a common word line. For example, the input terminals 38 (FIGURE 1) of the memory elements for all of the bits in the k^{th} word are connected to the same word line 74. This line 74, is connected to the appropriate word source or driver in box 76. The word driver performs the same function as the word source 40 in FIGURE 1, except that it is common to the memory elements for all bits of a word. All of the memory elements in any one plane are connected to a common digit source or driver. For example, all of the memory elements in the first plane 70-1 have their input terminals 32 (FIGURE 1) connected to a common digit driver 77-1.

Each memory plane 70-1..70n has associated therewith a separate current sensing device 78-1..78n, illustrated in the drawing as a tunnel diode. The junction points 29 of all of the memory elements in the first plane 70-1 are connected together and to the cathode of a common tunnel diode 78-1. Stated in another way, the sources 22a and 22b of the second and fourth transistors 20a and 20b of all memory elements in the first plane 70-1 are connected in common to the cathode of the tunnel diode 78-1, the anode of which is connected to the voltage source 30-1. The tunnel diode 78-1 is the current sensor 28 of FIGURE 1. By this arrangement, the currents flowing in all of the memory elements in the first plane 70-1 flow also through the tunnel diode 78-1. This current is very low in the steady state, being the sum of the leakage currents of the various elements. The memory elements in the other planes are similarly arranged.

A word of information is read out of memory by applying a word signal of +V volts to the word line of the desired word. For example, the k^{th} word is read out of

memory by conditioning the appropriate word driver to apply a signal of +V volts to word line 74. If the memory element for any bit of that word is storing a binary "1" when the word signal is applied, a transient current will flow in that memory plane. This transient current, which is the charge current for the capacitances C_1 and C_2 of the element being switched, flows through the tunnel diode associated with the plane in which the memory element is located.

The tunnel diode is selected to have a current peak that is greater than the total steady state leakage current of the elements in the plane, and less than the sum of the leakage currents plus the transient current that flows when an element in the plane is switched. The total leakage current, as mentioned above, is relatively small and may be less than the tunnel diode valley current, whereby the tunnel diode is operated monostably. In the steady state of the memory, therefore, each of the tunnel diodes is biased in an operating region of low voltage. The potential across the terminals of a tunnel diode may be a few tens of millivolts for this condition. When a memory element is reset by a word signal, the resulting transient current exceeds the peak current value of the associated tunnel diode and switches the diode temporarily to a state of high voltage. The voltage then appearing across the tunnel diode may be 400 to 800 millivolts, depending upon the type of diode, and is read out at the terminals 80-1, for example, and sampled during the read period. Any capacitance across the output terminals 80-1 may be charged and discharged rapidly at this low value of voltage through the low impedance of the tunnel diode, whereby the tunnel diode does not slow down the switching speed of the memory element.

Alternatively, the tunnel diode could be biased for bistable operation, whereby the tunnel diode, once switched, remains in a state of high voltage until reset (by means not shown). In this case, the tunnel diodes can serve the additional function of a memory register.

A memory system of the type illustrated in FIGURE 3 and comprising memory elements of the type as illustrated in FIGURE 1 has several advantages worthy of note. There is very little power dissipation in the various memory elements under steady state conditions. No output is derived from a memory element which is storing a binary "0" when the word signal is applied thereto. In a core memory, on the other hand, even a core which is storing a binary "0" generates an output signal when that core is interrogated, although the output signal has a smaller amplitude than is provided when the core is switched from

the "1" to the "0" state. A further advantage of this arrangement is that the memory elements can be manufactured in integrated form with high packing density using known fabrication techniques. Moreover, the various decoders, drivers and associated logic also can be manufactured at the same time, in integrated form, and preferably on the same substrate as the memory elements themselves. A further advantage is the fact that only a single read/write word pulse is required in the FIGURE 3 arrangement, whereas in a core type memory, separate read and write word pulses of opposite polarity generally are required.

One feature of the FIGURE 3 arrangement which may be a disadvantage in some cases is that a separate word line is required for each word of storage. For example, if each plane has an m -by- m array of memory elements, m^2 word lines are required for each plane, the like word lines of the separate planes being connected together. If the array is large, it may be difficult or undesirable to provide the large number of word lines. This problem may be obviated by an arrangement of the type illustrated in FIGURE 4.

In the arrangement of FIGURE 4 only two planes 84-1 and 84n of the memory are illustrated for convenience. Let it be assumed that each plane has an m -by- m array of memory elements, the same as in the case of the FIGURE 3 arrangement. There is provided a separate x input line for each row of memory elements, for a total of m row lines, and each x input line is common to all of the memory elements in the same numbered row in all of the planes. There is also a separate y input line for each column of memory elements, or a total of m , and each y input line is common to all of the memory elements in the same numbered column in all of the planes. For example, let the dashed box 90-1 in the first plane 84-1 contain the memory element at the intersection of the a^{th} row and b^{th} column of the first plane 84-1. Let the dashed box 90n contain the memory element at the intersection of the a^{th} row and b^{th} column of plane 84n. As shown in the drawing, the x input line 88 is common to both of these elements, as is the y input line 94. The total number of x and y input lines is $2m$, as contrasted to the m^2 lines required in the system of FIGURE 3.

The information stored in a memory element is read out when signals are applied on both of the x and y lines common to that element. A binary "1" bit of information is written into a memory element by energizing the information source for the memory plane containing that element

switched



while signals are present on both of the x and y lines common to that element. For example, the word stored in the group of memory elements that includes elements 90-1 and 90n is read out by applying signals concurrently to the x and y input lines 88 and 94. A binary "1" is written into the element 90-1 by energizing information source 96-1 during the write period when lines 88 and 94 are receiving input signals.

FIGURE 5 is a schematic drawing of a memory element suitable for use in the arrangement of FIGURE 4. This memory element is similar generally to the memory element of FIGURE 1, wherefore only the differences need be noted. In FIGURE 5, a seventh insulated gate field effect transistor 20d of p-type conductivity has its conduction path connected in parallel with the conduction path of fifth transistor 20c, and has its gate 26d connected to an input terminal 98. An eighth insulated gate field effect transistor 10d of n-type conductivity has its conduction path connected in series with the conduction path of sixth transistor 10c between input terminal 32 and the gates 16a, 26a of the first and second transistors, 10a, 20a. The gate 16d of the eighth transistor 10d is connected to input terminal 98. The signal sources 102, connected between input terminal 38 and ground, and the signal source 100, connected between input terminal 98 and ground, supply the x and y input signals, respectively, for the memory element.

The operation of the FIGURE 5 circuit is similar generally to the operation of the FIGURE 1 circuit, except for the following differences. In order to read out the information stored in the memory element, both the x and y input sources 102 and 100 must supply input signals. These input signals, which switch the voltages at terminals 38 and 98, respectively, from ground potential to +V volts, bias off the fifth and seventh transistors 20c and 20d to "open" the cross-coupling path from the drains 14b and 24b of the third and fourth transistors to the gates 16a, 26a of the first and second transistors. The signals supplied by sources 102 and 100 also bias "on" the sixth and eighth transistors 10c, 10d, respectively. A low impedance path then is provided through transistors 10c and 10d between input terminal 32 and the gates 16a, 26a of the first and second transistors to reset the memory element in the manner described in connection with the FIGURE 1 memory element.

To write a binary "1" bit of information into the memory element during the write period, the information source 96 supplies a signal of +V volts at input terminal 32 while the x and y input sources 102 and 100 are supplying input signals of +V

volts. If only one of the latter sources is supplying an input signal, then only one of the sixth and eighth transistors 10c, 10d is biased on. The other one of these transistors is biased "off," whereby the memory element cannot be reset during the read period, and new information cannot be written into the memory element during the write period. Hence the term "coincident voltage" memory element.

Various modifications may be made in the memory elements illustrated in FIGURE 1 and FIGURE 5. For example, n-type transistors may be substituted for the p-type transistors illustrated, and p-type transistors may be substituted for the n-type transistors, provided that the connections to the bias source 30 and current sensors 28 are reversed and provided also that the polarities of the digit and word signals are reversed. Also, the voltage levels may be changed by grounding the drain electrodes 22a, 22b of the first and fourth transistors 20a, 20b and connecting the bias source 30 between circuit ground and the sources 12a, 12b of the first and third transistors 10a, 10b with suitable change in the input signal levels.

WHAT WE CLAIM IS:—

1. A memory storage unit comprising a plurality of field effect transistors each having a source and a drain defining the ends of a conduction path, and an insulated gate; first, third and sixth ones of said transistors being of one conductivity type and second, fourth and fifth ones of said transistors being of the opposite conductivity type; said first and second transistors having their conduction paths serially connected in a first branch circuit with their drains connected together; said third and fourth transistors having their conduction paths serially connected in a second branch circuit with their drains connected together; a connection between the gates of the first and second transistors; a connection between the gates of the third and fourth transistors; a connection between the drains of the first and second transistors to a point common to the gates of the third and fourth transistors; the fifth transistor having its conduction path connected between a point common to the drains of the third and fourth transistors and a point common to the gates of the first and second transistors; a first input terminal; the sixth transistor having its conduction path connected between said first input terminal and the gates of the first and second transistors; and a second input terminal connected to the gates of said fifth and sixth transistors;

2. A memory storage unit according to Claim 1, comprising a current sensor con-



while signals are present on both of the x and y lines common to that element. For example, the word stored in the group of memory elements that includes elements 5 90-1 and 90n is read out by applying signals concurrently to the x and y input lines 88 and 94. A binary "1" is written into the element 90-1 by energizing information source 96-1 during the write period when 10 lines 88 and 94 are receiving input signals.

FIGURE 5 is a schematic drawing of a memory element suitable for use in the arrangement of FIGURE 4. This memory element is similar generally to the memory 15 element of FIGURE 1, wherefore only the differences need be noted. In FIGURE 5, a seventh insulated gate field effect transistor 20d of p-type conductivity has its conduction path connected in parallel with 20 the conduction path of fifth transistor 20c, and has its gate 26d connected to an input terminal 98. An eighth insulated gate field effect transistor 10d of n-type conductivity has its conduction path connected in series 25 with the conduction path of sixth transistor 10c between input terminal 32 and the gates 16a, 26a of the first and second transistors, 10a, 20a. The gate 16d of the eighth transistor 10d is connected to input 30 terminal 98. The signal source 102, connected between input terminal 38 and ground, and the signal source 100, connected between input terminal 98 and ground, supply the x and y input signals, 35 respectively, for the memory element.

The operation of the FIGURE 5 circuit is similar generally to the operation of the FIGURE 1 circuit, except for the following differences. In order to read out the 40 information stored in the memory element, both the x and y input sources 102 and 100 must supply input signals. These input signals, which switch the voltages at terminals 38 and 98, respectively, from ground 45 potential to +V volts, bias off the fifth and seventh transistors 20c and 20d to "open" the cross-coupling path from the drains 14b and 24b of the third and fourth transistors to the gates 16a, 26a of the first and 50 second transistors. The signals supplied by sources 102 and 100 also bias "on" the sixth and eighth transistors 10c, 10d, respectively. A low impedance path then is provided through transistors 10c and 10d between 55 input terminal 32 and the gates 16a, 26a of the first and second transistors to reset the memory element in the manner described in connection with the FIGURE 1 memory element.

To write a binary "1" bit of information 60 into the memory element during the write period, the information source 96 supplies a signal of +V volts at input terminal 32 while the x and y input sources 102 and 65 100 are supplying input signals of +V

volts. If only one of the latter sources is supplying an input signal, then only one of the sixth and eighth transistors 10c, 10d is biased "on". The other one of these transistors is biased "off," whereby the memory 70 element cannot be reset during the read period, and new information cannot be written into the memory element during the write period. Hence the term "coincident voltage" memory element. 75

Various modifications may be made in the memory elements illustrated in FIGURE 1 and FIGURE 5. For example, n-type transistors may be substituted for the p-type transistors illustrated, and p-type transistors 80 may be substituted for the n-type transistors, provided that the connections to the bias source 30 and current sensors 28 are reversed and provided also that the polarities of the digit and word signals are 85 reversed. Also, the voltage levels may be changed by grounding the drain electrodes 22a, 22b of the first and fourth transistors 20a, 20b and connecting the bias source 30 between circuit ground and the sources 12a, 90 12b of the first and third transistors 10a, 10b with suitable change in the input signal levels.

WHAT WE CLAIM IS:—

1. A memory storage unit comprising a 95 plurality of field effect transistors each having a source and a drain defining the ends of a conduction path, and an insulated gate; first, third and sixth ones of said transistors being of one conductivity type and 100 second, fourth and fifth ones of said transistors being of the opposite conductivity type; said first and second transistors having their conduction paths serially connected in a first branch circuit with their 105 drains connected together; said third and fourth transistors having their conduction paths serially connected in a second branch circuit with their drains connected together; a connection between the gates of 110 the first and second transistors; a connection between the gates of the third and fourth transistors; a connection between the drains of the first and second transistors to a point common to the gates of the third 115 and fourth transistors; the fifth transistor having its conduction path connected between a point common to the drains of the third and fourth transistors and a point common to the gates of the first and second 120 transistors; a first input terminal; the sixth transistor having its conduction path connected between said first input terminal and the gates of the first and second transistors; and a second input terminal connected 120 to the gates of said fifth and sixth transistors.

2. A memory storage unit according to Claim 1, comprising a current sensor con-



ected in series with the first and second circuit branches of said circuit.

3. A memory storage unit according to Claim 1, in which said circuit also includes
5 a seventh transistor of said opposite conductivity type having its conduction path connected in parallel with the conduction path of said fifth transistor, an eighth transistor of said one conductivity type having
10 its conduction path connected in series with the conduction path of said sixth transistor between said first input terminal and a point common to the gates of said first and second transistors, and a third input terminal common to the gates of the seventh
15 and eighth transistors.

4. A memory comprising: a plurality of groups of memory elements, each memory element including: an insulated gate field
20 effect transistor bistable circuit having an input point, and an insulated gate field effect input transistor having a drain connected to the input point, a source and a gate; a like plurality of control lines, one
25 for each said groups of memory elements; a plurality of signal input lines; means connecting the gates of all input transistors in the same group to the control line associated with that group; and means connecting
30 the source of each input transistor of a said group to a different one of said signal input lines.

5. A memory storage unit comprising first and second insulated gate field effect
35 transistors each having a source, a drain and a gate, first and second circuit branches connected in parallel to each other and across a source of operating potential, the first branch including the source-drain path
40 of the first transistor and a load connected in series therewith, the second branch including the source-drain of the second transistor and a load connected in series therewith, means cross-coupling the drains of
45 the first and second transistors to the gates of the second and first transistors, respectively,

in order to form a bistable circuit, and an input terminal; a third insulated gate field effect transistor having a source, a drain and a gate; means connecting the
50 source-drain path of the third transistor between said input terminal and the gate of the first transistor, said input terminal being adapted to receive information signals from a source of input signals; with the
55 gate of the third transistor being adapted to receive first control signals which are substantially concurrent with said information signals and which are effective to render said third transistor source-drain
60 path conductive; where the source-drain path of the third transistor, in the absence of such a control signal is substantially non-conductive.

6. A memory storage unit as claimed in
65 claim 5, wherein the cross-coupling means includes a fourth insulated gate field effect transistor having a source, a drain and a gate; with the source-drain path of the
70 fourth transistor being connected between the drain of the second transistor and the gate of the first transistor; the gate of the fourth transistor being adapted to receive from a source of second control signals
75 substantially concurrent with said information signals and said first control signals; where the second control signals are effective to render the source-drain path of said
fourth transistor substantially non-conductive, and where said source-drain path is
80 conductive in the absence of said second control signals.

7. A memory storage unit substantially as described with reference to the examples shown in Figures 1 and 5, of the accompanying drawings.

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