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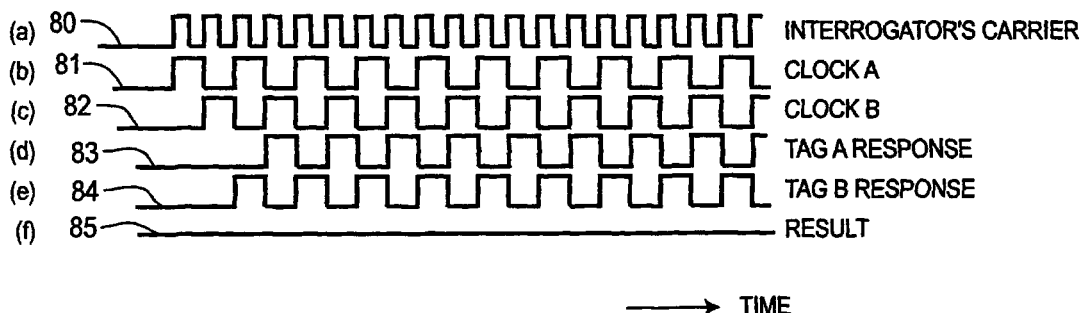
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(54) Title: ENCODING/DECODING SYSTEM FOR COHERENT SIGNAL INTERFERENCE REDUCTION



(57) Abstract: An apparatus is described for reducing coherent signal interference between at least two bit streams framed with a common clock signal. The apparatus includes an internal clock signal generated from the common clock signal and a Manchester encoder for encoding the internal clock signal with a unique signature. Also included is a logic AND-gate for combining one bit stream of the two bit streams with the encoded clock signal to produce an encoded output signal. When the encoded output signal is combined with another of the two bit streams during transmission, individual bits of the combined bit streams are identifiable at a receiving end. The receiving end decodes the combined bit streams and properly discriminates between ONES and ZEROS.

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