DUAL-DAMASCENE INTERCONNECTS WITHOUT AN ETCH STOP LAYER BY ALTERNATING ILDS

FIELD OF THE INVENTION

The invention relates to field of fabrication of interconnect layers in a semiconductor device.

PRIOR ART AND RELATED ART

In current integrated circuits, several layers of interconnect structures fabricated above a substrate containing active devices are often used. Each interconnect layer is fabricated in, or on, an interlayer dielectric (ILD). Vias are etched in each ILD to make contact with conductors in an underlying layer. It is generally accepted that the dielectric material in each ILD should have a low k to obtain low capacitance between the conductors. Often the low k dielectrics have low densities and etch quite rapidly. Particularly for unlanded contacts, over etching can occur and extend into an underlying layer causing a defect. For this reason, etchant stops are formed between each layer. Unfortunately, these etchant stop layers typically have higher k values, and thereby increase the capacitance between conductors.

The problem is shown in Figure 1 where a first ILD 10 includes a copper conductor and via fabricated with a dual damascene process. When an opening 12 is etched into the next ILD 11, the layer 13 acts as an etchant stop to prevent etching into the underlying ILD 10. But for the layer 13, the region shown by the dotted line 14 may be etched away causing a defect. Consequently, the layer 13 is needed even though it increases the capacitance between conductors.

Typically the layer 13 acts both as an etchant stop and as a diffusion barrier. Layer 13's role as an etchant stop is the major contributor to the capacitance since a layer thickness of 800 - 1600Å is often used for the etchant stop function compared to only 200Å needed to provide the barrier function.

Another technology that may be used instead of using the layer 13 of Figure 1 as a barrier layer is to use a shunt layer with cobalt or nickel or an alloy thereof. This involves the selection deposition of a shunting material over the copper lines to present electromigration into the overlying ILD. This is discussed in co-pending application 09/753,256; Interconnect Structures and a Method of Electroless Introduction of Interconnect Structures, assigned to the assignee of the present application, filed 12/28/2000.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a cross-sectional elevation view showing two levels of an interlayer dielectric (ILD) as used in the prior art.

Figure 2 is a cross-sectional elevation view showing two ILDs as fabricated in accordance with an embodiment of the present invention.

Figure 3 is a cross-sectional elevation view showing several ILDs fabricated with an embodiment of the present invention.

DETAILED DESCRIPTION

An integrated circuit interconnect structure and process for fabricating the structure is described. In the following description, numerous specific details are set forth such as specific-interlayer dielectrics (ILD) materials in order to provide a thorough understanding of the present invention. It will be apparent to one skilled in the art that the present

invention may be practiced without these specific details. In other instances, well known processing steps, such as etching and deposition steps, are not described in detail in order not to unnecessarily obscure the disclosure.

The present invention uses at least two different ILD materials which are alternated from one interconnect level to the next. The materials are selected such that each of the materials is etchable more rapidly in the presence of the other material. In one embodiment, the first material is an organic low k dielectric such as a polymer based dielectric and the second material is an inorganic material such a carbon-doped oxide.

The first category of materials, the organic polymers, are typically spun-on. A discussion of perfluorocyclobutane (PFCB) organic polymers is found in "Integration of Perfluorocyclobutane (PFCB)", by C. B. Case, C. J. Case, A. Kornblit, M. E. Mills, D. Castillo, R. Liu, Conference Proceedings, ULSI XII.COPYRGT. 1997, Materials Research Society, beginning at page 449. These polymers are available from companies such as Dupont, Allied Signal, Dow Chemical, Dow Corning, and others.

The second category of materials that may be used in the present invention are silica-based such as the nanoporous silica aerogel and xerogel. These dielectrics are discussed in "Nanoporous Silica for Dielectric Constant Less than 2", by Ramos, Roderick, Maskara and Smith, Conference Proceedings ULSI XII.COPYRGT. 1997, Materials Research Society, beginning at page 455 and "Porous Xerogel Films as Ultra-Low Permittivity Dielectrics for ULSI Interconnect Applications", by Jin, List, Lee, Lee, Luttmer and Havermann, Conference Proceedings ULSI XII.COPYRGT. 1997, Materials Research Society, beginning at page 463.

Assume for sake of discussion that a process has six levels of metalization, identified as ILDs 0-5. While the present invention in some cases may be used in all of the six levels of ILD, in one embodiment it is used for levels 1-4. The 0 level ILD generally contacts the

substrate and may require different processing such as discussed in US Patent 6,124,191. The uppermost ILD level typically receives special processing for packaging purposes such as the inclusion of bumps, and for this reason, an undoped silicon dioxide layer may be used.

Referring to Figure 3, the structure for four consecutive ILD levels 30, 31, 32, and 33 is illustrated. These levels may be levels 1-4 in a six level metalization process. Levels one and three are formed from a first ILD material which may be, for instance, a low k carbon-doped oxide. The alternate layers 31 and 33, as indicated, are fabricated from a second ILD material such as a polymer based dielectric.

As shown is Figure 3, vias and conductors are formed in each of the ILDs 30-33. These vias and conductors may be formed in an ordinary way using, for instance, a dual-damascene process. In this case, both the vias and conductors may, for instance, be fabricated from a copper or copper alloy which is enclosed within a conductive barrier material to prevent the copper from diffusing into adjacent dielectric materials.

In Figure 3, a barrier layer of silicon nitride or silicon carbide 34 is used between the ILDs. This dielectric presents the copper from diffusing into the ILDs. Layer 34, as mentioned above, may be relatively thin (e.g. 200Å) since it is not used as an etchant stop. Thus, it does not add to the interconnector and interconductor capacitance to the extent that the thicker etchant stop would.

In Figure 2, some of the processing used to fabricate a structure for one embodiment is illustrated. First ILD 19 is fabricated from a first material such as the polymer based dielectric and includes vias and conductors. A shunting layer 25 is added over the copper conductors to present electromigration for this embodiment. Then ILD 20 is formed from a second dielectric material such as the carbon-doped oxide. Vias and conductors are

fabricated in ILD 20 along with the shunting layer 25. All of this is done with known processing steps.

Now an ILD 21 is formed directly on ILD 20 without an intermediate etchant stop such as layer 13 of Figure 1. ILD 21 is fabricated from a first material such as the polymer based dielectric.

Patterning is used for each layer to define the via and conductor openings such as with a sacrificial light absorbing material (SLAM) or a dual hard masked process to form the opening 24 and like openings or a combination of these steps. The opening 24, is used to form a contact and conductor.

In Figure 2, a shunting material is used to provide a barrier whereas in Figure 3, a dielectric is used for the barrier. Both may be used at the same level in the ILDs or they may be alternated. For instance, often the shunting material has been deposited, the barrier dielectric may be formed. An opening is etched in the dielectric for a via when the via/conductor openings are etched for the overlying ILD.

Importantly, with the disclosed embodiment, the first material etches with a first etchant more rapidly than the underlying second material of the ILD 20. Preferably the differential etching rate is 20 to 1, or greater. Thus, when the opening 24 is etched, and the etchant reaches the second material, very little etching occurs in the ILD second material. For this reason, the defect shown by the dotted line 14 of Figure 1 does not occur even though there is no etchant stop.

Similarly, when the openings were etched in the ILD 20, an etchant is used that etches the second material more rapidly than the first material. Thus, when an opening was etched in the ILD 20, the etchant did not etch into the underlying first material. Again it is preferred that the etchant used to etch the first material etches this material at a rate at least 20 times faster than the first material.

While in one embodiment all the even number ILD levels are made from a first material and all the odd number ILD levels are made from a second material, this is not necessary. Each layer may have a different material a long as a layer can be etched at a higher rate than the underlying layer. However, it maybe more cost effective for all the odd numbered layers to be made of a first material and all of the even numbered layers to be made of a second material.

The inorganic materials discussed above may be etched with fluorocarbon such as C_4F_8, C_5F_8, C_2F_6, C_4F_6, CF_4 or CH_2F_2. The fluorocarbon is typically used in a mixture with oxygen and argon. A selective of 20 to 1 is achievable between the inorganic or organic ILDs discussed above.

The organic polymers discussed above may be etched with hydrogen or oxygen which in effect burns the polymer in a mixture with nitrogen. A selective of 30 to 1 is achievable between the organic and inorganic dielectrics.

Thus, ILDs with reduced capacitance has been disclosed.

CLAIMS

What is claimed.

1. An integrated circuit comprising:
   a first interlayer dielectric layer (ILD) of a first material, the first material having a first etchant rate when exposed to a first etchant;
   a second ILD of a second material disposed on the first ILD, the second ILD having an etchant rate slower than the first etching rate when exposed to the first etchant;
   a third ILD disposed on the second ILD of the first material.

2. The integrated circuit defined by claim 1 wherein the second material etches more rapidly than the first material when exposed to a second etchant different than the first etchant.

3. The integrated circuit defined by claim 2 wherein the first material comprises an organic based dielectric.

4. The integrated circuit defined by claim 3 wherein the second material comprises a non-organic based dielectric.

5. The integrated circuit defined by claim 1 including a fourth layer disposed on the third layer fabricated from the second material.

6. The integrated circuit defined by claim 5 wherein the first material comprises a polymer based dielectric.

7. The integrated circuit defined by claim 6 wherein the second material comprises a carbon-doped oxide.

8. An integrated circuit comprising:
   first interlayer dielectrics (ILDs) disposed alternately between second ILDs;

the first ILDs being etchable at a higher rate than the second ILDs by a first etchant;

the second ILDs being etchable at a higher rate than the first ILD's by a second etchant.

9. The integrated circuit defined by claim 8 where the first ILD include first conductors and first vias.

10. The integrated circuit defined by claim 9 wherein the second ILD's include second conductors and second vias.

11. The integrated circuit defined by claim 10 wherein the first ILDs comprise a polymer based dielectric.

12. The integrated circuit defined by claim 11 wherein the second ILDs comprise a carbon-based oxide.

13. An integrated circuit comprising:

first interlayer dielectrics (ILDs) disposed alternatively between second ILDs of first and second materials, respectively, wherein each of the first and second materials are etchable at faster rates than the other in the presence of different etchants.

14. The integrated circuit defined by claim 13 wherein the first ILDs include first conductors and first vias.

15. The integrated circuit defined by claim 14 wherein the second ILDs include second conductors and second vias.

16. The integrated circuit defined by claim 13 wherein the material for the first ILDs comprises an organic based dielectric.

17. The integrated circuit defined by claim 16 wherein the material for the second ILDs comprises a non-organic based dielectric.

18. An integrated circuit comprising:
    a first interlayer dielectric (ILD);
    a second ILD disposed over the first ILD, the second ILD being etchable at a faster rate than the first ILD by a first etchant;
    a third ILD disposed over the second ILD, the third ILD being etchable at a faster rate than the second ILD by a second etchant.

19. The integrated circuit defined by claim 18 wherein the first and third ILDs are fabricated from a first material.

20. The integrated circuit defined by claim 18 including a fourth ILD disposed over the third ILD, the second and fourth ILDs being fabricated from a second material.

21. The integrated circuit defined by claim 18 including conductors and vias in each of the ILD layers.

22. The integrated circuit defined by claim 20 wherein the first and third ILDs are fabricated from a polymer based dielectric.

23. The integrated circuit defined by claim 22 wherein the second ILD is fabricated from a carbon-based oxide.

24. The integrated circuit defined by claim 20 wherein the first and third ILDs are fabricated from a carbon-based oxide and the second and fourth ILDs are fabricated from a polymer based dielectric.

25. A method for fabricating an integrated circuit comprising:
    depositing a first ILD;
    forming vias and conductors in the first ILD;
    forming a second ILD directly on the first ILD;
    etching openings in the second ILD with an etchant that etches the second ILD faster than the first ILD;
    forming a third ILD directly on the second ILD; and

etching openings in the third ILD with an etchant that etches the third ILD faster than the second ILD.

26. The method defined by claim 25 wherein the second ILD comprises a carbon-based oxide.

27. The method defined by claim 26 wherein the third ILD comprises a polymer based dielectric.

28. The method defined by claim 27 wherein the second ILD is etched with a fluorocarbon.

29. The method defined by claim 28 wherein the third ILD is etched with oxygen or hydrogen.

30. The method defined by claim 25 including the steps of forming vias and conductors in the second and third ILDs.

31. A method of fabricating an integrated circuit comprising:

forming first alternate interlayer dielectrics (ILDs) of a first material;

forming second ILDs intermediate between the first ILDs of a second material where the second ILDs are etchable at a faster rate than the first ILDs by a first etchant and where the second ILDs are etchable at a faster rate than the first ILDs by a second etchant.

32. The method defined by claim 31 wherein the first material comprises an organic based material, and wherein the second material comprises a non-organic based material.

33. The method defined by claim 32 including forming vias and conductors in each of the ILDs.

34. The method defined by claim 33 wherein the vias and conductors are formed with a dual-damascene process.

35. The method defined by claim 31 wherein the first and second layers are separated by a barrier dielectric.

36. The method defined by claim 31 wherein conductors in the first and second layer are covered by a shunting material.

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