Claims

1. A failure location method for a 3D stacked integrated circuit chip, characterized in that the method comprises:

- determination of multiple comparative detection layers at different depths in the standard sample device;
- after grinding out the contrast detection layer each time, carry out short-circuit failure treatment on the surface of the exposed contrast detection layer to form a failure simulation hot spot, so that the contrast detection layer is in a failure state; use a thermal imager to detect all exposed compare the phase values corresponding to different detection frequencies of the detection layer in the failure state;
- determine the failure location curve of the comparison detection layer according to the corresponding relationship between the detection frequency and the phase value of each comparison detection layer in the failure state; wherein, the failure location curve is a curve in which the phase value of the comparison detection layer changes with the detection frequency;
- failure location of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curve of each comparative detection layer; wherein the standard sample device is a 3D stacked packaged integrated circuit chip of the same type as the 3D stacked packaged integrated circuit chip to be tested without failure the composition film layers of the standard sample device and the corresponding positions of each composition film layer are the same as the composition film layers

and the corresponding positions of each composition film layer of the 3D stacked package integrated circuit chip to be tested; the composition films of different positions layers correspond to different depths.

2. The method for locating failures of 3D stacked packaged integrated circuit chips according to claim 1, wherein the determination of a plurality of comparative detection layers at different depths in the standard sample device comprises:

- determining a plurality of comparative detection layers at different depths according to the thickness of the standard sample device;
- alternatively, a plurality of contrast detection layers at different depths are determined according to the functional film layers of the standard sample device.

3. The method for locating failures of 3D stacked packaged integrated circuit chips according to claim 1, wherein the phase values corresponding to different detection frequencies of the comparison detection layer exposed by the detection comprises from the side of the standard sample device away from the grinding side with a thermal imager, detecting the phase values of the exposed contrast detection layer at different detection frequencies.

4. The method for locating failures of 3D stacked packaged integrated circuit chips according to claim 2, wherein a plurality of comparative detection layers located at different depths are determined according to the thickness of the standard sample device, comprising

- dividing the standard sample device into multiple alternative contrast layers of equal thickness according to the predetermined thickness;
- selecting the candidate contrast layer at intervals as the contrast detection layer.

5. The method for locating failures of 3D stacked packaged integrated circuit chips according to claim 2, wherein said determining a plurality of comparative detection layers located at different depths according to the functional film layers of said standard sample device comprises:

- determining the functional film layer that the standard sample device has as an alternative contrast layer;
- selecting the candidate contrast layer at intervals as the contrast detection layer.

6. The method for locating failures of 3D stacked packaged integrated circuit chips according to claim 5, wherein the functional film layer of the standard sample device comprises: a solder ball layer, a PCB substrate, and a first connection contact layer stacked in sequence, a transition unit, a second connection contact layer and a top-layer chip; the interval selection of the alternative contrast layer as the contrast detection layer comprises selecting the solder ball layer located on the side of the PCB substrate away from the transition unit, the first connection contact layer between the PCB substrate and the transition unit, and the second contact layer between the transition unit and the top chip. the connecting contact layer is a contrast detection layer.

7. The method for locating failures of 3D stacked packaged integrated circuit chips according to claim 1, characterized in that, before the failure location of the 3D stacked packaged integrated circuit chips to be tested according to the failure location curves of each comparative detection layer, further comprising:

- detect the phase values of the 3D stacked packaged integrated circuit chip to be tested at different detection frequencies by a thermal imager; wherein, the detection frequency range of the 3D stacked packaged integrated circuit chip to be tested is within the detection frequency range of the standard sample device within the frequency range;
- determine the failure position curve to be tested according to the corresponding relationship between the detection frequency and the phase value of the 3D stacked packaged integrated circuit chip to be tested; curve.

8. The failure location method for a 3D stacked packaged integrated circuit chip according to claim 7, wherein the failure location of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curve of each comparison detection layer comprises:

according to the relative distance between the failure location curve of each comparative detection layer and the failure position curve to be tested, the position of the failure film layer of the 3D stack package integrated circuit chip to be tested is determined.

9. A failure location device for a 3D stacked packaged integrated circuit chip, characterized in that it is used to perform the failure location method for a 3D

stacked packaged integrated circuit chip according to any one of claims 1-8, comprising:

- a comparative detection layer determination unit configured to determine a plurality of comparative detection layers at different depths in the standard sample device;
- the phase value detection unit being used to detect the phase values corresponding to different detection frequencies of the exposed contrast detection layer in the failure state through a thermal imager after each layer of the contrast detection layer is ground sequentially;
- the failure location curve determination unit being used to determine the failure location curve of the comparison detection layer according to the corresponding relationship between the detection frequency and the phase value of each comparison detection layer in the failure state; wherein, the failure location curve is the phase value of the comparison detection layer The curve changing with the detection frequency;
- the failure location unit being used to locate the failure of the 3D stacked packaged integrated circuit chip to be tested according to the failure location curve of each comparative detection layer; wherein the standard sample device is the same type of intact 3D stacked packaged integrated circuit chip to be tested 3D stacked packaged integrated circuit chips.

10. A 3D stacked packaged integrated circuit chip, characterized in that it comprises a multi-layered film layer, and the failure location is performed by the failure location method of the 3D stacked packaged integrated circuit chip according to any one of claims 1~8.