WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a row decoder configured to decode a row address to generate a word line selection signal;

a column decoder configured to decode a column address to generate a column selection signal;

a memory cell array comprising a plurality of memory cells, one or more memory cells are selected in response to the word line selection signal and the column selection signal; and

an error correcting code (ECC) decoder configured to receive first data and a parity output from selected memory cells of the memory cell array and generate a syndrome based on the first data and the parity, and in response to a read operation of the semiconductor memory device being performed, to generate second data and a decoding status flag (DSF) indicating a type of an error of the first data by the syndrome and to output the second data and the DSF to an external device outside of the semiconductor memory device,

wherein a number of bits of the first data is the same as a number of bits of the second data, and

wherein the ECC decoder includes:

a syndrome generator configured to perform an exclusive OR (XOR) operation on each of row vectors of a second H matrix, and the first data and the parity and then perform a modulo 2 operation thereon to generate a predetermined number of bits of syndrome;

an error detector configured to detect a non-error, a correctable error, or an uncorrectable error using the syndrome;

an error position detector configured to detect a position of column vector of the second H matrix in which the syndrome is present to generate error position information when the correctable error is detected;

an error corrector configured to correct errors of the first data and the parity on the basis of the error position information when the correctable error is detected; and

a DSF generator configured to generate the DSF of a first state when the non-error or the correctable error is detected and generate the DSF of a second state when the uncorrectable error is detected.

2. The semiconductor memory device of claim 1, further comprising:

an ECC encoder configured to receive third data from the external device, to generate the parity, and to output fourth data and the parity to the selected memory cells when a write operation of the semiconductor memory device is performed,

wherein a number of bits of the third data is the same as a number of bits of the fourth data.

3. The semiconductor memory device of claim 2, wherein the ECC encoder includes a parity generator configured to perform an exclusive OR (XOR) operation on each of row vectors of a first H matrix and on the third data and then perform a modulo 2 operation thereon to generate the parity, and

wherein codes of column vectors of the first H matrix have different codes including “0” and “1,” that are not all “0,” and a minimum Hamming distance between the codes of the first H matrix is three.

4. The semiconductor memory device of any one of claims 1 to 3, wherein the ECC decoder is configured to:

output the first data as the second data when the syndrome indicates the non-error,

correct a corresponding bit of the first data and the parity and then output the corrected data as the second data when the syndrome indicates the correctable error, and

generate the DSF having the first state when the syndrome indicates the non-error or the correctable error and the second state when the syndrome indicates the uncorrectable error.

5. The semiconductor memory device of any one of claims 1 to 4, wherein the second data and the DSF are output to the outside of the semiconductor memory device in series or in parallel when the read operation is performed.

6. The semiconductor memory device of any one of claims 1 to 5, wherein codes of column vectors of the second H matrix have different codes including “0” and “1,” that are not all “0,” and a minimum Hamming distance between the codes of the second H matrix is three.

7. A memory system comprising:

a semiconductor memory device comprising:

a row decoder configured to decode a row address to generate a word line selection signal;

a column decoder configured to decode a column address to generate a column selection signal;

a memory cell array comprising a plurality of memory cells, one or more memory cells are selected in response to the word line selection signal and the column selection signal; and

a first error correcting code (ECC) decoder configured to:

perform a first ECC decoding operation by receiving first data and a parity output from selected memory cells of the memory cell array,

generate a syndrome based on the first data and the parity,

generate second data by performing the first ECC decoding operation, and

generate a decoding status flag (DSF) indicating a type of an error of the first data by the syndrome when a read operation of the semiconductor memory device is performed; and

a controller configured to control the semiconductor memory device, the controller comprising:

a second ECC decoder configured to perform an ECC decoding operation selected from among a plurality of ECC decoding operations on the second data applied from the semiconductor memory device in response to the DSF applied from the semiconductor memory device,

wherein the first ECC decoder includes:

a first syndrome generator configured to perform an exclusive OR (XOR) operation on each of row vectors of a second H matrix, and the first data and the parity and then perform a modulo 2 operation thereon to generate a predetermined number of bits of syndrome;

a first error detector configured to detect a non-error, a correctable error, or an uncorrectable error using the syndrome;

a first error position detector configured to detect a position of column vector of the second H matrix in which the syndrome is present to generate error position information when the correctable error is detected;

a first error corrector configured to correct errors of the first data and the parity on the basis of the error position information when the correctable error is detected; and

a DSF generator configured to generate the DSF of a first state when the non-error or the correctable error is detected and generate the DSF of a second state when the uncorrectable error is detected.

8. The memory system of claim 7, wherein the first ECC decoder outputs the first data as the second data when the syndrome indicates the non-error,

when the syndrome indicates the correctable error, corrects a corresponding bit of the first data and the parity and then outputs the corrected data, and

generates the DSF having the first state when the syndrome indicates the non-error or the correctable error and the second state when the syndrome indicates the uncorrectable error.

9. The memory system of claim 7 or claim 8, wherein the semiconductor memory device outputs the second data and the DSF to the controller in series or in parallel when the read operation is performed.

10. The memory system of claim 7, wherein the second ECC decoder comprises:

a first ECC decoding unit configured to perform a second ECC decoding operation in response to the DSF of the first state; and

a second ECC decoding unit configured to perform a third ECC decoding operation in response to the DSF of the second state,

wherein the second ECC decoding operation is an error detection operation, and

the third ECC decoding operation is an error correction and detection operation.

11. The memory system of any one of claims 7 to 10, wherein the second ECC decoder comprises:

a syndrome generator configured to perform an exclusive OR (XOR) operation on each of row vectors of an H matrix and the second data and then perform a modulo 2 operation thereon to generate a predetermined number of bits of syndrome;

an error detector configured to detect the non-error or a 3-bit or less error using the syndrome;

an error position detector configured to detect a position of column vector of the H matrix in which the syndrome is present to generate error position information when a 3-bit or less error is detected in response to the DSF; and

an error corrector configured to correct an error of the second data on the basis of the error position information in response to the DSF when the 3-bit or less error is detected,

wherein codes of column vectors of the H matrix have different codes including “0” and “1,” that are not all “0,” and a minimum Hamming distance between the codes of the H matrix is three.