

METHOD AND STRUCTURE FOR FORMING STRAINED DEVICES

Field of Invention

The invention generally relates to semiconductor devices and methods for manufacturing such devices, and more particularly to methods for forming a smooth boundary between nitride films to enhance device performance and product yield.

Background Description

Generally, metal-oxide semiconductor transistors include a substrate made of a semiconductor material such as silicon. The transistors typically include a source region, a channel region and a drain region within the substrate. The channel region is located between the source and the drain regions. A gate stack, which usually includes a conductive material, a gate oxide layer and sidewall spacers, is generally provided above the channel region. More particularly, the gate oxide layer is typically provided on the substrate over the channel region, while the gate conductor is provided above the gate oxide layer. The sidewall spacers help protect the sidewalls of the gate conductor.

The current flowing through a channel, which has a given electric field across it, is generally directly proportional to the mobility of the carriers in the channel. Thus, by increasing the mobility of the carriers in the channel, the operation speed of the transistor can be increased. Also, mechanical stresses within a semiconductor device substrate can modulate device performance by, for example, increasing the

mobility of the carriers in the semiconductor device. That is, stresses within a semiconductor device are known to enhance semiconductor device characteristics.

Thus, to improve the characteristics of a semiconductor device, tensile and/or compressive stresses are created in the channel of the n-type devices (e.g., NFETs) and/or p-type devices (e.g., PFETs). However, the same stress component, for example tensile stress or compressive stress, improves the device characteristics of one type of device (i.e., n-type device or p-type device) while discriminatively affecting the characteristics of the other type device. By way of example, a tensile stress will improve the performance of an NFET and a compressive force will improve the performance of a PFET. Thus, in order to maximize the performance of both NFETs and PFETs within integrated circuit (IC) devices, the stress components should be engineered and applied differently for NFETs and PFETs.

To selectively create tensile stress in an NFET and compressive stress in a PFET, distinctive processes and different combinations of materials are used. For example, a trench isolation structure has been proposed for forming the appropriate stresses in the NFETs and PFETs, respectively. When this method is used, the isolation region for the NFET device contains a first isolation material which applies a first type of mechanical stress on the NFET device in a longitudinal direction (parallel to the direction of current flow) and in a transverse direction (perpendicular to the direction of current flow). Further, a first isolation region and a second isolation region are provided for the PFET and each of the isolation regions of the PFET device applies a unique mechanical stress on the PFET device in the transverse and longitudinal directions.

Alternatively, methods have been proposed for providing a single strain layer on the entire device, using two lithography masks for patterning. By way of one illustrative example, a single nitride layer with a first stress component is placed over the entire structure, e.g., NFET and PFET, after silicidation. In the example discussed herein, the first nitride layer imposes a tensile component within the channel of the NFET. An oxide hard mask is then deposited over the nitride layer, and a photo resist is placed over one of the transistors, e.g., NFET. A reactive ion etching (RIE) is then performed to remove the hard mask over the PFET and the remaining photo resist over the NFET. A nitride etch is then performed to remove the nitride layer over the PFET.

A nitride layer with a compressive component is then placed over the PFET and the hard mask over the NFET, across a trench isolation structure (STI). This nitride layer will impose a compressive component in the PFET to enhance device performance. A photo resist is then deposited over the nitride layer of the PFET and across the STI. This photo resist also overlaps the tensile nitride layer of the NFET, taking into consideration only the vertical edge of the first nitride layer during the mapping process. A nitrogen etching process is then performed, which etches away the compressive nitrogen layer over portions of the NFET.

However, due to normal alignment errors of the patterning process, e.g., placement of the photoresist and difficulties controlling the etching, an overlap of the nitride layers is formed near the boundary of the compressive nitride layer and the tensile nitride layer. Namely, the compressive nitride layer remains over portions of the hard mask and the tensile nitride layer over a gate poly and the STI, resulting in

three layers of material. These overlaps result in subsequent etching difficulties at this overlap region.

These same alignment errors can also cause gaps between the nitride layers; however, such a gap is not very desirable because metal ions such as Cu can diffuse into silicon from back-end-of-the-line process. Thus, it is very important to ensure that there are no gaps. To guarantee that there are no gaps, further compensations are made in the etching process so that the nitride layers fill any gaps. Although such compensation ensures that the nitride layers will prevent such out diffusing, a larger overlap can occur.

In further processing steps, an oxide layer is deposited over the nitride layers, and vias are then etched into the oxide layer. A metal is then placed in the vias to create via contacts to the source and drain regions of the device. However, etching becomes very difficult due to the variations in layer thickness, especially at the overlap of the nitride layers. For example, etching in the overlap region (i.e., over the nitride layers and the hard mask layer) to make contact with the device results in over etching of the remaining portions of the device. On the other hand, etching designed for the portions of the device with one or two layers will result in an under etch of the overlap region. This under etch will result in a layer blocking contact between the device and the contact. (Figure 1).

While these methods do provide structures that have tensile stresses being applied to the NFET device and compressive stresses being applied to the PFET device, they may require additional materials and/or more complex processing, and thus, resulting in higher cost. Further, due to the inaccuracies of the etching processes,

an under etch or over etch can result in portions of the device. In the case of under etching in the overlap region, the contact will be blocked from contacting the device.

SUMMARY OF THE INVENTION

According to one embodiment of the invention, there is provided a method for manufacturing a device includes mapping extreme vertical boundary conditions of a mask layer based on vertical edges of a deposited first layer and a second layer. The mask layer is deposited over portions of the second layer based on the mapping step. The exposed area of the second layer is etched to form a smooth boundary between the first layer and the second layer. The resist layer is stripped.

According to another embodiment of the invention, there is provided the method includes depositing a first strain layer over a first device and depositing a second strain layer over a second device and a portion of the first strain layer. A mask layer is deposited over portions of the second strain layer, where an edge of the mask layer will not exceed extreme vertical boundary conditions measured from vertical edges of the first strain layer and the second strain layer. The exposed areas of the second strain layer are etched to form a smooth boundary between the first strain layer and the second strain layer. The mask layer is then stripped.

In one aspect of the invention, a semiconductor device comprises a semiconductor substrate having at least one p-type device and one n-type device. A first strain layer imposes a compressive stress in the p-type device and a second strain layer imposes a tensile stress in the n-type device. A smooth boundary is provided

between the first strain layer and the second strain layer. A dielectric layer is deposited over the first strain layer and the second strain layer, including the smooth boundary. At least one via contact is formed in the dielectric layer and connects to one of the n-type device and p-type device at the smooth boundary, wherein one of the at least one via contact is in contact with the first strain layer and the second strain layer, and wherein the smooth boundary is devoid of overlaps.

In another aspect of the invention, there is provided a semiconductor device, comprising: a semiconductor substrate having at least one p-type device and one n-type device; a first strain layer imposing a compressive stress in the p-type device; a second strain layer imposing a tensile stress in the n-type device; a smooth boundary provided between the first strain layer and the second strain layer; a dielectric layer deposited over the first strain layer and the second strain layer, including the smooth boundary; and at least one via contact formed in the dielectric layer and connecting to one of the n-type device and p-type device at the smooth boundary, wherein one of the at least one via contact is in contact with the first strain layer and the second strain layer, and wherein the smooth boundary is defined as abutting ends of the first strain layer and the second strain layer.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 illustrates a conventional structure;

Figure 2 illustrates a beginning structure for forming stress components for a p-type transistor and n-type transistor according to the invention;

Figures 3-8 illustrate exemplary processes for forming stress components for a p-type transistor and n-type transistor according to the invention;

Figure 9 illustrates boundary conditions for a resist pattern according to the invention;

Figures 10 and 11 illustrate an exemplary process using one boundary condition according to the invention;

Figure 12 illustrates an another boundary condition according to the invention;

Figures 13 and 14 illustrate an exemplary process using the boundary condition of Figure 12;

Figures 15 and 16 illustrate end processes for forming stress components for a p-type transistor and n-type transistor using the boundary conditions of either Figures 10-11 or Figures 12-13 according to the invention; and

Figure 17 shows a cross-section of a semiconductor substrate according to the invention using a scanning electron microscope.

DETAILED DESCRIPTION OF EMBODIMENTS OF THE INVENTION

The invention provides a method for fabricating devices with improved performance characteristics. In one aspect of the invention, a smooth boundary is formed between two films or layers, i.e., a layer that imposes a tensile component in an NFET and a layer that imposes a compressive component in a PFET. The smooth boundary does not have gaps or overlaps between the layers. The smooth boundary of the tensile and compressive films is also critical to improved product yield.

To form a smooth boundary between two stain layers, a resist pattern is aligned to a vertical portion of the second layer, e.g., Si_3N_4 , so that a minimum overlap overlay condition of the resist is aligned to the outer surface of the vertical portion of the second nitride layer. Then, an isotopic etch process is applied to remove the second nitride layer from the exposed surface and some or all of a vertical portion of the second nitride layer that is covered by the resist. In one implementation, the second layer is aligned to the first layer pattern to provide the smallest overlap possible.

Figure 2 illustrates a beginning structure for forming stress components for a p-type transistor and n-type transistor according to the invention. In Figure 2, a PFET 100 and NFET 200 are formed in a conventional manner in a substrate 102, such as silicon. A gate polysilicon 104 is formed over a gate oxide 106 on the substrate 102. Source and drain regions 108 and 110 are formed in the substrate 102 using known dopants such as arsenic, for example. An oxide spacer 112 is formed on sides of the gate polysilicon 104, with nitride spacers 114 formed on the oxide spacers 112. A silicide 116 is formed on the exposed portions of the substrate 102 and on the top of the gate polysilicon 104. An STI region 118 is formed between the PFET 100 and NFET 200.

In Figure 3, a first layer 120 such as, for example, a nitride layer, is formed over the structure of Figure 2. In the exemplary illustration of Figure 2, the first nitride layer 120 generates a tensile stress in the NFET channel in order to enhance the performance of the NFET 200. Those of skill in the art should recognize, though, that the first nitride layer 120 might generate a compressive stress to enhance the performance of the PFET. In this latter scenario, a tensile nitride layer would then be deposited to enhance the performance of the NFET. These layers will be termed hereinafter “tensile” and “compressive” for sake of convenience. In one application using a current 248nm lithographic tool, the first nitride layer is approximately 75nm with very good conformality. An oxide hard mask 122 is deposited over the first nitride layer 120.

Figure 4 illustrates an exemplary process for forming a photoresist mask 123 on the oxide hard mask 122, over the NFET 200. In this exemplary illustration, the first nitride layer 120 is a tensile nitride layer and the photoresist mask 123 will

protect the tensile nitride layer during subsequent etching process. However, in the event that the first nitride layer 120 is a compressive nitride layer, the photoresist mask 123 would then be placed over the PFET to protect the compressive nitride layer during subsequent etching process.

Figures 5-7 illustrate additional processing steps. Figure 5 illustrates an oxide etching process in which the oxide hard mask 122 is etched or removed from the PFET. In Figure 6, the photo resist mask 123 is stripped to expose the underlying oxide hard mask 122, over the NFET. Figure 7 illustrates a nitride etch to strip the nitride over the PFET 100. The nitride etch will stop at the silicide layer 116. These processes can equally be used for a compressive nitride layer provided over the PFET, during the initial processing stages.

Figure 8 illustrates the deposition of a second nitride layer 124. In this illustration, the second nitride layer 124 is a compressive nitride layer deposited after the first nitride layer 120 is patterned. In the illustration shown, the thickness of the second nitride layer 124 is approximately 75nm with very good conformality. The width of the vertical portion of the second nitride layer 124 is similar to the maximum overlap size, e.g., approximately 70 to 75nm. In embodiments, vertical film thickness is in a range of alignment error $\pm 50\text{nm}$. As discussed in more detail below, the oxide layer 122 will act as an etch stop during the second nitride etching process.

Figure 9 illustrates extreme vertical boundary conditions for a resist pattern according to the invention. These extreme boundary conditions are used to map the edges of the resist layer and to ensure a smooth boundary region between the first nitride layer 120 and the second nitride layer 124 after etching. As should be

understood, though, edge conditions within the extreme edge conditions can be used in accordance with the invention to achieve the smooth boundary layer between the nitride layers.

In the example of Figure 9, a resist layer 126 is formed over the second nitride layer 124. In designing or mapping this resist layer 126, two considerations are taken in account during the design process: (i) the edge 120' of the first nitride layer 120 and (ii) the vertical edge 124' of the second nitride layer 124. The distance between the vertical edges 120' and 124' is considered the inner and outer tolerances of the mask layer 126. In 90nm or 65nm technology, the overlay tolerance is approximately 40nm, so the maximum overlap of the photo resist is approximately 80nm, including the vertical portion of the second nitride layer 124. The 80nm dimension provides a slight overlap with the edge of the first nitride layer 120. These extreme vertical edge conditions can be adjusted depending on other technologies or other considerations, as should be understood by those of skill in the art.

Figures 10 and 11 illustrate the process of providing a smooth boundary between the first nitride layer 120 and the second nitride layer 124, using the example of the extreme outer edge 124'. In the process steps of Figure 10, an isotropic Si_3N_4 RIE process is used to remove the second nitride layer 124 in the photo resist 126 opening, as well as laterally below the photo resist 126. During this RIE, the oxide layer 122 acts as an etch stop to protect the edge of the first nitride layer 120. Figure 11 illustrates the removal or stripping of the photo resist 126. As shown, these process steps result in a smooth boundary between the first nitride layer 120 and the second nitride layer 124, e.g., no overlap.

Figures 13 and 14 illustrate the process of providing a smooth boundary between the first nitride layer 120 and the second nitride layer 124, using the example of the extreme inner edge 120' shown in Figure 12. In the process steps of Figure 13, an isotropic RIE process is used to remove the second nitride layer 124 in the photo resist 126 opening. Similar to that described with reference to Figure 10, during this RIE, the oxide layer 122 acts as an etch stop to protect the edge of the first nitride layer 120. Figure 14 illustrates the removal or stripping of the photo resist. As shown, these process steps result in a smooth boundary between the first nitride layer 120 and the second nitride layer 124, e.g., no overlap.

Figures 15 and 16 show end processes for forming the contacts. In Figure 15, an inter level dielectric 128 is formed over the nitride layers 120 and 124. The inter level dielectric 128 may be a deposited TEOS, BPSG or low K dielectric material. The interlevel dielectric 128 is then planarized using, for example, a chemical or mechanical polishing process. As seen in the illustration of Figure 16, a contact via with a metallization formed therein, generally represented as reference numeral 130, is then formed in the interlevel dielectric 128. In the processes described herein, since there is a smooth boundary between the nitride layers 120 and 124, over or under etching is no longer problematic and the metallization properly makes contact with the device.

Figure 17 shows a cross-section of a semiconductor substrate, manufactured in accordance with the invention, using a scanning electron microscope. As shown in this illustration, a smooth boundary layer is provided between the nitride layers 120 and 124. That is, the smooth boundary layer is formed as abutting ends of the nitride layers 120 and 124.

In the invention, the NFET and PFET devices are enhanced simultaneously using dual silicon nitride liners. In the invention, the smooth boundary between the nitride films will not block the contact to the NFET or PFET. Also, due to the strain engineering, a gap is not formed and metal ions will not diffuse into the silicon from BEOL.

While the invention has been described in terms of embodiments, those skilled in the art will recognize that the invention can be practiced with modification within the spirit and scope of the appended claims.

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:
 - a semiconductor substrate having at least one p-type device and one n-type device;
 - a first strain layer imposing a compressive stress in the p-type device;
 - a second strain layer imposing a tensile stress in the n-type device;
 - a smooth boundary provided between the first strain layer and the second strain layer;
 - a dielectric layer deposited over the first strain layer and the second strain layer, including the smooth boundary; and
 - at least one via contact formed in the dielectric layer and connecting to one of the n-type device and p-type device at the smooth boundary,
 - wherein one of the at least one via contact is in contact with the first strain layer and the second strain layer, and
 - wherein the smooth boundary is devoid of overlaps.
2. The device of claim 1 wherein the smooth boundary is devoid of gaps.
3. The device of claim 1 wherein the at least one via contact is plural via contacts, the plural via contacts contacting the n-type device and p-type device at the smooth boundary and at locations other than the smooth boundary.

4. A semiconductor device, comprising:
- a semiconductor substrate having at least one p-type device and one n-type device;
 - a first strain layer imposing a compressive stress in the p-type device;
 - a second strain layer imposing a tensile stress in the n-type device;
 - a smooth boundary provided between the first strain layer and the second strain layer;
 - a dielectric layer deposited over the first strain layer and the second strain layer, including the smooth boundary; and
 - at least one via contact formed in the dielectric layer and connecting to one of the n-type device and p-type device at the smooth boundary,
- wherein one of the at least one via contact is in contact with the first strain layer and the second strain layer, and
- wherein the smooth boundary is defined as abutting ends of the first strain layer and the second strain layer.