

ABSTRACT

In a semiconductor memory device 10, the maximum counter value in a carry-up unit 111 of an address counter 110 is set to 128 bits when an access request is for writing data to a memory array 100. On the other hand, in the semiconductor memory device 10, if the access request is for reading data from the memory array 100, the maximum counter value in the carry-up unit 111 of the address counter 110 is set to 256 bits.

10 The result is that it is possible to reduce the circuit structure required for specifying the desired address in an EEPROM array 101 and a masked ROM array 102.