A METHOD OF SUBSTRATE MANUFACTURE THAT DECREASES THE PACKAGE RESISTANCE

FIELD

[0001] Integrated circuit packaging.

BACKGROUND

[0002] Integrated circuits in the form of a chip or die are typically enclosed by a package that is mounted to a printed circuit board. The package has a number of external contacts on, for example, a land side of a package substrate that are connected to the printed circuit board and dedicated to the various power, ground and signal pins of the integrated circuit. Typical techniques for connecting contacts of a package with contacts of a printed circuit board include solder ball, pin, and socket techniques. In a situation where the contacts are not formed by solder balls that are attached to conductive contacts or lands of the package substrate, a typical package reference is as a land grid array (LGA) package.

[0003] A package substrate typically has internal routing layers which connect external lands to contacts on an opposite side of the substrate package that are connected to the integrated circuit chip or die. An internal routing layer typically contains separate layers for a ground bus, a power bus and a plurality of signal lines. The various layers are connected to the external lands by vias that extend through the substrate.

[0004] In general, the amount of current required of a die determines a performance of the die. If package resistance is high, current flow in the package will be reduced and the package and die will require more power. If resistance is low, the integrated circuit die can function at a lower power (e.g., 1.3 to 1.5 volts). Thus, one objective is to develop a low resistivity package.

[0005] As noted above, a package substrate has multiple conductive layers and power dissipation with respect to these layers is generally minimal. Most of the

power dissipation of a substrate package occurs at the contacts or lands. Thus, in one sense, the lands determine the overall resistivity of the package substrate.

[0006] According to a current process, the external conductive lands of a package substrate are copper coated structures. For example, a copper contact formed in the substrate package is coated with a layer of nickel, followed by a coating of palladium, followed by a coating of gold.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] **Figure 1** shows a computer system including microprocessor enclosed by a package mounted to a printed circuit board.

[0008] **Figure 2** shows a schematic cross-sectional side view of a land on a package substrate.

[0009] **Figure 3** shows a flow chart for forming coating layers on a land of a package substrate.

DETAILED DESCRIPTION

[0010] **Figure 1** shows a cross-sectional side view of an integrated circuit package that is physically and electrically connected to a printed wiring board or printed circuit board (PCB) to form an electronic assembly. The electronic assembly can be part of an electronic system such as a computer (e.g., desktop, laptop, handheld, server, etc.), wireless communication device (e.g., cellular phone, cordless phone, pager, etc.), computer-related peripheral (e.g., printer, scanner, monitor, etc.), entertainment device (e.g., television, radio, stereo, tapes and compact disc player, video cassette recorder, motion picture expert group audio layer 3 player (MP3), etc.), and the like. **Figure 1** illustrates the electronic assembly as part of a desktop computer. **Figure 1** shows electronic assembly 100 including die 110, physically

and electrically connected to package substrate 120. Die 110 is an integrated circuit die, such as a microprocessor die, having, for example, transistor structures interconnected or connected to power/ground or input/output signals external to the die through interconnect lines to contacts 130 on an external surface of die 110. Contacts 130 may be aligned with contacts 140 making up, for example, a die bump layer on an external surface of package substrate 120. On a surface of package substrate 120 opposite a surface including contacts 140 are land contacts 150. Connected to each of land contacts 150 are solder bumps 160 that may be used to connect package 170 to circuit board 180, such as a motherboard or other circuit board.

[0011] **Figure 2** shows an example of one of the land contacts of the package substrate of **Figure 1**. **Figure 3** describes a representative process flow for forming coating layers on a contact. Referring to **Figure 2**, package substrate 120 includes land contacts 150 each of which includes contact 210 formed in or on package substrate 120 as a contact point. Contact 210 has a number of coating layers overlying a surface (a top surface as viewed). In one embodiment, contact 210 is an electrically conductive material such as copper or an alloy of copper. Contact 210 may be separated by adjacent contacts on package substrate 120 through a dielectric material, such as a polymer (e.g., polyimide) material.

[0012] Overlying a surface of contact 210 (a top surface as viewed) is first coating layer 220. In an embodiment where contact 210 is a copper material, first coating layer 220 is a nickel material formed. Referring to the process flow in **Figure 3**, process 300 includes depositing a first coating layer such as a nickel material on a land contact of a package substrate, such as land contact 210 of package substrate 120 (block 310). One technique for depositing a first coating layer of a nickel material onto a contact of a copper material is through an electroless deposition process.

[0013] Overlying first coating layer 220 in the structure of **Figure 2** is layer 230. Layer 230 is selected, in one embodiment, of a material of gold. The process flow described in **Figure 3** includes depositing a first gold layer on the first coating layer

(block 320). One technique for depositing a gold material is through an electroplating process.

[0014] Overlying layer 230 in the structure shown in **Figure 2** is layer 240 of, in one embodiment, a palladium material. Process 300 of **Figure 3** includes depositing palladium layer on first gold layer (block 330). In one embodiment, palladium is deposited through an electroplating process.

[0015] The depositing of palladium is followed by a deposition of a second gold layer (block 340, **Figure 3**). In one embodiment, the second gold layer is deposited by an electroplating process. **Figure 2** shows overlying layer 250 of a material of gold overlying layer 240. Thus, the structure shown in **Figure 2** includes layer 240 sandwiched or disposed between layer 230 and layer 250 of a material of gold.

[0016] In one embodiment, a coating of nickel (Ni)/gold (Au)/palladium (Pd) is deposited to the following thicknesses: Ni 5.6 microns; Au 0.025 micron; Pd 0.08 micron; Au 0.06 micron. A total thickness of the composite coating in this example, is 5.75 microns. If this composite coating is compared to a prior art coating utilizing 5.6 microns nickel, 0.8 microns palladium, and 0.6 micron gold for a composite thickness of 5.73 microns, a prediction on a resistance of the composite stacks would be the stack with the additional gold layer would have a higher resistance as a thicker stack. However, although an overall resistance might be predicted to be higher, it has been found that an electronic structure (e.g., a work function) of the metal is such that tunneling of electrons through the composite stack is easier when the palladium material is sandwiched between gold layers as described.

[0017] In the preceding detailed description, reference is made to specific embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the following claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than a restrictive sense.

What is claimed is:

1. A method comprising:

forming a coating on a land contact of a package substrate configured to connect to a circuit die, the land contact comprising copper, the coating comprising a first material disposed between a first layer and a second layer, and each of the first layer and the second layer being made of a second material comprising gold.

2. A method comprising:

forming a first coating on a land contact of a package substrate, the land contact comprising copper; and

forming a second coating on the land contact comprising a first material disposed between a first layer and a second layer, each of the first layer and the second layer being made of a second material comprising gold.

3. The method of claim 2, wherein the first coating comprises nickel.

4. The method of claim 2, wherein the first material comprises palladium and the coating is a second coating, the method further comprising:

prior to forming the second coating, forming a first coating comprising nickel.

5. The method of claim 2, wherein forming a first coating comprises electrodepositing the first layer and the second layer.

6. The method of claim 5, wherein electrodepositing comprising electroplating.

7. An apparatus comprising:

a package substrate configured to connect to a circuit die, the package substrate comprising a plurality of land contacts comprising copper, wherein each of the plurality of land contacts comprises a first coating and a second coating, the second coating comprising a first material disposed between a first layer and a second layer, and wherein the first coating is disposed between the second coating and the land contact each of the first layer and the second layer being made of a second material comprising gold.

8. The apparatus of claim 7, wherein the first coating comprises nickel.

9. The apparatus of claim 7, wherein the first material comprises palladium.

10. The apparatus of claim 7, wherein the plurality of contacts comprise a first plurality of contacts on a first side of the package substrate, the package substrate further comprises a plurality of second contacts on a second opposite side of the package substrate, the apparatus further comprising:

a chip coupled to the plurality of second contacts.

11. A system comprising:

a computing device comprising:

a microprocessor;

a printed circuit board; and

a substrate, wherein the microprocessor is coupled to the printed circuit board through the substrate, the substrate comprising a plurality of land contacts comprising copper, wherein each of the plurality of land contacts comprises a first coating and a second coating, the second coating comprising a first material disposed between a first layer and a second layer, and wherein the first coating is disposed between the second coating and the land contact each of the first layer and the second layer being made of a second material comprising gold.

12. The system of claim 11, wherein the first coating comprises nickel.

13. The system of claim 12, wherein the first material comprises palladium.