

PATENT SPECIFICATION

DRAWINGS ATTACHED

1.197.154



1.197.154

Date of Application and filing Complete Specification: 26 March, 1969.

No. 15764/69.

Application made in United States of America (No. 720128) on 10 April, 1968.

Complete Specification Published: 1 July, 1970.

Index at acceptance: —H1 K(211, 21Y, 217, 22Y, 223, 238, 422, 474, 482, 507, 511, 51Y, 522, 523, 54Y, 55Y, 551, 555 563, 566, 581, 594, 595, 61Y, 618, 650)

International Classification: —H 01 c 7/14; H 01 I 19/00

COMPLETE SPECIFICATION

High Voltage Transient Protection for an Insulated Gate Field Effect Transistor

We, RCA CORPORATION (formerly Radio Corporation of America), a corporation organised under the laws of the State of Delaware, United States of America, of 30 Rockefeller Plaza, City and State of New York, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

The present device comprises an insulated gate field effect transistor which is protected against overvoltage, and allows operation of the device with gate voltages of both polarities, by back-to-back diodes connected between its gate electrode and its substrate. The back-to-back diodes are formed by a pair of similar spaced regions within a single region in the transistor substrate.

In the accompanying drawings:—

Figure 1 is a schematic diagram of the equivalent circuit of the present novel transistor;

Figure 2 is a plan view of a preferred layout for the present novel transistor;

Figure 3 is an enlarged partial cross sectional view taken on the line 3—3 of Figure 2; and

Figure 4 is an enlarged partial cross sectional view taken on the line 4—4 of Figure 2.

Figure 1 illustrates in schematic form the electrical equivalent circuit of the present novel transistor. The circuit, indicated generally by the reference numerals 10, includes an insulated gate field effect transistor 12 which has a source terminal 14, a drain terminal 16, a substrate terminal 18 and a

gate terminal 20. In the circuit 10, the substrate terminal 18 is connected to the material of the substrate by a lead 19 and the gate terminal 20 is connected to a gate electrode 21 by a lead 22.

Structurally, the gate electrode 21 of the transistor 12 is separated from the substrate of the transistor by a thin insulating layer, ordinarily composed of silicon dioxide. This material has a breakdown strength of about 10^7 v/cm.

To protect the gate insulating material of the transistor 12 against breakdown due to high gate voltages, the gate electrode 21 is connected to the substrate through a pair of diodes connected in back-to-back relation. Thus, there is one diode 24 and another diode 26 connected in cathode-to-cathode opposed series relation between a terminal 28 on the gate lead 22 and a terminal 30 on the substrate lead 19.

The transistor 12 in Figure 1 has an N type channel, in this example. Enhancement mode operation results from the application of positive voltage on the gate electrode 21 and depletion mode operation results from negative voltage thereon. In each mode, one or the other of the diodes 24 and 26 will be reverse biased. For example, if the diodes have anodes of P+ type material and cathodes of N type material, the diode 24 will be forward biased but the diode 26 will be reverse biased under enhancement conditions of positive gate voltage. If the gate voltage exceeds the breakdown voltage of the diode 26, current will flow to the substrate. The diode 26 thus limits the positive voltage which can be applied across the gate insulator of the transistor 12.

[Price 5s. 0d. (25p)]

10 The situation is reversed for negative voltages on the gate electrode 21. Under these circumstances, the diode 24 is reverse biased while the diode 26 is forward biased. If the voltage on the gate electrode 21 exceeds the breakdown voltage of the diode 24, current again will flow in the circuit between the gate electrode 21 and the substrate, with the result that a limit is established for the amount of negative voltage which can be applied across the gate insulator of the transistor 12.

15 A preferred structure for the transistor 12 and the diode protection for its gate insulator is illustrated in Figures 2 to 4. The transistor 12 is fabricated by known diffusion and photolithographic processes in a substrate body 40 of semiconductive material which is of p type conductivity in this example. The transistor 12 has a channel region 43 adjacent to a surface 42 thereon. The length of the channel region 43 is determined by a pair of spaced source and drain regions. The source region is constituted by a highly doped N+ region 44, near the right side of the structure in Figure 3 adjacent to the surface 42 of the substrate 40, and an N type region 46 adjacent to the surface 42 between the N+ type region 44 and the channel region 43. The drain region is similarly constituted at the left side of Figure 3 by an N+ type region 48 and an N type region 50. The purpose of the N+ type regions 44 and 48 is to facilitate ohmic contact to the device, and the purpose of the N type regions 46 and 50 is to establish ohmic contact from the regions 44 and 48 to the channel 43 while keeping the doping level relatively low adjacent to the channel. A more stable operating characteristic is achieved by this expedient.

40 A layer of insulating material 52 is disposed on the surface 42 of the substrate 40. The insulating layer 52 has openings, indicated at 53 and 54, which are coincident with the N+ type regions 44 and 48 for receiving a metal source electrode 55 and a metal drain electrode 56, respectively. The source electrode 55 extends to a source bonding pad 58, disposed on the insulating layer 52, to which a wire may be bonded to connect the source electrode 55 to external circuitry. A wire may be bonded directly in the drain electrode 56, which is relatively large in area. See Figure 2.

55 Adjacent to the channel 43, the insulating layer 52 has a thinner portion 59 which is the active gate insulator of the device. A gate electrode 21 is disposed on the thinner portion 59 of the insulating layer 52 and extends in parallel relation to the source and drain electrodes 55 and 56, as shown in Figure 2, and terminates in a gate bonding pad 60. The thinner region 58 of the insulating layer 52 may be about 1000 Å thick and will withstand voltage differences between the gate

electrode 21 and the substrate 40 of up to about 100 volts without breaking down.

Figure 4 illustrates the structure of the back-to-back diodes 24 and 26. As shown in Figure 4, the gate bonding pad 60 overlies a portion of a diffused N type region 62 on the substrate 40 adjacent to the surface 42. This region acts as a cathode region for both of the diodes 24 and 26. A P+ type diffused region 64 surrounds the N type region 62, in spaced relation from the periphery thereof, and acts as a guard ring to isolate the N type region 62 from the other N type active regions of the device.

The anodes of the diodes 24 and 26 are constituted by diffused P+ type regions 66 and 68 which are formed within the region 62 adjacent to the surface 42. These regions have substantially the same area, depth, and doping profile so that, with the N type region 62, they form diodes having substantially the same electrical characteristics. The spacing between each of the P+ regions 66 and 68 and between them and the junction between the region 62 and the substrate 40 are made large enough so that PNP transistor action does not take place.

The gate bonding pad 60 is connected to the P+ type region 68 through an opening 70 in the insulating layer 52. The other P+ type region 66 is ohmically connected to the P type material of the substrate 40 by means of a metal connection 72 which extends into contact with the P+ type region 66 through an opening 74 in the insulating layer 52. The metal connection 72 extends beyond the periphery of the N type region 62 and through an opening 76 in the insulating layer 52 into contact with the P+ type region 64. This region thus serves to facilitate contact to the substrate 40 in addition to its guard ring function.

Because the N type region 62 is disposed below the gate bonding pad 60, the present device occupies about the same area as a device which has no diode protection. The placing of the diodes below a gate bonding pad is especially useful in an insulated gate field effect transistor which has more than one gate electrode and in which at least one gate bonding pad is completely surrounded by other elements, such as a source or a drain region, of the device. In such a transistor, a pair of diodes having a structure as described herein may be conveniently incorporated in the space below each of the bonding pads.

The structure described herein operates in the manner described above with respect to the circuit of Figure 1. The simultaneous formation of the regions 66 and 68 in the single region 62 so as to have substantially the same structural characteristics provides diodes which have equal electrical characteristics.

(11)

In the preferred embodiment described above, the substrate 40 is of P type conductivity and each diode of the pair has a P+, N structure. Such a structure may also be employed in a so-called P channel device as long as the N type common region is isolated from the N type material of the substrate thereof. Moreover, in both N channel and P channel devices, the diodes may be a pair of N+ type regions in a P type common region, with the reservation that the P type common region must be isolated from the P type material of the substrate of an N channel device. Isolation may be achieved, for example, by disposing the common region within an auxiliary region of conductivity type opposite to that of the substrate, thereby introducing a pair of back-to-back junctions between the common region and the substrate.

20 WHAT WE CLAIM IS:—

1. An improved insulated gate field effect transistor formed in a semiconductive substrate having a surface, a channel adjacent to said surface, a layer of insulating material on said surface, and at least one gate electrode disposed on said layer of insulating material in field-applying relation to said channel, wherein the improvement is characterized by: comprising back-to-back diode means for protecting said insulating material against breakdown due to high voltages of either positive or negative polarity on said gate electrode, said diode means comprising a first region in said substrate adjacent to said surface, second and third spaced regions within said first region adjacent to said surface and forming a pair of PN junctions therewith, first

conductive means connecting said gate electrode to one of said second and third regions, and second conductive means connecting the other of said second and third regions to said substrate.

2. An insulated gate field effect transistor as defined in claim 1 further comprising a bonding pad of relatively large area disposed on said layer of insulating material, said gate electrode being connected to said bonding pad and said first region being disposed below and adjacent to said bonding pad.

3. An insulated gate field effect transistor as defined in claim 1 wherein said second and third regions are substantially equal in area, depth of diffusion, and doping profile whereby said junctions have substantially the same electrical properties.

4. An insulated gate field effect transistor as defined in claim 1 wherein said substrate is of P type conductivity, said first region is of N type conductivity, and said second and third regions are of P+ type conductivity.

5. An insulated gate field effect transistor as defined in claim 4 further comprising a P+ type region in said substrate adjacent to said surface in surrounding relation to said N type first region.

6. An insulated gate field effect transistor as claimed in claim 1 and substantially as described with reference to the accompanying drawing.

For the Applicants,
MATTHEWS, HADDAN & CO.,
Chartered Patent Agents,
31—32, Bedford Street,
London, W.C.2.

In the preferred embodiment described above, the substrate 40 is of P type conductivity and each diode of the pair has a P+, N structure. Such a structure may also be employed in a so-called P channel device as long as the N type common region is isolated from the N type material of the substrate thereof. Moreover, in both N channel and P channel devices, the diodes may be a pair of N+ type regions in a P type common region, with the reservation that the P type common region must be isolated from the P type material of the substrate of an N channel device. Isolation may be achieved, for example, by disposing the common region within an auxiliary region of conductivity type opposite to that of the substrate, thereby introducing a pair of back-to-back junctions between the common region and the substrate.

20 WHAT WE CLAIM IS:—

1. An improved insulated gate field effect transistor formed in a semiconductive substrate having a surface, a channel adjacent to said surface, a layer of insulating material on said surface, and at least one gate electrode disposed on said layer of insulating material in field-applying relation to said channel, wherein the improvement is characterized by: comprising back-to-back diode means for protecting said insulating material against breakdown due to high voltages of either positive or negative polarity on said gate electrode, said diode means comprising a first region in said substrate adjacent to said surface, second and third spaced regions within said first region adjacent to said surface and forming a pair of PN junctions therewith, first

conductive means connecting said gate electrode to one of said second and third regions, and second conductive means connecting the other of said second and third regions to said substrate.

2. An insulated gate field effect transistor as defined in claim 1 further comprising a bonding pad of relatively large area disposed on said layer of insulating material, said gate electrode being connected to said bonding pad and said first region being disposed below and adjacent to said bonding pad.

3. An insulated gate field effect transistor as defined in claim 1 wherein said second and third regions are substantially equal in area, depth of diffusion, and doping profile whereby said junctions have substantially the same electrical properties.

4. An insulated gate field effect transistor as defined in claim 1 wherein said substrate is of P type conductivity, said first region is of N type conductivity, and said second and third regions are of P+ type conductivity.

5. An insulated gate field effect transistor as defined in claim 4 further comprising a P+ type region in said substrate adjacent to said surface in surrounding relation to said N type first region.

6. An insulated gate field effect transistor as claimed in claim 1 and substantially as described with reference to the accompanying drawing.

For the Applicants,
MATTHEWS, HADDAN & CO.,
Chartered Patent Agents,
31—32, Bedford Street,
London, W.C.2.

Printed for Her Majesty's Stationery Office by the Courier Press, Leamington Spa, 1970.
Published by The Patent Office, 25 Southampton Buildings London WC2A 1AY, from which copies may be obtained.

