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PATENT SPECIFICATION

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(54) IMPROVEMENTS IN OR RELATING TO
 AUTOMATIC POWER SUPPLY OPERATED RESETTING
 CIRCUITS FOR USE IN CONNECTION WITH
 ELECTRON TIMEPIECES, CALCULATORS AND
 OTHER DIGITAL APPARATUS

(71) We, KABUSHIKI KAISHA SUWA SEIKOSHA, a Japanese Company of 34, 4-chome, Ginza, Chuo-ku, Tokyo, Japan, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to automatic power supply operated re-setting circuits (these are usually called "Power-on-Reset" (POR) circuits, though they are also known as "Power-on-clear circuits") which, on the supply of operating power automatically reset or clear flip-flop memory or other circuits in a digital apparatus to which a POR circuit is fitted. A POR circuit ensures that the digital apparatus to which it is fitted starts operating correctly when power is switched on. Were it not for a POR circuit, digital apparatus would be liable to display a meaningless figure or character or combination thereof when power is first supplied to it. This is not only a defect from the user's point of view since it tends to make him think the apparatus is out of order, but is also a serious defect from the manufacturing viewpoint because it increases difficulty of a time spent in examining and testing the functioning of digital apparatus at the factory.

The invention seeks to provide improved simple and reliable POR circuits which lend themselves to embodiment in integrated circuit (IC) and monolithic construction and may therefore be made very small and compact. The achievement of this object makes the invention particularly advantageously applicable to POR circuits in electronic timepieces (and especially electronic watches, since there is so little space available in such watches) and pocket or table digital calculators, though the invention is not limited to its application to these particular digital devices.

Hitherto conventional digital electronic apparatus, such for example, as digital electronic timepieces, using in their circuitry semiconductor integrated circuits monolithically constituted by complementary field effect transistors (C-MOS-FET) incorporated in a C-MOS structure and arranged to occupy a minimum of space, have not usually been provided with means for resetting the whole circuitry automatically at the time power is switched on. As a result (as already stated) factory testing and inspection takes an undesirably long time and this makes for increased cost, and also users, when they switch on, are apt to think the apparatus is out of order, which is a nuisance. The main reason why POR circuits have in general, not been fitted to digital apparatus of the foregoing nature is that known POR circuits cannot be readily incorporated into semiconductor integrated circuits monolithically constituted with C-MOS transistors. An important object of this invention is to overcome this difficulty.

According to this invention there is provided, in a digital apparatus employing in its circuitry MOS field transistors in a semiconductor integrated structure, a power-on-reset circuit (POR) which is included in the integrated circuit structure and which utilises parasitic capacitance in that part of the POR circuit which detects change of voltage in the power supply voltage and produces therefrom a re-setting pulse when power is applied said POR circuit including an inverter comprising two field effect transistors of opposite conductivity types and having a common drain connection and a common gate connection, a normally open switch connected at one end to the common gate connection and at the other to a first terminal to which one potential is applied and from which potential is applied to the source of one transistor, a connecting

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circuit between said other end of said switch and a second terminal to which another potential is applied and from which potential is applied to said source of said second transistor, capacitance including that of a condenser and stray capacitance across it, connected between said second terminal and said common drain connection and a connection for taking off a POR re-setting pulse from said common drain connection, the whole circuit being so dimensioned that the total capacitance between said common drain connection and said first terminal is small in relation to that between said common drain connections and said second terminal.

Said connecting circuit may include a further field effect transistor with its source connected to the source of said second transistor, its drain connected to the common gate connection and its gate connected to said first terminal.

Said first terminal may be connected to the source of said one transistor through a resistance additional to that provided by said one transistor and said additional resistance may be provided by an additional field effect transistor.

Two additional transistors may be provided one in series between said first terminal and the source of said one transistor and the other in series between said second terminal and the source of said second transistor.

The invention is illustrated in and further explained in connection with the accompanying drawings, in which:—

Figure 1 is a theoretical circuit representative of the principle of a POR circuit,

Figures 3 and 5 illustrate diagrammatically two embodiments of the invention, and

Figures 2 and 4 are graphical Figures related to the operation of Figures 1 and 3 respectively.

In order automatically to bring a digital system to its correct initial state—i.e. the state in which it should be at the time power is switched on if it is to start working properly—it is necessary to generate a resetting pulse by utilizing a voltage level change which occurs at the instant power is first switched on, since the voltage level of the power supply after power is on is predetermined and fixed. The accompanying Figure 1 is a theoretical representation of a known POR circuit which does this. It comprises a series capacity-resistance (CR) circuit comprising a condenser C and a resistance r connected across another series circuit consisting of a power supply or voltage E₀ and a switch SW the said switch SW being one which is closed when the power is switched on. On closure of the

switch the voltage e across the RC circuit follows the (idealised) curve shown in the upper part of the accompanying Figure 2, while the voltage v exhibits a transient change as shown by the lower part of Figure 2 and is available for use as a re-setting pulse to re-set the digital apparatus with which the POR circuit is associated to its correct initial state. However, in the case of integrated circuitry, the process of resetting when power is switched on becomes complicated because of effects such as chatter and effects due to parasitic capacitance. If the change in the supply voltage e is taken as given by:—

$$e = -E_0 [1 - \exp(-t/\tau)] \quad (1)$$

where τ is the time constant of the fall of supply voltage on switching on and $E_0 > 0$, then, in order to satisfy the requirements of the POR circuit the change in v of the circuit of Figure 1 is given by:—

$$v = \frac{rc}{rc - \tau}$$

$$E_0 [\exp(-t/\tau) - \exp(-t/rc)] \quad (2)$$

where r and c are the values of the elements so referenced in Figure 1.

In order to obtain a pulse of sufficient width and amplitude to be satisfactory for use as the reset pulse, the

$$\tau < rc \quad (3)$$

must be satisfied.

If, however, a POR circuit is to be monolithically constructed, account must be taken of the fact that there will be substantial parasitic capacitance to earth or frame on both sides of the power source. Because of this, the relation which must be satisfied if a reliably functioning re-setting pulse is to be obtained becomes

$$C_p \ll (C_e + C_n) \quad (4)$$

where C_p is the parasitic capacitance on the side of the supply source connected to the resistance end of the series RC circuit and C_n is the parasitic capacitance on the other side of the supply. C_e is additional capacitance which, as will be seen later when the present invention comes to be described may be added in parallel with C_p. If C_n is not itself large enough substantially to satisfy equation (4). Additional capacitance C_e necessary substantially to satisfy equation (4) may be obtained in the process of forming the gate of a C-MOS. Once more anticipating the description of the invention, in carrying out the said invention the sum C_e + C_n may be only about

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10pF or so but, nevertheless, this capacitance, small as it is, is of great importance in securing good operation of the C-MOS POR circuit. The time constant τ is dependent on the product τC but to obtain a required time constant it is better to increase C rather than τ .

The requirements for a good C-MOS POR circuit in accordance with this invention are not difficult to satisfy. As regards self capacitance in a MOS IC the junction capacitance is the largest per unit area after the gate capacitance. The junction capacitance in an N type diffusion area is about twice the corresponding capacitance in a P type diffusion area. Therefore N type diffusion may be used, as far as possible, for the crossunders of the system reset circuit. By "crossunders" is meant the diffusion layer which can pass through the metallic wiring used for the mutual wiring in a C-MOS IC. Further, in the case of a C-MOS IC constituted by counters which are disposed in series and which are reset by the POR circuit—as is the case of the digital display of an electronic timepiece—the length of the wiring and the number of crossunders of the system reset circuit increase in proportion to the size of the IC. Accordingly, the larger the size of the integrated circuit the more advantageous is the utilization of parasitic capacitance.

Figure 3 shows one embodiment of the invention. Fundamentally the CR circuit in the POR circuit of Figure 3 could be represented by the theoretical circuit of Figure 1. Figure 4 shows response wave forms obtained with Figure 3. In Figure 3, however, the CR circuit is composed of r and the capacitance $(C_e + C_n)$. C_e is the additional capacitance already mentioned and which is added deliberately to satisfy expression (4) about the value of C_n alone is not enough to satisfy said expression. The resistance r (of Figure 1) includes the channel resistance of the transistor T_1 in Figure 3—it may be wholly constituted by it—and the resistance r (of Figure 3) and the two transistors T_1 and T_2 (together with the capacitances across the latter) provide the RC circuit r and C of the theoretical circuit of Figure 1. In order to obtain required resistance values the P channel transistor may be smaller than the N channel transistor. As will be seen the two transistors together form an inverter. The reset pulse voltage (v in Figure 1) appears between the re-set pulse terminal SSR and earth in Figure 3. The channel resistance of the MOS transistor R is provided for the falling gate potentials of the transistors T_1 and T_2 , which normally fall towards V_{ss} . Switch SW is for performing manual reset. Figure 4, the references in which correspond with the same reference in Figure 3, shows in its up-

per part the way in which V_{ss} changes when power is switched on and, in its lower part, the transient pulse, used for resetting, which is produced. The curves of Figure 4 are charging curves obtained in dependence on the volt/ampere characteristics of the MOS transistors and result in a somewhat greater reset pulse width than do the idealised curves of Figure 2.

Another embodiment of the invention is shown in Figure 5. This has two additional resistance providing CMOS transistors T_{11} and T_{14} providing series resistances of values r_{11} and r_{14} respectively, inserted at opposite ends of the inverter constituted by transistors T_1 , T_2 . The MOS resistance r_{11} has the effect of increasing the time constant $r_{11}(C_e + C_n)$ and helps to secure a good pulse width at SSR by its effect on the operating characteristic of the MOS transistor characteristic when the fall of voltage V_{ss} at the time power is switched on is small. It also improves matters if there is chatter having a fluctuation period of several nano seconds. The embodiment of Figure 5 can be used with considerable advantage in a case in which the power source which drives the digital system of for example a conventional liquid crystal display quartz crystal wristwatch comprises a main power source proper and a booster circuit driven by a pulse output generated from an oscillation circuit driven by said main power source, for example, a Cockcroft-Walton circuit. If the threshold voltage of the MOS resistance r_{11} is chosen higher than the main power source voltage, there is obtained a POR circuit of extremely good operating reliability, for, if this is done, the POR circuit and the associated circuitry may be regarded as, and are, in effect, driven by the said booster circuit. This is because there is an interval between the time the oscillation circuit receives power and the time it starts to oscillate and also an interval until the boosting voltage necessary for the booster circuit to bring the MOS resistance r_{11} on the ON state is supplied to the POR circuit, and the sum of these time intervals is much longer than the time required for the MOS transistor to operate.

The purpose of the MOS resistance r_{14} is to help balance the inverter and improve the signal/noise ratio.

As will now be seen, the effective use of parasitic capacitance such as wiring capacitance enables the invention to provide a very simple POR of high reliability. Various modifications of the embodiments illustrated are possible. For example, the embodiment of Figure 3 can be made more sure in operation by adding

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an external capacitor in parallel with the switch SW.

WHAT WE CLAIM IS:—

5 1. In a digital apparatus employing in its circuitry MOS field effect transistors in a semi-conductor integrated circuit structure, a power-on-reset circuit (POR) which is included in the integrated circuit structure and which utilises parasitic capacitance in that part of the POR circuit which detects change of voltage in the power supply voltage and produces therefrom a re-setting pulse when power is applied, said POR circuit including an inverter comprising two field effect transistors of opposite conductivity types and having a common drain connection and a common gate connection, a normally open switch connected at one end to the common gate connection and at the other to a first terminal to which one potential is applied and from which potential is applied to the source of one transistor, a connecting circuit between said other end of said switch and a second terminal to which another potential is applied and from which potential is applied to said source of said second transistor, capacitance including that of a condenser and stray capacitance across it connected between said second terminal and said common drain connection, and a connection for taking off a POR re-setting pulse from said common drain connection, the whole circuit being so dimensioned that the total capacitance between said common drain connection and said first terminal is small in relation to

that between said common drain connection and said second terminal.

2. Apparatus as claimed in Claim 1 wherein said connecting circuit includes a further field effect transistor with its source connected to the source of said second transistor, its drain connected to the common gate connection and its gate connected to said first terminal.

3. An apparatus as claimed in Claim 1 or 2 wherein said first terminal is connected to the source of said one transistor through a resistance additional to that provided by said one transistor.

4. An apparatus as claimed in Claim 3 wherein said additional resistance is provided by an additional field effect transistor.

5. An apparatus as claimed in Claim 1 or 2 wherein two additional transistors are provided one in series between said first terminal and the source of said one transistor and the other in series between said second terminal and the source of said second transistor.

6. POR circuits substantially as herein described with reference to Figures 3 and 5 of the accompanying drawings.

7. A digital electronic timepiece having a POR circuit as claimed in any of the preceding claims.

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structure, a power-on-reset circuit (POR)
which is included in the integrated circuit
10 structure and which utilises parasitic
capacitance in that part of the POR circuit
which detects change of voltage in the
power supply voltage and produces
therefrom a re-setting pulse when power is
15 applied, said POR circuit including an
inverter comprising two field effect
transistors of opposite conductivity types
and having a common drain connection and
a common gate connection, a normally
20 open switch connected at one end to the
common gate connection and at the other
to a first terminal to which one potential is
applied and from which potential is applied
to the source of one transistor, a connecting
25 circuit between said other end of said
switch and a second terminal to which
another potential is applied and from which
potential is applied to said source of said
second transistor, capacitance including
30 that of a condenser and stray capacitance
across it connected between said second
terminal and said common drain
connection, and a connection for taking off
a POR re-setting pulse from said common
35 drain connection, the whole circuit being
so dimensioned that the total capacitance
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