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PATENT SPECIFICATION

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COMPLETE SPECIFICATION

DRAWINGS ATTACHED

Semiconductor Device

WE, TEXAS INSTRUMENTS INCORPORATED, of 13500 North Central Expressway, Dallas, Texas, United States of America, a corporation organized and existing under the laws of the State of Delaware, United States of America, do hereby declare the invention, for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:

This invention relates to semiconductor devices.

Many methods and techniques for miniaturizing electronic circuits have been proposed in the past. At first, most of the effort was spent upon reducing the size of the components and packing them more closely together. Work directed toward reducing component size is still going on, but has nearly reached a limit. Other efforts have been made to reduce the size of electronic circuits, such as by eliminating the protective coverings from components, by using more or less conventional techniques to form the components of a complete circuit on a single substrate, and by providing the components with a uniform size and shape to permit closer spacings in the circuit packaging therefor.

All of these methods and techniques require a very large number and variety of operations in fabricating a complete circuit. For example, of all circuit components, resistors are usually considered the most simple to form, but when adapted for miniaturization by conventional techniques, fabrication requires at least the following steps:

a. Formation of the substrate
b. Preparation of the substrate
c. Application of terminations
d. Preparation of resistor material
e. Application of the resistor material
f. Heat treatment of the resistor material
g. Protection or stabilization of the resistor

Capacitors, transistors, and diodes, when adapted for miniaturization, each require at least as many steps in the fabrication thereof. Unfortunately, many of the steps required are not compatible. A treatment that is desirable for the protection of a resistor may damage another element formed on the same substrate, such as a capacitor or transistor, and as the size of the complete circuit is reduced, such conflicting treatments, or interactions, become of increasing importance. Interactions may be minimized by forming the components separately and then assembling them into a complete package, but the very act of assembly may cause damage to the more sensitive components.

Because of the large number of operations required, control over miniaturized circuit fabrication becomes very difficult. To illustrate, many raw materials must be evaluated and controlled, even though they may not be well understood. Further, many testing operations are required and, even though a high yield may be obtained for each operation, so many operations are required that the over-all yield is often quite low. In service, the reliability of a circuit produced by methods of such complexity may also be quite low due to the tremendous number of controls required. Additionally, the separate formation of individual components requires individual terminations for each component. These terminations may eventually become as small as a dot of conductive paint. However, they still account for a large fraction of the usable area or volume of the circuit, and may become an additional cause of

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circuit failure or rejection due to misalignment.

In contrast to the approaches to miniaturization that have been made in the past, the present invention has resulted from a new and totally different concept for miniaturization. Semiconductor network devices made in accordance with this concept are the subject matter of our co-pending patent application no. 3633/60 (Serial no. 945,734) and divisionals therefrom.

In the specification of our co-pending patent application aforesaid, a single crystal of semiconductor material exhibiting one type of conductivity, either N-type or P-type, has formed therein by diffusion a region or regions of appropriate conductivity type to form a P-N junction between such region or regions and the semiconductor crystal or as the case may be, between diffused regions. In our parent patent application no. 16071/60 (Serial no. 958,242), from which the present application is divided, all components of a semiconductor device are fabricated within a body of semiconductor material by adapting the techniques described in the specification of said co-pending patent application, together with certain other techniques. It is to be noted that all components of the device are originally formed into a single body of semiconductor material and constitute portions thereof.

The present invention is a semiconductor device comprising a single crystal semiconductor wafer including two or more first P-N junctions extending to and terminating at one and the same major wafer face to form two or more spaced discrete regions on, adjacent to said one major wafer face and spaced from the apposite major wafer face, two or more of said discrete regions being adapted to provide the electrical properties of circuit elements each including a second N-P junction extending to and terminating at said one major wafer face within one of said first P-N junctions, and said device further including ohmic contacts secured to said one major wafer face within each of said first P-N junctions and on each side of said second P-N junction.

The concept of shaping, described in detail in the specification of said co-pending application no. 3633/60 (Serial no. 945,734) makes it possible in a semiconductor device to obtain the necessary isolation between components and to define the components or, stated differently, to limit the area which is utilized for a given component. Shaping may be accomplished in a given semiconductor device in one or more of several different ways. These various ways include actual removal of portions of the semiconductor material, specialized configurations of the semiconductor material, such as rectangles, "L" shapes, "U" shapes, etc., selective conversion of intrinsic semiconductor material by diffusion of impurities therein to provide low resistivity paths for current flow, and selective conversion of semiconductor material of one conductivity type to conductivity of the opposite type wherein the P-N junction thereby formed acts as a barrier to current flow. In any event, the effect of shaping is to direct and/or confine paths for current flow, thus permitting the fabrication of circuits which could not otherwise be obtained in a single wafer or slice of semiconductor material. As a result, the final circuit is arranged in essentially planar form. It is possible to shape the wafer or slice during processing and to produce by diffusion the various circuit elements in a desired and proper relationship.

An embodiment of the invention will now be described, by way of example, with reference to the accompanying drawing, in which:

Fig. 1 illustrates a top plan view of a semiconductor device according to the invention; and

Fig. 2 illustrates a schematic diagram of the semiconductor device illustrated in Fig. 1.

This invention is primarily concerned with providing miniature electronic circuits. Also, as noted, the invention contemplates the use of a body or slice of semiconductor material appropriately shaped and having formed therein by diffusion P-N junctions and the use of components designed for the various circuit components which can be integrated into or which constitute parts of the aforesaid body or slice of semiconductor material.

Figs. 1-5, inclusive, of said co-pending application 3633/60 illustrate in detail semiconductor network elements which can be formed into a body of semiconductor material. It is noted at this point that the body of semiconductor material is of single crystal structure, and can be composed of any suitable semiconductor material. Examples of such suitable material are germanium, silicon, intermetallic alloys such as gallium arsenide, aluminum antimonide, indium antimonide, as well as others.

With reference to the accompanying drawing, there is shown a miniature semiconductor network which provides gated bistable multivibrator operation. Mounted on substrate 10 by solder glass are strips 12 and 14 of single crystal semiconductor material. The space 16 between these two strips was formed by originally starting with a single large strip of semiconductor

material and etching to divide the crystal into two portions. However, the purpose of this shaping operation is to provide isolation between the circuit components integrated with strips 12 and 14, and it is to be understood that substantial electrical isolation could be obtained by means other than etching completely through a larger crystal strip to form two strips; for example, electrical isolation could be provided by a high resistance area in the crystal between circuit components desired to isolate. This high resistance will provide a substantial open circuit to prevent undesired interference between the circuit components involved. However, in the embodiment shown in Figure 1, isolation between two portions of the multivibrator circuit is provided by etching the space 16 in an original crystal to form two crystal strips 12 and 14 which are physically separate, one from the other.

The original crystal has firstly formed therein over one entire surface thereof a layer formed by diffusion of acceptor impurity material to form a P-N junction. Circuit components are then formed therein by selective etching of the semiconductor material and by selectively diffusing donor material into the P layer. Metal contacts may then be plated or evaporated onto desired layers to form electrical connections.

Formed in strip 12 is transistor TR-2 of the NPN type with a second N region formed by diffusion in the P-type base to form in effect a two-emitter transistor. This double emitter structure actually provides one NPN transistor plus an integral diode formed by the additional diffused PN junction. TR-2 has an N-type collector region provided by the crystal strip 12, a P-type base region 20 and two N-type emitter regions 22 and 24. Ohmic contacts 26, 28, and 30 are plated or evaporated onto their corresponding semiconductor layers. Output lead 33 is soldered or alloyed to substrate 10, and extends beneath the left-hand end of strip 12 and makes ohmic contact therewith, and thereby also with the collector region of TR-2. Double emitter transistor TR-3 is identical with TR-2.

Contiguous with base region 20 is a strip 32 of P-type material formed by diffusion in strip 12 and formed in a tortuous path to define a cross-coupling resistor R_1 having a value of 7 kilohms (K). The left-half 34 of crystal strip 12, a portion of which underlies P-strip 32, defines a bias resistor R_2 having a value of 5K. An ohmic contact 36 is formed on the other end of P-strip 32 to provide means for electrically connecting this end of R_1 to the output lead 38. Resistance R_2 is connected to the bias lead 40 which is mounted on substrate 10 and passes beneath strip 12 into ohmic contact therewith. P-strip 42 and its corresponding underlying end crystal portion 44 define resistors R3 and R4 in an identical manner. The distributed capacitance at the PN junctions formed by P-strips 32 and 42 with their underlying corresponding N-strip portions provide a distributed capacitance equivalent to capacitors C_3 and C_4, each having a value of 1000 micromicrofarads.

Also formed in N-strip 12 is the transistor TR-1 having a collector region defined by an area of strip 12, a P-layer 45 formed by diffusion defining a base region and an N-layer 46 defining an emitter region. An ohmic contact 48 is plated on the emitter layer 46 and an ohmic contact 50 is plated on the base layer so that electrical leads may be interconnected between these contacts and other elements, as described below. In cross section, TR-1 is similar to TR-2 with the exception that TR-1 has only one diffused emitter region instead of two. Even though TR-1 has the form of a transistor, it provides two junction diodes by means of its collector-base and emitter-base PN junctions. The structure is here utilized as two separate PN junction diodes D_1 and D_4 rather than to provide conventional transistor action.

Also formed in strip 12 is a PN junction diode D_3, this diode being formed of a PN junction comprising a portion 52 of the N-crystal and a P-layer 54 formed therein by diffusion and carrying an ohmic contact 56.

A P-layer 58 formed in N-strip 14 by diffusion is not etched away, and two N-layers are formed in P-layer 58 by diffusion to form identical junction diodes D_2 and D_7. In this case, the PN junction is formed between the P-layer 58 and the N-layer 60 with the N-strip 14 merely acting as a substrate. A metal contact 62 is plated on N-layer 60 to provide means for interconnecting the junction with other circuit components or leads.

Also formed on strip 14 are two oxide-type semiconductor network coupling capacitors C_1 and C_2 formed as described in said co-pending application No. 3633/60 (Serial no. 945,734). Oxide capacitor C_1 comprises a silicon dioxide coating 64 on P-layer 58. This coating acts as a dielectric for the capacitor C_1. A metal plate 66 is then plated on top of oxide coating 64 to complete formation of the capacitor. The capacitor is defined by the two conductors, P-layer 58 and metal plate 66, separated by the dielectric oxide coating 64.

Additional leads are attached to the substrate 10, and are utilized when this bistable multivibrator is connected as a part of a binary counter. These leads are as follows: input lead 68; clear lead 70; set lead 72; lockout lead 74; ground lead 76. External wires interconnect the various circuit components with each other, and with the leads in a manner to provide bistable multivibrator operation.

The general operation of the semiconductor device just described will be briefly described to provide a better understanding of the device.

The device provides a gated bistable multivibrator designed for use as one stage of a binary counter. The set input lead is utilized to determine which transistor will be initially conducting and which initially non-conducting. Since both TR-2 and TR-3 are NPN transistors, a positive pulse on the base of transistor TR-2 will render that transistor conducting and TR-3 non-conducting. Negative trigger pulses may then be applied to the input lead through diode D_7, coupling capacitor C_1 and diode D_5 to cut off transistor TR-2 and render transistor TR-3 conducting. A second trigger pulse will return the circuit to its original condition. Selective application of pulses to the lockout lead may lock out or block trigger pulses applied to the input lead to render the multivibrator circuit insensitive to input pulses. A positive polarity pulse applied to the clear lead will return the circuit to its original condition. Output 1 and output 2 supply output pulses indicative of the state of their corresponding transistor.

Therefore, Fig. 2 illustrates a basic gated bistable multivibrator circuit diagram which represents the operation of the semiconductor device of Fig. 1.

It must be emphasized here that only one preferred embodiment of this invention has been described above, and that variations and modifications thereof may be made without departing from the scope of this invention, which is defined in the appended claims.

Thus, for example, since it is known that intrinsic semiconductor material is characterized by a relatively high order of resistivity, the substrate could be formed therefrom; or, the entire unit could be formed from a block of intrinsic semiconductor material into which doping impurities are diffused in the regions occupied by the cut wafers in the drawing. According to this arrangement, Item 10 of Fig. 1 would be either a separate block of intrinsic material on which wafers 12 and 14 were mounted, or it would be part of the same physical piece of semiconductor material as areas 12 and 14, the latter differing therefrom only in electrical characteristics due to impurity doping.

Reference is additionally made to our co-pending patent applications nos. 46086/63; 46087/63; 46088/63; 46089/63; and 46090/63 (Serial nos. 958,245, 958,246, 958,247, 958,248 and 958,249) also divided from said parent application no. 16071/60 (Serial no. 958,242).

WHAT WE CLAIM IS:—

1. A semiconductor device comprising a single crystal semiconductor wafer including two or more first P-N junctions extending to and terminating at one and the same major wafer face to form two or more spaced discrete regions on, adjacent to said major wafer face and spaced from the opposite major wafer face, two or more of said discrete regions being adapted to provide the electrical properties of circuit elements each including a second P-N junction extending to and terminating at said one major wafer face within one of said first P-N junctions, and said device further including ohmic contacts secured to said one major wafer face within each of said first P-N junctions and on each side of said second P-N junction.

2. A semiconductor device according to claim 1, wherein one or more of said discrete regions comprises an elongated portion adapted to provide the electrical properties of a resistor.

H. D. FITZPATRICK & CO.,
Chartered Patent Agents,
3 Gray's Inn Square, London, W.C.1,
and
94 Hope Street, Glasgow, C.2.

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