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POLYSILICON GATE REOXIDATION IN A GAS MIXTURE OF OXYGEN AND NITROGEN TRIFLUORIDE GAS BY RAPID THERMAL PROCESSING TO IMPROVE HOT CARRIER IMMUNITY AND DEVICE PRODUCED THEREBY

BACKGROUND OF THE INVENTION

1. Field of the Invention

This invention relates to MOS FET transistor devices and more particularly to a method and a design to provide improved hot carrier immunity.

2. Description of Related Art

In the past transistors with fluorine in the gate oxide layer have been employed to enhance hot carrier reliability. However, gate oxide thickening is undesirable.

SUMMARY OF THE INVENTION

Problems encountered in providing hot carrier immunity are shown by the embodiments of FIGS. 3 and 4. The problem is that it has been found that while fluorine in the gate oxide layer of an FET device will improve hot carrier reliability, gate oxide thickening is undesirable.

FIG. 4 shows an FET transistor device 110 manufactured with LDD regions 120, 120' as well as source/drain regions 122/122'. The P- doped silicon semiconductor substrate 112 has an upper surface upon which is formed a fluorinated gate oxide layer 118 composed of silicon oxide. The gate oxide layer 118, which has a thickness from about 50Å to about

150Å, is formed by the process of thermal processing or CVD (chemical vapor deposition) processing.

A polysilicon gate electrode 116 has been formed over the exposed top surface of gate oxide layer 118. Layer 116 has been highly doped with phosphorus (P) or arsenic (As) dopant with a concentration from about 10^{19} atoms/cm^3 to about $5x10^{21}$ atoms/cm^3 formed by ion implanting at an energy level from about 20keV to about 50keV.

A tungsten silicide (WSi_x) layer is then deposited by a CVD process based on a SiH_4 and WF_6 reaction. Fluorine is introduced into the polysilicon and consequently to the gate oxide by the annealing cycle. Fluorine (F) concentration is from about 1 x 10^{20} atoms/cm^3 to about 1 x 10^{22} atoms/cm^3.

Lightly doped (LDD) regions 120 and 120' have been formed in the substrate 112 aside from the gate electrode 116. Source/drain regions 122/122' have been formed in the substrate 112 aside from silicon spacers 140 which are formed adjacent to the gate electrode 116.

FIG. 5 shows an FET transistor device 130 manufactured with source/drain regions 144/144', but without any LDD regions. The P- doped silicon semiconductor substrate 132 has an upper surface upon which is formed a gate oxide layer 138 composed of silicon oxide. The gate oxide layer 138 has a thickness from about 50Å to about 150Å is formed by the

process of thermal processing or CVD (chemical vapor deposition) processing.

A polysilicon gate electrode 136 has been formed over the exposed top surface of fluorinated gate oxide layer 138. Layer 136 has been highly doped with As or P dopant with a concentration from about 1 x 10^{19} atoms/cm^3 to about 5x10^{21} atoms/cm^3 formed by ion implanting at an energy level from about 20keV to about 50keV.

A tungsten silicide (WSi_x) layer is then deposited by a CVD process based on a SiH_4 and WF_6 reaction. Fluorine is introduced into the polysilicon and consequently to the gate oxide by the annealing cycle. The resulting fluorine (F) concentration is from about 1 x 10^{20} atoms/cm^3 to about 1 x 10^{22} atoms/cm^3.

Source/drain regions 144/144' have been formed in the substrate 132.

Disadvantages of fluorinated gate dielectrics are as follows:

1. More traps - P channel/hot electron much worse;
2. Gate oxide charge to breakdown is reduced;
3. Fluorine (F) in gate oxide changes dielectric constant reduces current driver;
4. If too much fluorine (F) the gate oxide thickness is increased and that also reduces the current driver.

An FET transistor in accordance with this invention comprises a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein. The control gate electrode may be formed of a polysilicon and tungsten silicide (WSi_x). A WSi_x layer may be deposited by chemical vapor deposition (CVD) by the reaction of dichlorosilane (DCS) SiH_2Cl_2 and tungsten hexafluoride (WF_6) which does not introduce significant fluorine (F) into the gate oxide layer. A silicon oxide layer is formed over the stack of the gate oxide layer and the control gate electrode and exposed portions of the semiconductor substrate where the source/drain regions of the transistor are formed. The silicon oxide layer and the corners of the gate oxide layer have been fluorinated by rapid thermal processing providing a fluorinated silicon oxide layer.

In accordance with this invention, a method of forming an FET transistor comprises the following steps. Form a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein. Form a silicon oxide layer over the stack of the gate oxide layer and the control gate electrode and exposed portions of the semiconductor substrate including the source/drain regions. Form a transistor with the source/drain regions. Then, fluorinate

the silicon oxide layer and the corners of the gate oxide layer by rapid thermal processing providing a fluorinated silicon oxide layer.

Preferably, the rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas, at a temperature from about 900°C to about 1050°C; for a time duration from about 10 seconds to about 50 seconds, and the fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

In accordance with another aspect of this invention the process includes the following steps. Form a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein. Form a silicon oxide layer over the stack of the gate oxide layer and the control gate electrode and exposed portions of the semiconductor substrate including the source/drain regions. The silicon oxide layer has a thickness from about 200Å to about 400Å. Then, fluorinate the silicon oxide layer and the corners of the gate oxide layer by rapid thermal processing providing a fluorinated silicon oxide layer.

Preferably, the rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about

10 seconds to about 50 seconds, and the fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

In accordance with another aspect of this invention, an FET transistor includes the following features. A stack of a gate oxide layer and a control gate electrode is formed on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein. A silicon oxide layer is formed over the stack of the gate oxide layer and the control gate electrode and exposed portions of the semiconductor substrate including the source/drain regions. The silicon oxide layer and the corners of the gate oxide layer having been fluorinated by rapid thermal processing providing a fluorinated silicon oxide layer.

The rapid thermal processing was performed at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds and the fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

Further in accordance with this invention, an FET transistor has the following features. A stack of a gate oxide layer and a control gate electrode is formed on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein. A silicon oxide layer overlies the stack of the gate oxide layer and the control gate electrode and exposed portions of the semiconductor

substrate including the source/drain regions. The silicon oxide layer has a thickness from about 200Å to about 400Å. The silicon oxide layer and the corners of the gate oxide layer have been fluorinated by rapid thermal processing provide a fluorinated silicon oxide layer.

Preferably, the rapid thermal processing was performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds, and the fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å. The control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other aspects and advantages of this invention are explained and described below with reference to the accompanying drawings, in which:

FIGS. 1A-1J show the process of manufacture of a MOS FET transistor device 10 on a P- substrate or well 12 in accordance with this invention. Alternatively an N- substrate or well can be used.

FIG. 2 shows a modification of FIG. 1 in which an alternative process in accordance with this invention is employed with a WSi_x layer deposited on the polysilicon to form a polycide type of gate electrode.

FIG. 3 shows an FET transistor device in accordance with this invention manufactured without any LDD regions.

FIG. 4 shows an FET transistor device manufactured with LDD regions, as well as, source/drain regions. The P- doped silicon semiconductor substrate has an upper surface upon which is formed a fluorinated gate oxide layer composed of silicon oxide with a polysilicon gate electrode formed over the exposed top surface of gate oxide layer. A tungsten silicide (WSi_x) layer has been deposited by a CVD process based on a SiH_4 and WF_6 reaction with fluorine introduced into the polysilicon and consequently to the gate oxide by the annealing cycle.

FIG. 5 shows an FET transistor device 130 manufactured with source/drain regions, without any LDD regions. A P-doped silicon semiconductor substrate has an upper surface with a gate oxide layer with a polysilicon gate electrode formed over the exposed top surface of fluorinated gate oxide layer, and a tungsten silicide (WSi_x) layer based on a SiH_4 and WF_6 reaction with fluorine being introduced into the polysilicon and consequently to the gate oxide by the annealing cycle.

DESCRIPTION OF THE PREFERRED EMBODIMENT

In accordance with this invention, an FET transistor comprises a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate

with counterdoped source/drain regions therein. A silicon oxide layer is formed over the stack of the gate oxide layer and the control gate electrode and exposed portions of the semiconductor substrate including the source/drain regions of a transistor. The silicon oxide layer has a thickness from about 200Å to about 400Å. The silicon oxide layer and the corners of the gate oxide layer have been fluorinated by rapid thermal processing providing a fluorinated silicon oxide layer. The rapid thermal processing was performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds, and the fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

This invention suggests reoxidation of polysilicon in O_2 and NF_3 by RTP (Rapid Thermal Processing also known as RTA or Rapid Thermal Annealing) as a simple approach to incorporate fluorine (F) only at the gate edge of an MOS FET device to reduce overlap capacitance and improve HCI (Hot Carrier Injection) without oxide thickening.

The process includes the steps as follows:

A. Define a polysilicon gate electrode over a gate oxide layer.

B. Regrow or deposit a thin oxide layer over the gate electrode.

C. Treatment of the device by RTP in an atmosphere of O_2 & NF_3 for both P & N channel devices is possible, i.e. there is no problem. The process involves RTP in O_2 & NF_3 (900°C to 1050°C for 10 seconds to 50 seconds) fluorine (F) incorporation into gate oxide only in the corner of the gate electrode.

Advantages of the process of this invention are as follows:

1. Improve N- channel HCI;
2. Reduce N- channel & P- channel overlap capacitance;
3. The process is simple;
4. A single drain could be used.

FIGS. 1A-1J show the process of manufacture of a MOS FET transistor device 10 on a P- substrate or well 12 in accordance with this invention. Alternatively an N- substrate or well can be used.

FIG. 1A shows the device 10 in an early stage of manufacture with a P- doped silicon semiconductor substrate 10 (or a well 10) having an upper surface upon which a blanket gate oxide layer 14 composed of silicon oxide has been formed. The gate oxide layer 14 has a thickness from about 50Å to about 150Å is formed by thermal processing or chemical vapor deposition.

FIG. 1B shows the device 10 FIG. 1A after a blanket layer of polysilicon 16 (for a gate electrode) has been formed over the exposed top surface of gate oxide layer 14.

Layer 16 has been highly doped with arsenic (As) or phosphorus (P) dopant 15 with a concentration from about 1 x 10^{19} atoms/cm^3 to about 5 x 10^{21} atoms/cm^3 formed by ion implanting at an energy level from about 20keV to about 50keV. Alternatively, layer 16 could be a stack consisting of polysilicon and tungsten silicide (WSi_x) which is deposited by CVD involving the reaction of dichlorosilane (DCS) SiH_2Cl_2 and tungsten hexafluoride (WF_6), which does not introduce significant fluorine (F) into the gate oxide layer 14.

FIG. 1C shows the device 10 of FIG. 1B after a gate electrode mask 17 has been formed over the layer 16 and used during patterning of the gate electrode 16 and the gate oxide layer 14 by etching away the portions of those layers unprotected by the mask 17. Portions of the top surface of the substrate 12 from which layers 14 and 16 have been removed are exposed.

FIG. 1D shows the device 10 of FIG. 1C after a blanket thin silicon oxide dielectric layer 18 has a thickness from about 200Å to about 400Å is formed by the process of LPCVD (Low Pressure Chemical Vapor Deposition) or thermal processing.

The parameters of the process for forming the dielectric layer 18 are within the range from about 600°C to

about 750°C for an LPCVD process or from 850°C to about 920°C for thermal processing.

FIG. 1E shows the device 10 of FIG. 1D after it has been subjected to rapid thermal processing, oxidation and fluorination (i.e. treatment with fluorine) of layer 18 into a fluorinated (i.e. having fluorine in combination) layer 18'. The process of fluorination and oxidation is performed in a chamber which is first evacuated and then filled with a gaseous atmosphere of oxygen gas (O_2) and nitrogen trifluoride gas (NF_3) at a temperature from about 900°C to about 1050°C for a duration from about 10 seconds to about 50 seconds converting the silicon oxide layer 18 into a layer 18' composed of a silicon oxide and fluorine. The resulting fluorine (F) concentration is from about 5×10^{20} atoms/cm^3 to about 1×10^{22} atoms/cm^3. Layer 18' has a thickness from about 200Å to about 400Å, which was the thickness of layer 18 prior to fluorination.

Note that the treatment by fluorination and oxidation in a gaseous atmosphere of oxygen gas (O_2) and nitrogen trifluoride gas (NF_3) will not change the thickness of oxide layer 18 when it it is converted to layer 18'. The reduction in the overlap capacitance is mainly attributable to the change in the dielectric constant.

The resulting layer 18' with silicon oxide layer and fluorine includes portions 14' and 14'' of the gate oxide

layer 14 at the periphery of the gate electrode 16 just above the substrate 12. The fluorine incorporated in layer 14 extends between about 100Å to about 500Å from the sidewall of the gate electrode 16 and extending beneath the lower surface of the gate electrode 16 in portions 14' and 14''.

FIG. 1F shows the device 10 of FIG. 1E after the lightly doped drain N- doped regions 20, 20' are formed on either side of the gate electrode 16 by ion implantation with ions 25. LDD regions 20, 20' are lightly doped in a process of self-aligned doping of those regions with phosphorus (P) or arsenic (As) dopant 25 with a concentration from about about 1 x 10^{17} atoms/cm^3 to about 5 x 10^{18} atoms/cm^3 formed by ion implanting at an energy level from about 25 keV to about 80 keV.

FIG. 1G shows the device 10 of FIG. 1F after a formation of a blanket silicon dioxide spacer layer 40' covering the device 10 having a thickness from about 500Å to about 1500Å has been formed over the device 10.

Next, referring to FIG. 1H, the spacer layer 40' on device 10 of FIG. 1G has been subjected to a spacer etch back to yield the spacers 40 seen in FIGS. 1H-1J. In addition to forming the spacers 40, the spacer etching process etches away those portions of layer 18' aside from

the spacers 40 down to the surface of substrate 12, above portions of lightly doped drain (LDD) N- regions 20, 20'.

FIG. 1I shows the device 10 of FIG. 1H after the source/drain regions 22, 22' have been heavily doped in a process of self-aligned doping of those regions with arsenic (As) dopant 27 with a concentration from about about 5×10^{19} atoms/cm^3 to about 1×10^{21} atoms/cm^3 formed by ion implanting at an energy level from about 25 keV to about 80 keV.

FIG. 1J shows the product of FIG. 1I after completion of processing in accordance with this invention.

FIG. 2 shows a modification of FIG. 1 in which an alternative process in accordance with this invention is employed. The same process is employed except that after the step of FIG. 1B, a WSi_x layer 66 was deposited on the polysilicon layer 16 to form a polycide type of gate electrode formed of layers 16 and 66. The WSi_x layer 66 was formed by chemical vapor deposition (CVD) by the reaction of dichlorosilane (DCS) SiH_2Cl_2 and tungsten hexafluoride (WF_6) which does not introduce significant fluorine (F) into the gate oxide layer.

FIG. 3 shows an FET transistor device 30 in accordance with this invention manufactured without any LDD regions. A P- doped silicon semiconductor substrate 32 has an upper surface upon which is formed gate oxide layer 34 composed of

silicon oxide. The gate oxide layer 34, with a thickness from about 50Å to about 150Å, is formed by thermal processing or chemical vapor deposition.

A polysilicon gate electrode 36 has been formed over the exposed top surface of gate oxide layer 34. Layer 36 has been highly doped with arsenic (As) or phosphorus (P) dopant 15 with a concentration from about 1 x 10^{19} atoms/cm^3 to about 5 x 10^{21} atoms/cm^3 formed by ion implanting at an energy level from about 20keV to about 50keV.

A thin fluorinated silicon oxide dielectric layer 38' has a thickness from about 200Å to about 400Å formed as described above in connection with FIGS. 1A-1D.

The fluorinated silicon oxide layer 38' is composed of silicon oxide and fluorine. The resulting fluorine (F) concentration is about 5 x 10^{20} atoms/cm^3.

There are portions 34' and 34'' of the gate oxide layer 34 at the periphery of the gate electrode 36 above the substrate 32 which have fluorine incorporated therein extending from about 100Å to about 500Å from the sidewall of the gate electrode 36 and extending beneath the lower surface of the gate electrode 36.

While this invention has been described in terms of the above specific embodiment(s), those skilled in the art will recognize that the invention can be practiced with modifications within the spirit and scope of the appended claims,

i.e. that changes can be made in form and detail, without departing from the spirit and scope of the invention. Accordingly all such changes come within the purview of the present invention and the invention encompasses the subject matter of the claims which follow.

CLAIMS

Having thus described the invention, what is claimed as new and desirable to be secured by Letters Patent is as follows:

1. A method of forming an FET transistor comprising the steps as follows:

forming a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein,

forming a silicon oxide layer over said stack of said gate oxide layer and said control gate electrode and exposed portions of said semiconductor substrate including said source/drain regions,

fluorinating said silicon oxide layer and the corners of said gate oxide layer by rapid thermal processing providing a fluorinated silicon oxide layer.

2. A method in accordance with claim 1 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas.

3. A method in accordance with claim 1 wherein said rapid thermal processing is performed at a temperature from about 900°C to about 1050°C.

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4. A method in accordance with claim 1 wherein said rapid thermal processing is performed at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds.

5. A method in accordance with claim 1 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C.

6. A method in accordance with claim 1 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds.

7. A method in accordance with claim 1 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

8. A method in accordance with claim 1 wherein said rapid thermal processing is performed at a temperature from about 900°C to about 1050°C and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

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9. A method in accordance with claim 1 wherein said rapid thermal processing is performed at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

10. A method in accordance with claim 1 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

11. A method in accordance with claim 1 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds, and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

12. A method of forming an FET transistor comprising the steps as follows:

forming a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein,

forming a silicon oxide layer over said stack of said gate oxide layer and said control gate electrode and over exposed portions of said semiconductor substrate including said source/drain regions, said silicon oxide layer having a thickness from about 200Å to about 400Å,

fluorinating said silicon oxide layer and the corners of said gate oxide layer by rapid thermal processing providing a fluorinated silicon oxide layer.

13. A method in accordance with claim 12 wherein said rapid thermal processing is performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds, and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

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14. An FET transistor comprising:

a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein,

a silicon oxide layer over said stack of said gate oxide layer and said control gate electrode and over exposed portions of said semiconductor substrate including said source/drain regions,

said silicon oxide layer and the corners of said gate oxide layer having been fluorinated by rapid thermal processing providing a fluorinated silicon oxide layer.

15. A transistor in accordance with claim 14 wherein said rapid thermal processing was performed in an atmosphere of NF_3 gas and O_2 gas and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

16. A transistor in accordance with claim 14 wherein said rapid thermal processing was performed at a temperature from about 900°C to about 1050°C and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

17. A transistor in accordance with claim 14 wherein said rapid thermal processing was performed at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

18. A transistor in accordance with claim 14 wherein said rapid thermal processing was performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

19. A transistor in accordance with claim 14 wherein said rapid thermal processing was performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds, and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

20. An FET transistor comprising:

a stack of a gate oxide layer and a control gate electrode on a surface of a doped semiconductor substrate with counterdoped source/drain regions therein,

a silicon oxide layer over said stack of said gate oxide layer and said control gate electrode and exposed portions of said semiconductor substrate including said source/drain regions, said gate oxide layer having a thickness from about 200Å to about 400Å,

said silicon oxide layer and the corners of said gate oxide layer having been fluorinated by rapid thermal processing providing a fluorinated silicon oxide layer.

21. A transistor in accordance with claim 20 wherein said rapid thermal processing was performed in an atmosphere of NF_3 gas and O_2 gas at a temperature from about 900°C to about 1050°C for a time duration from about 10 seconds to about 50 seconds, and said fluorinated silicon oxide layer has a thickness from about 200Å to about 400Å.

22. A method in accordance with claim 1 wherein the control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.

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23. A method in accordance with claim 12 wherein the control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.

24. A method in accordance with claim 13 wherein the control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.

25. A transistor in accordance with claim 14 wherein the control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.

26. A transistor in accordance with claim 20 wherein the control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.

27. A transistor in accordance with claim 21 wherein the control gate electrode comprises a polycide structure comprising a layer of polysilicon and a tungsten silicide layer.