CLAIMS

1. An equalization training method, comprising:

obtaining (900) a training rate of each of a master chip (1603) and a slave chip (1604) in a target phase of equalization training, wherein the target phase is a third phase or a fourth phase; and

determining a target rate threshold interval within which the training rate in the target phase falls, determining (901), based on a correspondence between N+1 rate threshold intervals and N+1 equalization timeout periods, a target equalization timeout period corresponding to the target rate threshold interval, and configuring (902) the target equalization timeout period as an equalization timeout period in the target phase, wherein N rate thresholds are predetermined, N is an integer greater than 0, and each (N+1)-th rate threshold interval is larger than a N-th rate threshold interval, and an equalization timeout period corresponding to the (N+1)-th rate threshold interval is larger than the equalization timeout period corresponding to the N-th rate threshold interval; and wherein

equalization training in the target phase is performed on the master chip (1603) and the slave chip (1604) within the equalization timeout period in the target phase.

2. The method according to claim 1, wherein when the target rate threshold interval is a threshold interval comprising a minimum rate in the N+1 rate threshold intervals, the target equalization timeout period is a forward compatible equalization timeout period.

3. The method according to claim 1, wherein the correspondence between the N+1 rate threshold intervals and the N+1 equalization timeout periods is prestored in a register of the master chip (1603) or in a register of the slave chip (1604).

4. The method according to any one of claims 1 to 3, wherein the master chip (1603) and the slave chip (1604) are connected through a peripheral component interconnect express, PCIe, bus or a cache coherent interconnect for accelerators, CCIX, bus, the master chip (1603) is a root complex or a switch chip, and the slave chip (1604) is an endpoint device independent of the master chip (1603).

5. An equalization training apparatus (1200), comprising:

a transceiver (1201), configured to obtain a training rate of each of a master chip (1603) and a slave chip (1604) in a target phase of equalization training, wherein the target phase is a third phase or a fourth phase; and

a manager (1202), configured to: determine a target rate threshold interval within which the training rate in the target phase falls, determine, based on a correspondence between N+1 rate

threshold intervals and N+1 equalization timeout periods, a target equalization timeout period corresponding to the target rate threshold interval, and configure the target equalization timeout period as an equalization timeout period in the target phase, wherein N rate thresholds are predetermined, N is an integer greater than 0, and each (N+1)-th rate threshold interval is larger than a N-th rate threshold interval, and an equalization timeout period corresponding to the (N+1)-th rate threshold interval is larger than the equalization timeout period corresponding to the N-th rate threshold interval, wherein equalization training in the target phase is performed on the master chip (1603) and the slave chip (1604) within the equalization timeout period in the target phase.

6. The apparatus (1200) according to claim 5, wherein when the target rate threshold interval is a threshold interval comprising a minimum rate in the N+1 rate threshold intervals, the target equalization timeout period is a forward compatible equalization timeout period.

7. The apparatus (1200) according to claim 5, wherein the correspondence between the N+1 rate threshold intervals and the N+1 equalization timeout periods is prestored in a register of the master chip (1603) or in a register of the slave chip (1604).

8. The apparatus (1200) according to any one of claims 5 to 7, wherein the master chip (1603) and the slave chip (1604) are connected through a peripheral component interconnect express, PCIe, bus or a cache coherent interconnect for accelerators, CCIX),bus, the master chip (1603) is a root complex or a switch chip, and the slave chip (1604) is an endpoint device independent of the master chip (1603).

9. The apparatus(1200) according to any one of claims 5 to 8, being a chip (1500), the chip (1500) being the master chip (1603) or the slave chip (1604).

10. A communications system (1600), comprising system software (1601), a master chip (1603), and a slave chip (1604), wherein the master chip (1603) and the slave chip (1604) are connected to each other through a peripheral component interconnect express, PCIe, bus or a cache coherent interconnect for accelerators, CCIX, bus; and

the system software (1601) is configured to perform the method according to claims 1 to 4.