ABSTRACT

PACKAGED SEMICONDUCTOR DEVICE HAVING STRESS ABSORBING FILM

A packaged semiconductor device has a semiconductor chip (1) and leads (3) formed over the chip with an electrically insulating film (4) interposed therebetween and a packaging material (2) for sealing the chip and the inner lead portions (3A) of the leads. The electrically insulating film has such an area as to provide a peripheral portion not covered by parts of the inner lead portions of the leads for strengthening adherence of the electrically insulating film to the packaging material and to the chip. The electrically insulating film has a thickness substantially in a range from 80 μm to 200 μm for absorbing stress which may be produced in the packaged semiconductor device when subjected to variations of the ambient temperature. A stress absorption film (20) may be formed between the electrically insulating film and the semiconductor chip for absorbing stress which may be produced in the packaged semiconductor device when subjected to variations of the ambient temperature.

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