

(12)

"A memory device"

5 The present invention relates to a memory device
and, more particularly, to a programmable read-only
memory device.

RAMs (random access memories) and ROMs (read-only
10 memories) are memory devices which are used in a variety
of electronic machines such as electronic computers.
ROMs include PROMs (programmable ROMs), one type of
which is a bipolar PROM.

As is well known in the art, PROMs are divided
15 into those using fuses and those using diodes. In
the former type of PROM, data is written by applying
a constant voltage of several volts to melt a fuse
made of polysilicon or nichrome. In the latter type
of PROM, on the other hand, the data writing operation
20 is conducted bit by bit by destroying PN junctions with
constant-current pulses of a pulse width of about 10
µsecs. As a result, the PROMs cannot have their data
erased once the data are written.

Semiconductor memory devices are used widely, not
25 only in microcomputers and minicomputers, but also in

(13)

- 2 -

large-scale computers, their capacities and speed continue to increase, and their power consumption decrease. With this increase in capacity and speed, the components of the semiconductor memory devices are reduced further in size so that the fabrication process thereof becomes even more complex. Even a slight difference in the fabrication process conditions means that the completed products have variations in their characteristics, and fail to meet their desired characteristics. This makes it necessary to check whether or not the product has characteristics satisfying the desired specifications, after the product is completed and before it is shipped to the user. For example, it is necessary to check whether or not the access time (i.e., the time interval from the instant when an input specifying an address is given, to the instant when the data stored in the predetermined memory cell is read out) meets the required characteristics. As has been described above, however, since no data can be written into the PROM before the user uses it, after the user have written in data, whether or not the access time of a PROM has the desired value cannot be checked when the product is completed.

We have, therefore, developed a system by which the characteristics are checked, by providing

a checking memory cell which is separate from the memory cell used by the user and which has data written into it in advance at the fabrication stage, and by using that checking memory cell. Fig. 1 is a schematic circuit diagram of a portion of a semiconductor memory device previously developed by us. The checking method will be described with reference to Fig. 1 of the accompanying drawings.

Memory cells $C_1, C_2, C_3, C_4, C_5,$

C_6, C_7, C_8 and C_9 are provided so as to intersect

word lines X_{ℓ_1}, X_{ℓ_2} and X_{ℓ_3} and bit lines Y_{ℓ_1}, Y_{ℓ_2} and Y_{ℓ_3} . Of these memory cells, memory cells C_1, C_2, C_3, C_6 and C_9 are used for checking operations, and memory cells C_4, C_5, C_7 and C_8 provide memory circuits which are used as required by the user.

During the checking, a voltage signal of about 8 V is supplied to a word input X and a bit input Y. The voltage level of 8 V is that used in the checking, two values of 0 V and 3 V are supplied when the user is using the PROM. In Fig. 1, the threshold voltages of inverters IV_1 and IV_5 are set at 7 V, and those of inverters $IV_2, IV_3, IV_4, IV_6, IV_7$ and IV_8 at 1.5 V. The setting of the threshold voltages of these inverters at different values is designed to prevent the user reading the data written into the checking memory cells by the manufacture of the PROM.

(5)

- 4 -

A method of selecting the directions of the word lines of the checking memory cells will now be described. When the voltage signal of 8 V is supplied through the word input X and the bit input Y, the output of the inverter IV_1 forming a checking circuit 1 goes low

and the output of the inverter IV_2 goes high.

As a result, the output of a word driver A_1 goes high so that the word line X_{θ_1} is selected. It should be noted that the word lines and bit lines are selected when they go high. The word lines X_{θ_2} and X_{θ_3} are not selected.

Similarly, the output of the inverter IV_5 forming a check circuit 2 goes low, and the output of the inverter IV_6 goes high. The output of the inverter IV_7 also goes low, and the output of the inverter IV_8 goes high. As a result, the input terminal a of an AND circuit A_{11} goes low. The input terminals a and b of an AND circuit A_{12} go high and low, respectively, the outputs of the AND circuits A_{11} and A_{12} are fixed at the low level irrespective whether the data written in the memory cells C_1 and C_2 is at the level "1" or "0". Since the input terminal a of an AND circuit A_{13} is high on the other hand, the data stored in the memory cell C_3 is extracted from the output of the AND circuit A_{13} , and is further output through an OR circuit O_1 . Thus, the data in the memory

cell C_3 is read out. In each memory cell, the state in which either the fuse is melted or the diode is destroyed corresponds to the level "1", and the undestroyed state thereof corresponds to the level "0".

5 In the following, when the memory cell C_2 is to be checked, the voltage signal of 8 V is supplied to the word input X, and a voltage signal of about 3 V is supplied to the bit input Y. This selects the word line $X\phi_1$, as described above. Since the output of the
10 inverter IV_5 is high and the output of the inverter IV_8 is also high, on the other hand, the bit line $Y\phi_2$ is selected so that the data in the memory cell C_2 is read out from the AND circuit A_{12} .

15 When the memory cell C_1 is being checked, moreover, the bit input Y is dropped to 0 V, so that the word line $X\phi_1$ is selected in the same way. However, the output of the inverter IV_5 is high, and that of the inverter IV_6 is low. Moreover, the output of the inverter IV_7 is high, and the output of the inverter IV_8 is
20 low. In this case, the bit line $Y\phi_1$ is selected so that the data in the memory cell C_1 is read out from the AND circuit A_{11} . By changing the voltage levels of the word input X and the bit input Y in this manner, data is consecutively read out from the memory cells
25 C_1 , C_2 , and C_3 so that the characteristics of the

(17)

- 6 -

memory can be checked by measuring the access times.

The description thus far made concerns the data reading operation in the word line direction during the checking. The data reading operation in the bit line direction is conducted by fixing the bit input Y at the voltage level of 8 V, and by switching the voltage level of the word input X consecutively to 8 V, 3 V and 0 V. When the word input X is 8 V, the word line $X\phi_1$ and the bit line $Y\phi_3$ are selected, as described above, so that the data in the memory cell C_3 is read out. When the word input X is 3 V, the word line $X\phi_2$ is selected so that the data in the memory cell C_6 is read out. When the word input X is 0 V, the word line $X\phi_3$ and the bit line $Y\phi_3$ are selected so that the data in the memory cell C_9 is read out. This means that the data in the checking memory cells C_3 , C_6 and C_9 can be consecutively read out. This is the data reading operation in the bit line direction of the circuit, it is used to measure the access time to perform the check. However, a variety of further investigations conducted by us on this semiconductor memory device have revealed the following problems.

The voltage levels of the word address input X and the bit address input Y when the user uses the PRCM are 0 V and 3 V, whereas a voltage level of 8 V

is used in addition to the voltage levels 0 V and 3 V during the checking. As has been described above, when the check is changed from that on the access times of the checking memory cells in the word line direction to that on the access times of the memory cells in the bit line direction, the voltage level of the word address input X must be switched from 8 V to 3 V to 0 V. Thus, the input condition for selecting a memory cell during the checking is different from that used by the user, so that the access time obtained is different from that during use, reducing the checking accuracy.

Since the threshold voltages of the inverters IV_1 and IV_5 in the first stages of the check circuits 1 and 2 are set at 7 V, as described above, and are different from the threshold value of 1.5 V of the inverters IV_3 and IV_7 which are used by the user, the circuit constructions of the inverters is accordingly complicated. As a result, the signal delay in the inverters is different so that the access time obtained by the check is different from that during use, reducing the checking accuracy.

According to the present invention there is provided a memory device including:

- (a) main memory cells;
- (b) checking memory cells;
- 5 (c) an address circuit for permitting selective addressing of either the main memory cells or the checking memory cells by the applicaiton of selected first or second signal levels to addressing lines to the memory cells;
- 10 (d) an output buffer arranged to output the data in one of the memory cells with a predetermined address, by the operation of said address circuit; and
- (e) a control circuit for inhibiting the data output operation of said output buffer in response to a
- 15 first level of a control input signal;

wherein said address circuit includes a checking address circuit for selecting none of said checking memory cells when said control input signal is at a second level and for selecting said checking memory cell with said

20 predetermined address in response to a third level of said control input signal.

The present invention will now be described in greater detail by way of example with reference to the remaining figures of the accompanying drawings:-

25 Figure 2 is a circuit diagram of one preferred form of PROM;

Figure 3 is a more detailed circuit diagram of the PROM shown in Figure 2;

Figure 4 is a circuit diagram of the essential

30 parts of the multiplexer of the PROM shown in Figure 3;

and

Figure 5 is a circuit diagram of a second embodiment of PROM.

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Referring first to Fig. 2, the PROM includes a checking memory cell 11, and a control circuit 12 for switching the PROM between an operating mode and a checking mode. Inverters IV_{11} to IV_{14} together form an address input buffer, and an OR circuit N_1 provides an output buffer. The PROM also includes multiplexers M_1 to M_3 , word drivers A_{21} , A_{22} and A_{23} composed of AND circuits, word lines X_{11} , X_{12} and X_{13} , bit lines Y_{11} , Y_{12} and Y_{13} , and memory cells C_{11} , C_{12} , C_{13} , C_{14} , C_{15} , C_{16} , C_{17} , C_{18} and C_{19} .

It should be noted that, in this circuit, an output signal which is prepared by inverting the level of an

(21)

- 10 -

input signal supplied to the input terminal of a chip-
enable circuit 13 by an inverter IV_{15} , and an output
signal which is prepared by inverting the level of the
first output signal by an inverter IV_{16} , are supplied
5 to the word drivers A_{21} and A_{22} , respectively.

Another point to be noted is that address input
terminals X_1 and Y_1 , the inverters IV_{11} to IV_{14} forming
the input buffer and the output buffer N_1 are used in
common for checking and in actual use. Incidentally,
10 the inverters IV_{11} , IV_{12} , IV_{13} and IV_{14} , the word
drivers A_{21} , A_{22} and A_{23} and the multiplexers M_1 , M_2
and M_3 will be referred to collectively as "the address
circuit" in the following. The chip-enable circuit
(a chip-select circuit) will now be briefly described.

15 A chip-enable circuit has been incorporated recently
into most of the bipolar ROM ICs (integrated circuits),
and is a circuit which is used to expand the capacity
of the ROM, leaving the number of output bits unchanged
when a plurality of ROMs are connected in parallel,
20 and which controls whether one memory IC chip is
operative or inoperative. The chip-enable circuit 13
of the circuit shown in Fig. 2 is set so as to have
an input threshold voltage of 1.5 V, it makes the OR
circuit N_1 operative when a voltage higher than 1.5
25 V is applied, and inoperative when a voltage lower than

1.5 V is applied.

The input threshold voltages of the inverters IV_{11} , IV_{12} , IV_{13} , IV_{14} and IV_{16} are set at 1.5 V, and only the threshold voltage of the inverter IV_{15} is set at 7 V.

The word input X_1 (e.g., 0 V and 3 V) is supplied to the input terminal of the inverter IV_{11} . The bit input Y_1 (e.g., 0 V and 3 V) is supplied to the input terminal of the inverter IV_{13} .

The checking voltage of 8 V is supplied to the terminal T_1 when the PROM is being checked, and a voltage of 0 V or 3 V is applied to the terminal T_1 when the PROM is being used.

The procedure of checking the access time will be specifically explained in the following. First of all, the checking operation in the word line direction will be described.

A voltage signal of about 8 V is supplied to the input terminal T_1 . A high-level signal (of 3 V) is supplied to the word input X_1 . A low-level signal (of 0 V) is supplied to the bit input Y_1 . An output signal $\bar{B}$ from the inverter IV_{15} is low level, and an output signal B from the inverter IV_{16} is high level. Similarly, the output from the inverter IV_{11} is low level, and the output from the inverter IV_{12} is high

23

- 12 -

level. The output from the inverter IV_{13} is high level, and the output from the inverter IV_{14} is low level.

As a result, both inputs to the word driver A_{21} are high level and it operates to select the word line X_{21} . On the other hand, the word drivers A_{22} and A_{23} are inoperative, their outputs fixed at low level.

The inputs $\underline{a}$ and $\underline{b}$ of the multiplexer M_2 and the input $\underline{a}$ of the multiplexer M_3 are low so that the outputs of the multiplexers M_2 and M_3 are fixed at low irrespective of the data in the checking memory cells. The input $\underline{a}$ of the multiplexer M_1 is high so that the data in the checking memory cell C_{11} is read out through the multiplexer M_1 and the OR circuit N_1 acting as an output buffer.

Another example will be described in the following. The voltage signal of 8 V is supplied to the input terminal T_1 , and the high-level signal (of 3 V) is supplied simultaneously to the word input X_1 and the bit input Y_1 . The output signal $\bar{B}$ goes low and the output signal B goes high. The output from the inverter IV_{11} is low and the output from the inverter IV_{12} is high. Similarly, the output from the inverter IV_{13} is low and that from the inverter IV_{14} high.

As a result, the word driver A_{21} operates to



select the word line X_{11} , and the word drivers A_{22} and A_{23} are made inoperative. The multiplexer M_3 operates to select the bit line Y_{13} , so that the data in the memory cell C_{13} is read out.

5 The checking operation in the bit line direction will be described in the following. The voltage signal of about 8 V is supplied to the input terminal T_1 , the voltage of 0 V is supplied to the word input X_1 , and the voltage signal of 3 V is supplied to the bit input Y_1 . The output
10 signal $\bar{B}$ is low, and the output signal B is high. The output from the inverter IV_{11} is high and the output from the inverter IV_{12} is low. The output from the inverter IV_{13} is low and the output from the inverter IV_{14} is high.

As a result, the word driver A_{23} operates to
15 select the word line X_{13} , and the word drivers A_{21} and A_{22} are made inoperative. The multiplexer M_3 operates to select the bit line Y_{13} , so that the data in the memory cell C_{19} is read out.

It will be appreciated from the above that only
20 the checking memory cells C_{11} , C_{13} and C_{19} can be selected when the control signal T_1 is at the third level, the cells C_{12} and C_{16} being unselectable by the checking address circuit 12.

The data in each of the checking memory cells,
25 which is read out by these checking operations, is supplied from the corresponding multiplexers to the NOR circuit N_1 . Data is obtained from each checking memory cell in response to an output signal 0 from the NOR

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circuit N_1 . The characteristics are checked by repeating these operations to examine the access times.

In this PROM, more specifically, the input conditions for checking and for actual use are identical (i.e. 0 V or 3 V) so that the checks can be conducted without supplying any special checking voltage signal. When used by the user, the voltage supplied to the terminal T_1 is 0 V or 3 V, which ensures that the outputs from the checking word driver A_{21} and the multiplexer M_3 are fixed at low level so that the data in the checking memory cells is not read out when the user is using the PROM.

The PROM shown in Fig. 2, will now be described in greater detail with reference to Figs. 3 and 4. Fig. 3 is a circuit diagram of a bipolar PROM which is constructed to have 1,024 words x 8 bits, and which has one chip-enable input and an address decoder built in, and Fig. 4 is an enlarged circuit diagram of the multiplexers and an output buffer of the PROM shown in Fig. 3.

Referring to Fig. 3, the bipolar PROM includes: a chip-enable circuit 13 which makes OR circuits (output buffers) N_2 to N_9 operative, when its terminal T_1 is supplied with a voltage higher than 1.5 V, and inoperative when supplied with a voltage lower than 1.5 V; a word buffer 14 which corresponds to the

inverters IV_{11} and IV_{12} of Fig. 2; and a bit address buffer 15 which corresponds to the inverters IV_{13} and IV_{14} of Fig. 2. The circuit further includes a decoder 16 for decoding 1 : 64; memory cell blocks 17 of 1,024 (i.e. 16×64 bits), which form
5 a memory cell array of a total of 8,192 bits; and a 1 : 16 multiplexer 18 which corresponds to the multiplexers M_1 , M_2 and M_3 of Fig. 2. The word address buffer 14, the bit address buffer 15, the X decoder 16, the word drivers A_1 to A_{65} and the multiplexers M_1 to M_{129} will hereinafter be referred to
10 collectively as "the address circuit". An output buffer 19 is formed by OR circuits N_2 to N_9 which correspond to the OR circuit N_1 of Fig. 2.

Of the word drivers A_1 to A_{65} , the word driver A_1 is used for checking the access time, whereas the sixty-four drivers A_2
15 to A_{65} are used by the user. The circles in the drawing indicate each of the memory cells, in particular, the block enclosed in the triple-dot-dash line is the checking memory cell.

The features of the PROM constructed as above described will now be explained in greater detail. First of all, the address
20 circuit and the output buffer 19 are used in



common when the checking memory cells are selected, and when the main memory cells are selected. Another feature is that the respective output signals $\bar{B}$ and B from the inverters IV_{15} and IV_{16} forming the checking address circuit 12 are supplied to the word drivers A_1 and A_2 and the multiplexers M_{128} and M_{129} .

In view of the above circuit construction the word drivers A_1 and A_2 are prevented from operating simultaneously when a predetermined input condition is imposed upon the word inputs X_1 to X_7 , so that the checking operations and the operations in actual use are separated. A further notable feature is that the input threshold voltage of the inverter IV_{15} is set at 7 V, whereas the input threshold voltage of the inverter IV_{16} is set at 1.5 V.

One example of the checking operation will now be explained, with reference to the reading of data from a memory cell C_{100} .

In this case, the voltage signal of 8 V is first supplied to the input terminal T_1 to switch the FROM to the checking mode. The voltage of 0 V or 3 V is supplied to the word inputs X_1 to X_6 so that the corresponding input terminals of the word drivers A_1 and A_2 are at the high level. The output signal $\bar{B}$ from the inverter IV_{15} is at the low level, and the output signal B from the inverter

IV_{16} is at the high level. As a result, the output from the word driver A_2 is low whereas the output from the word driver A_1 is high so that the word line $X\ell_1$ is selected.

5 When the voltage signal of 3 V is supplied to all the bit inputs Y_1 to Y_4 , all the lines ℓ_1 , ℓ_3 , ℓ_5 and ℓ_7 of Figs. 3 and 4 go high because of the operations of the inverters IV_{41} to IV_{44} and IV_{51} to IV_{54} . On the other hand, all the lines ℓ_2 , ℓ_4 , ℓ_6 and ℓ_8 go low.

10 As a result, the bit line $Y\ell_{113}$ is selected and the data in the memory cell C_{100} is read out through the multiplexer M_{113} so that an output signal O_8 is obtained through the NOR circuit N_9 acting as the output buffer. Because the voltage signal of 8 V is supplied
15 to the input terminal T_1 , a control signal V_C is supplied from the chip-enable circuit 13 to the NOR circuit N_9 so that this NOR circuit N_9 is made operative.

20 When the data in a main memory cell C_{200} is to be read out, the voltage signal of 3 V is supplied to the terminal T_1 to switch the PROM to the operating mode so that the data in the memory cell C_{200} is read out if the addresses X_1 to X_6 and Y_1 to Y_4 are set to the same input conditions as those when the data in the checking memory cell C_{100} was read out.

25 The reading out of the data in a checking memory

cell C_{300} will be described in the following. The voltage signal of 8 V is supplied to the input terminal T_1 so that the PROM is switched to checking mode. The word inputs X_1 to X_7 are supplied with inputs determined by the combination of the decoder 16. As a result, the output from the word driver A_{65} is high so that the word line X_{65} is selected.

All the bit inputs Y_1 to Y_4 are supplied with the low-level voltage (i.e., 0 V) so that all the lines ℓ_1 , ℓ_3 , ℓ_5 and ℓ_7 are made low by the operations of the inverters IV_{41} to IV_{44} and IV_{51} to IV_{54} . On the other hand, the lines ℓ_2 , ℓ_4 , ℓ_6 and ℓ_8 are at the high level.

As a result, all the inputs to the multiplexers M_{128} and M_{129} are at the high level. Since the PROM is in the checking mode so that the control signal B is high and the control signal $\bar{B}$ is low, however, the output from the multiplexer M_{128} is fixed at the low level. As a result, the data in the checking memory cell C_{300} is read out through the multiplexer M_{129} and the OR circuit N_9 .

When the data in a memory cell C_{400} is to be read out, the voltage signal of 3 V is supplied to the terminal T_1 , and the same input conditions as those when the data in the checking memory cell C_{300} was

read out are imposed upon the addresses X_1 to X_6 and Y_1 to Y_4 . The data in the memory cell C_{400} is then read out through the multiplexer M_{128} and the OR circuit N_9 .

5 The PROM described above has the following advantages. Since the access time is checked under the same input conditions (i.e., 0 V and 3 V) as those when the PROM is actually used, the measuring accuracy is so improved that accurate checks can be conducted.

10 Since the checking circuit for the checking memory cells and the circuit for actual use have an identical construction, the access time measured by using the checking memory cells and the access time when in actual use are the same so that the checking
15 accuracy is improved.

Since the address buffers and the output buffers are skillfully used in common for the checking operations and for actual use, inputs and outputs do not increase.

20 Since the switching operations of the checking mode and the operating mode are conducted by making use of the input terminals of the chip-enable circuit, it is unnecessary to provide any dedicated input pin. As a result, there is no increase in the
25 number of pins of the PROM IC, so that the size of the

IC package is not increased in any way.

Incidentally, in the embodiment shown in Figs. 3 and 4, the chip-enable circuit has the function of making the output buffers N_2 to N_9 operative when a high-level input is received, but there is another chip-enable circuit which makes the output buffers N_2 to N_9 inoperative when the high-level input is received. This is exemplified by the case in which the chip-enable circuit acts as an inverter. In this case, the low-level output V_C of the chip-enable circuit makes the NOR circuits N_2 to N_9 inoperative when a voltage higher than 1.5 V, for example, is supplied to the terminal T_1 , and makes the output buffers N_2 to N_9 operative when a voltage lower than 1.5 V is supplied. With the circuit construction described above, the output V_C of the chip-enable circuit is low when the voltage signal of 8 V is applied to the terminal T_1 , as described above, so that the output buffers N_2 to N_9 cease to operate. The data written into the checking memory cells cannot be read out, so that the access time cannot be measured.

Referring now to the second embodiment of the PROM shown in Fig. 5, a chip-enable circuit 13' is provided which is

constructed of TTL inverters with tri-state outputs.

The threshold voltage of the inverter IV_{15} is set at 7 V, in the same way as that of the previous embodiment, and the threshold voltage of the inverter IV_{16} is set at 1.5 V. When the terminal T_1 is supplied with a voltage lower than 1.5 V, the resultant high-level output V_C makes the OR circuits N_2 to N_9 operative. When the terminal T_1 is supplied with a voltage higher than 1.5 V, on the other hand, the low-level output V_C of the chip-enable circuit makes the NOR circuits N_2 to N_9 inoperative. It should be noted here that, when the voltage signal of 8 V is supplied during checking to the terminal T_1 , the output $\bar{B}$ from the inverter IV_{15} is at the low level, which brings the chip-enable circuit 13' to a high-impedance state (floating state) so that the floating output V_C stops the control on the OR circuits N_2 to N_9 . At this time, more specifically, the OR circuits are operative because they are not controlled. With this construction, the output buffers are made operative to read out the data from the checking memory cells when the voltage signal of 8 V is applied to the terminal T_1 during the checking by the PROM manufacturer. The checking operations are similar to those described before. When in actual use (by the user), on the other hand, the PROM is

switched to the operating mode by applying the signal voltage of 0 V to the terminal T_1 . In view of the above circuit construction, the same advantages as those of the previous embodiment can be obtained, even although the chip-enable circuit 13' is constructed of inverters.

The following modifications of the above described circuits are possible.

The multiplexers, and the OR circuits shown in Fig. 4 may be constructed of combinations of logic circuits, or they may be constructed of diodes or TTL circuits.

The memory circuit being checked is not limited to a memory structure of 1K x 8 bits, but may be a memory structure with a larger capacity.

Whilst the above described embodiments specifically relate to the checking of a bipolar PROM, it can have other applications. For example, the circuit techniques described above can be applied to memory cells having a ROM structure.

Even if the memory cells are of the type used in electronic computers or other various industrial devices, for example, the circuit techniques described above can also be applied to the process of inspecting them.



(34)

- 23 -

CLAIMS.

1. A memory device including:
 - (a) main memory cells;
 - (b) checking memory cells;
 - (c) an address circuit for permitting selective
5 addressing of either the main memory cells or the checking
memory cells by the application of selected first or second
signal levels to addressing lines to the memory cells;
 - (d) an output buffer arranged to output the
data in one of the memory cells with a predetermined
10 address, by the operation of said address circuit; and
 - (e) a control circuit for inhibiting the data
output operation of said output buffer in response to a
first level of a control input signal;

wherein said address circuit includes a checking
15 address circuit for selecting none of said checking memory
cells when said control input signal is at a second level
and for selecting said checking memory cell with said
predetermined address in response to a third level of
said control input signal.
- 20 2. A memory device according to claim 1, wherein
said main memory cells are programmable ROMs.
3. A memory device according to claim 1 or 2,
wherein said control input signal is supplied from a chip
selecting input terminal.



- 24 -

4. A programmable read only memory device constructed and arranged to operate substantially as herein described with reference to and as illustrated in Figures 2 to 5 of the accompanying drawings.
