FIG. 1

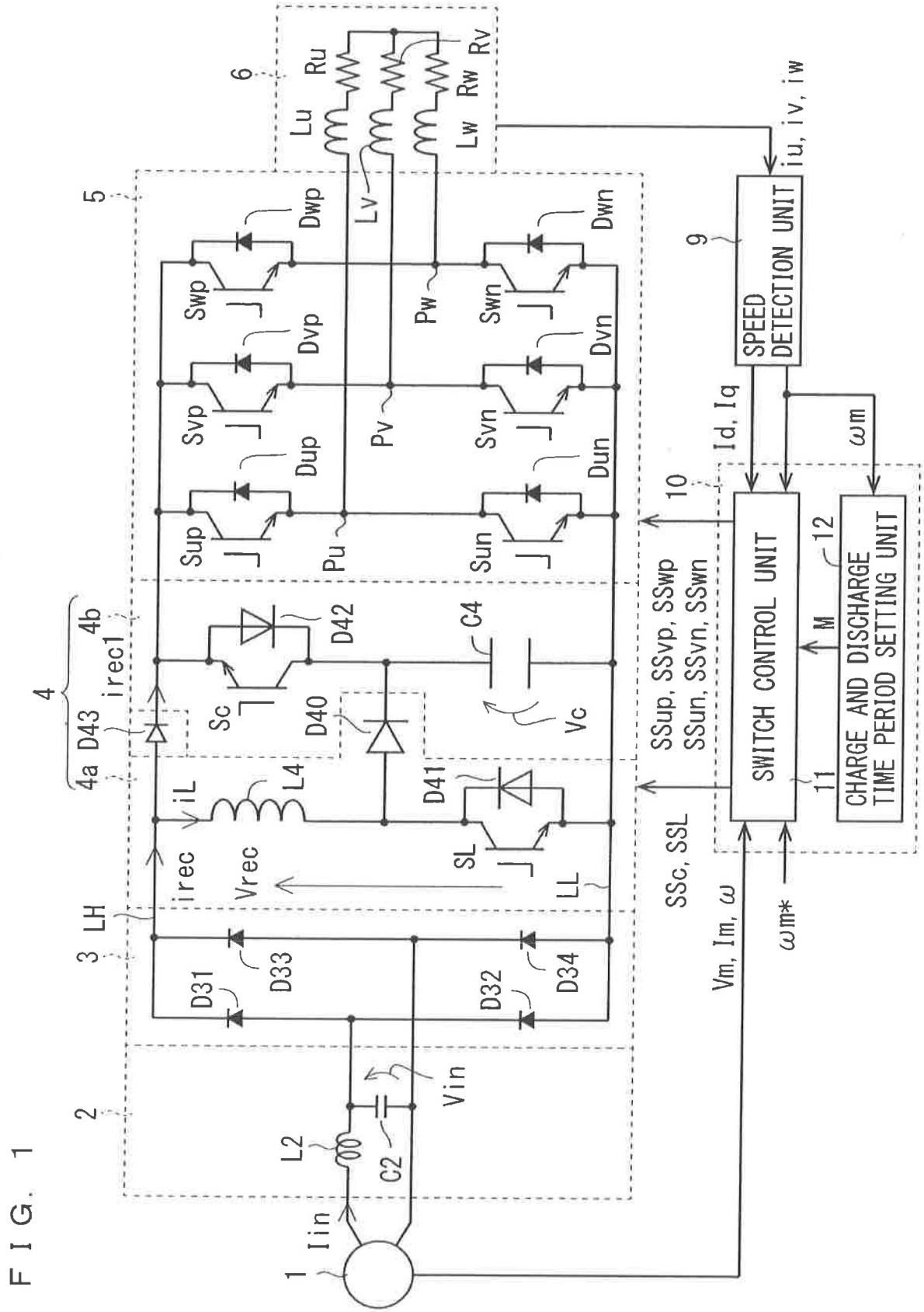

1
Iin
2
L2
C2
Vin
3 LH
D31
D33
D32
D34
4
4a D43
4b
irec1
D42
C4
Sc
D40
Vc
iL
L4
D41
irec
Vrec
SL
LL
5
Dwp
Swp
Dvp
Svp
Dup
Sup
Pu
Pv
Pw
Swn
Dwn
Dvn
Svn
Dun
Sun
6
Lu
Ru
Lv
Rv
Lw
Rw
9
SPEED DETECTION UNIT
iu, iv, iw
Id, Iq
ωm
10
SSup, SSvp, SSwp
SSun, SSvn, SSwn
SSc, SSL
SWITCH CONTROL UNIT
11
12
M
CHARGE AND DISCHARGE TIME PERIOD SETTING UNIT
Vm, Im, ω
ωm*

FIG. 2A

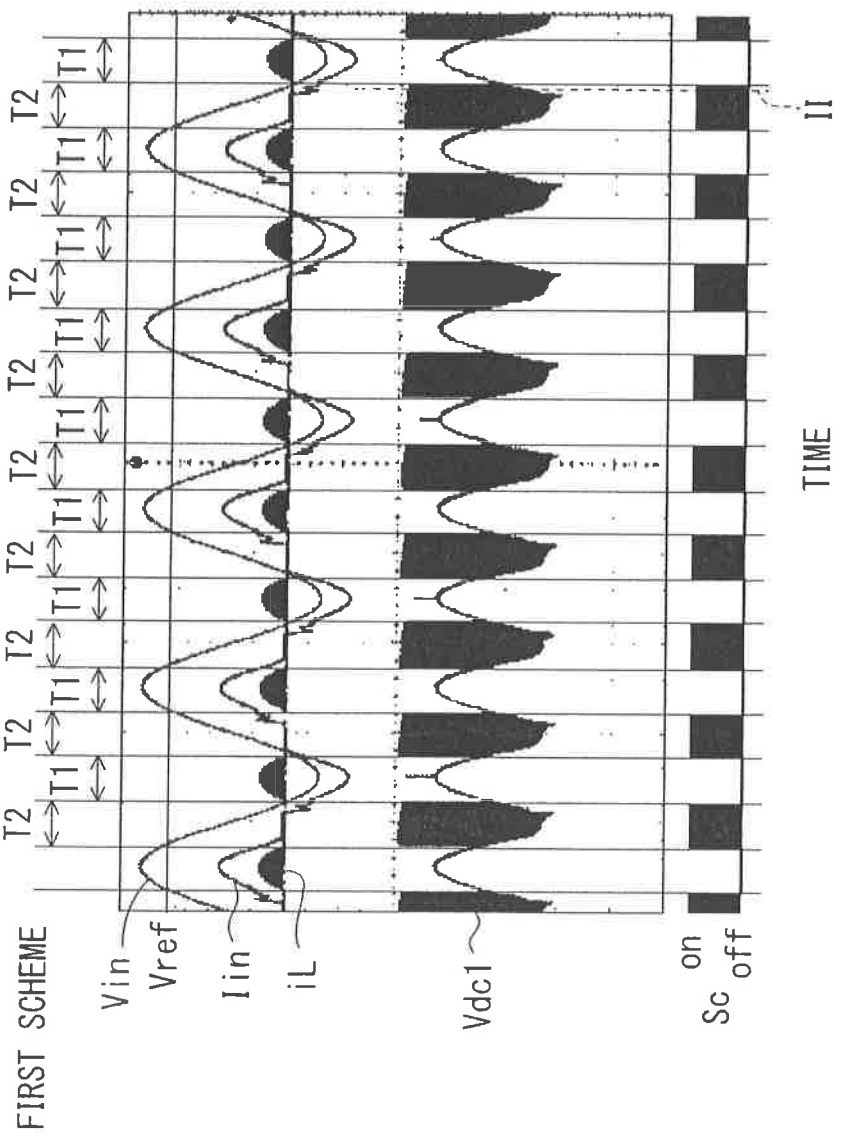

FIRST SCHEME
Vin
Vref
Iin
iL
Vdc1
Sc
on
off
T1
T2
II
TIME

FIG. 2B

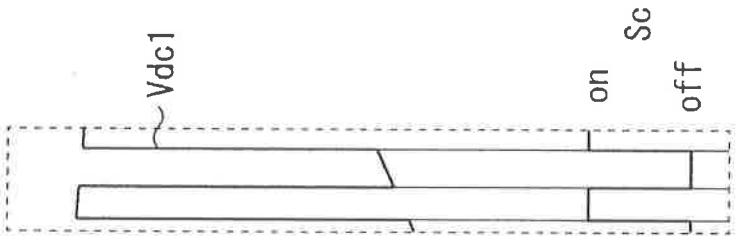

Vdc1
Sc
on
off

FIG. 3B

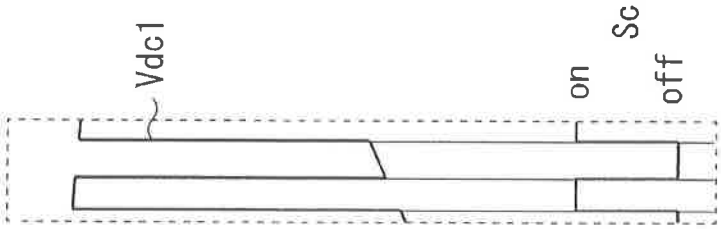

Vdc1
Sc
on
off

FIG. 3A

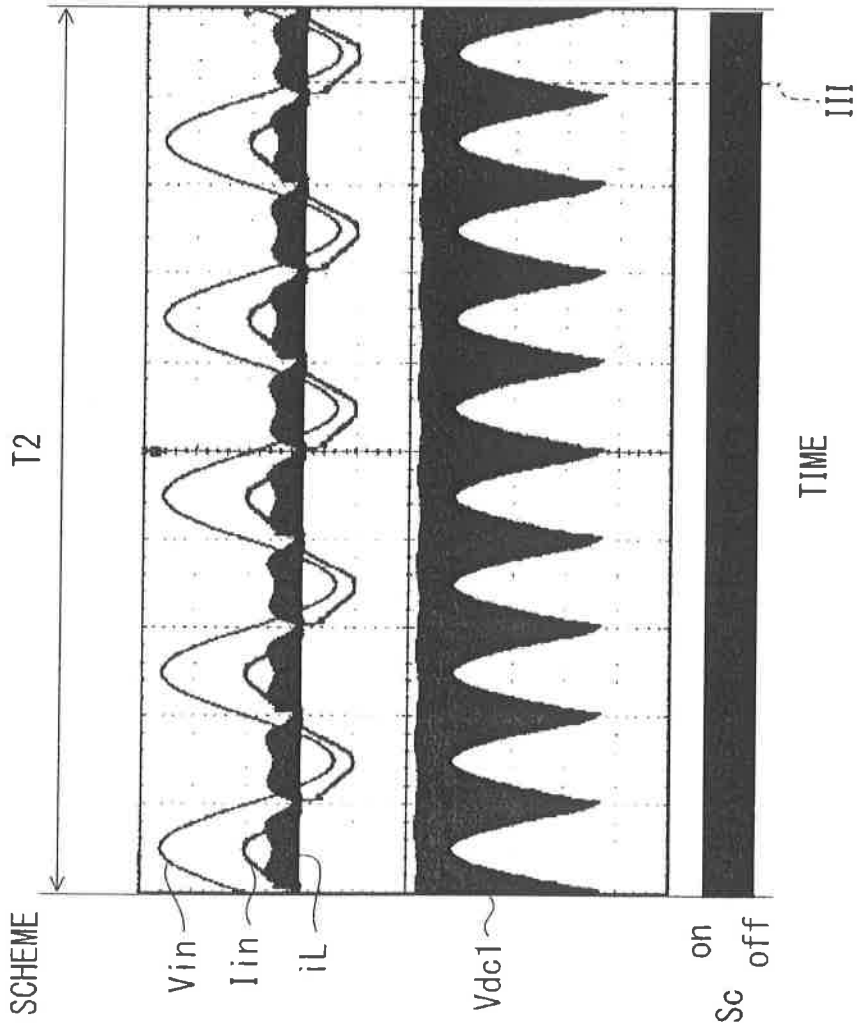

SECOND SCHEME
T2
Vin
Iin
iL
Vdc1
Sc
on
off
III
TIME

FIG. 4

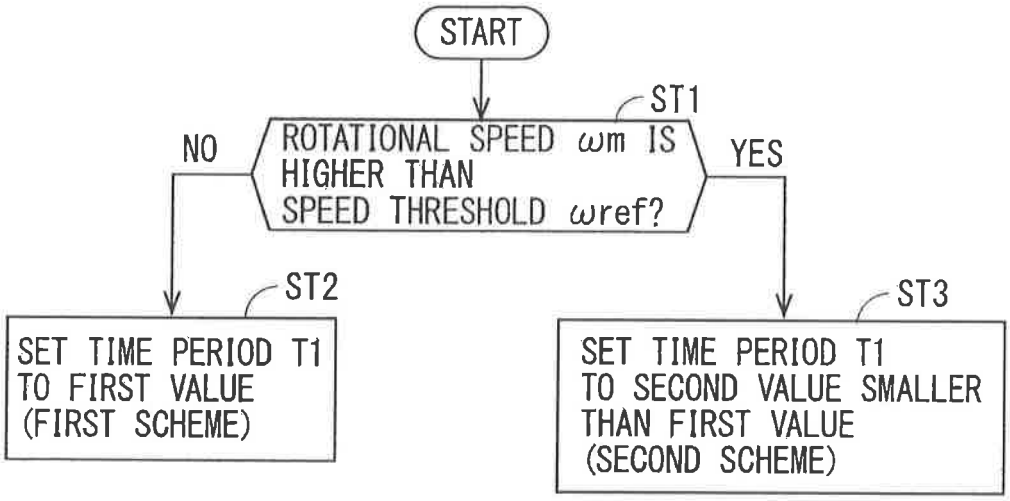


FIG. 5



FIG. 6

