A NANOWIRE DEVICE HAVING GRAPHENE TOP AND BOTTOM ELECTRODES AND METHOD OF MAKING SUCH A DEVICE

This invention concerns the use of thin graphitic layers as a transparent, conductive and flexible top contact electrode material for nanowire arrays preferably grown by a metal catalyst vapour-liquid-solid (VLS) method. In particular, the metal catalytic particles that remain on top of the nanowires after the nanowire growth are beneficially used as an intermediate material to enhance the electrical contact of nanowires to the top-contacted graphitic layers. The resulting array of nanowires, preferably composed of semiconductor materials, with a top-contact to the transparent, flexible graphitic layers have a wide range of applications in opto-electronic device applications including nanowire light-emitting diodes (LEDs) and nanowire solar cells.

Over recent years, the interest in semiconductor nanowires has intensified as nanotechnology becomes an important engineering discipline. Nanowires, which are also referred to as nanowhiskers, nanorods, nanopillars or nanocolumns etc by some authors, have found important applications in a variety of electrical devices such as sensors, solar cells to LED's.

For the purpose of this application, the term nanowire is to be interpreted as a structure being essentially in one-dimensional form, i.e. is of nanometer dimensions in its width or diameter and its length typically in the range of a few 100 nm to a few μm. Usually, nanowires are considered to have at least two dimensions not greater than 500 nm, such as not greater than 350 nm, especially not greater than 300 nm such as not greater than 200 nm.

Many different types of nanowires exist, including metallic (e.g., Ni, Pt, Au), semiconducting (e.g., Si, InP, GaN, GaAs, ZnO), and insulating (e.g., SiO_2, TiO_2) nanowires. The present inventors are primarily concerned with semiconductor nanowires although it is envisaged that the principles outlined in detail below are applicable to all manner of nanowire technology.

Conventionally, semi-conductor nanowires have been grown on a substrate identical to the nanowire itself (homoepitaxial growth). Thus GaAs nanowires are grown on GaAs substrates and so on. This, of course, ensures that there is a lattice match between the crystal structure of the substrate and the crystal structure of the

growing nanowire. Both substrate and nanowire can have identical crystal structures.

Growing a nanowire on a matching substrate is, however, expensive and limiting. For example, GaAs substrates need to be specifically manufactured and that is expensive. In order to ensure nanowire growth in the normally favoured [111]B direction, the substrate needs to be specially sliced to have (111)B oriented surface, as compared to the more normal substrate with (001) oriented surface. (111)B oriented GaAs substrates are more expensive than (001) oriented GaAs substrates. Also, GaAs is not the ideal material to carry a nanowire anyway. It is not mechanically strong or inert for example. It is not flexible or transparent. It would be better if other more attractive substrates could be employed.

The present inventors sought ways of using more substrates. Of course, doing so is not just a matter of using a different substrate. As soon as the substrate is different from the nanowire being grown then there is, by definition, a potential lattice mismatch between substrate and nanowire as well as numerous other possible problems to consider.

In one embodiment of the invention, the present inventors grow nanowires epitaxially on graphitic substrates. Graphitic substrates are substrates composed of single or multiple layers of graphene or its derivatives. In its finest form, graphene is a one atomic layer thick sheet of carbon atoms bound together with double electron bonds (called a sp^2 bond) arranged in a honeycomb lattice pattern. Unlike other semiconductor substrates, graphitic substrates are thin, light, and flexible, yet very strong.

They can be easily transferred onto any other substrates. Compared to other existing transparent conductors such as ITO, ZnO/Ag/ZnO, TiO_2/Ag/TiO_2, graphene has been proven to have superior opto-electrical properties as shown in a recent review article in Nature Photonics 4 (2010), 611.

For many applications it will be important that the nanowires can be grown vertically, perpendicular to the substrate surface. Semiconductor nanowires normally grow in the [111] direction (if cubic crystal structure) or the [0001] direction (if hexagonal crystal structure). This means that the substrate surface needs to be (111)

or (0001) oriented where the surface atoms of the substrate is arranged in a hexagonal symmetry.

The present inventors have found that epitaxial nanowires of certain compounds/elements can be grown on graphitic substrates. Since graphitic substrates have no dangling bonds at the surface and very short atomic bond length compared with typical semiconductors like silicon and GaAs, there is no reason to anticipate nucleation and epitaxial growth of nanowires thereon. As surprisingly noted below, there is a good lattice match with many semiconductors when using graphene depending on how the semiconductor atoms are placed on the surface of graphene.

In particular, the use of molecular beam epitaxy offers excellent results in terms of nanowire growth. In particular the invention enables the growth of group IV, II-VI or in particular group III-V semiconductor nanowires on graphitic substrates.

Even if nanowires can be grown on a substrate, there remains the problem of using those nanowires successfully in a device. If a nanowire is purely composed of semiconductors, it would naturally form a Schottky contact to metals depending on the work function of the contacted metal. So it is expected that the metallic graphitic layers contacted to semiconductors will also form a Schottky junction as demonstrated by S. Tongay et al. in Appl. Phys. Lett. 95 (2009), 222103. The formation of a non-ohmic, Schottky junction between graphitic layers and semiconductors is detrimental to the efficiency of devices such as LEDs and solar cells by blocking the proper current flow though contacts.

The present inventors sought a way of generating an ohmic top contact using graphitic layers as the material for the top-contact to semiconductor nanowire arrays vertically grown on substrates. In this way the advantageous properties of graphitic layers (as top contacts) in terms of flexibility and transparency can be combined with valuable electrical properties.

The present inventors have realised that the growth of semiconductor nanowires can involve metal catalyst particles. In particular, for the growth of nanowires using the molecular beam epitaxy (MBE) or metal organic vapour phase epitaxy (MOVPE) techniques, metal catalysts such as Au, Ga, or In are preferably

used as seeds for the growth of nanowires. The metal catalyst has the form of a nanoparticle that remains on top of each nanowire after completion of the nanowire growth. The present inventors have realised that metal catalysts deposited on the top of a growing nanowire can be used to make self-aligned ohmic contacts between grown nanowire arrays and graphitic layers as a top contact material.

It is worth noting that the mentioned top contact between graphitic layers and grown nanowires could be fundamentally different from the bottom contact between as-grown nanowires and substrates such as Si(111), GaAs (111), and especially graphitic substrates. Because nanowires are epitaxially grown involving physical and chemical bonding to substrates at high temperature, the bottom contact is expected to be much better and intimate, preferably ohmic.

There is limited discussion of this type of idea in the literature. Soo-Ghang Ihn *et al.*, IEEE Transactions on Nanotechnology 6 (2007), 384, report an observation of ohmic I-V curves in nanowires grown by Au-assisted MBE by contacting to the Au catalytic particle on top of single nanowire using an atomic force microscope tip.

Jung Min Lee et al., Nano Lett. 10 (2010), 2783 reports on the fabrication of vertical pillar-superlattice arrays and graphene hybrid LEDs. In this paper vertical arrays of GaAs nanopillars were made by "top-down" etching and graphene was used as a transparent top contact material. To evade from the expected Schottky contact between the top of semiconducting nanopillars and graphene, thin metal layers of Ti/Au (~ 4nm) were deposited onto the graphene. The metal-deposited side of graphene was used as the top contact to the nanopillars with a subsequent post-annealing. Due to the deposition of thin metal layers, the graphene top-contact suffers from a significant reduction of the transmittance from ~98 % for bare graphene to ~ 70 % for the metal/graphene contact.

In contrast to this, nanowires grown by a metal catalyst-assisted vapour-liquid-solid (VLS) "bottom-up" method naturally have a metallic nanoparticle left at the top. These metal nanoparticles can be used to facilitate the formation of self-aligned ohmic contacts to the graphitic layers with a possible post-annealing processes or doping of the graphitic layers. An added benefit of using such metallic particles as self–aligned contacts is that since the metallic particles are only

positioned at the nanowire/graphitic layer contact points, it would not affect the overall optical transparency of the top-contacted graphitic layers. The superior properties of the graphitic layers as a top contact material can be fully utilized in resulting opto-electronic devices.

Summary of Invention

Thus, viewed from one aspect the invention provides a composition of matter comprising a plurality of nanowires on a substrate, said nanowires having been grown epitaxially on said substrate in the presence of a metal catalyst, preferably in a vapour-liquid-solid method, such that a catalyst deposit is located at the top of at least some of said nanowires,

wherein said nanowires comprise at least one group III-V compound or at least one group II-VI compound or comprises at least one non carbon group IV element; and

wherein a graphitic layer is in contact with at least some of the catalyst deposits on top of said nanowires.

Viewed from another aspect the invention provides a process comprising:

(I) providing group II-VI elements or group III-V elements or at least one non carbon group IV element to the surface of a substrate, preferably via a molecular beam;

(II) epitaxially growing a plurality of nanowires from the surface of the substrate in the presence of a metal catalyst such that a catalyst deposit remains on the top of at least some of said nanowires;

(III) contacting said metal catalyst deposits with a graphitic layer a graphitic layer is in contact with at least some of the catalyst deposits on top of said nanowires.

Optionally, the surface of the substrate can be chemically/ physically modified to enhance the epitaxial growth of nanowires.

Viewed from another aspect the invention provides a device, such as an electronic device, comprising a composition as hereinbefore defined, e.g. a solar cell.

Definitions

By a group III-V compound is meant one comprising at least one ion from group III and at least one ion from group V. Similarly, a group II-VI compound is one comprising at least one group II ion and at least one group VI ion. In this application the term group (II) covers both classic group (IIa) and (IIb) periods, i.e. the alkaline earth series and the Zn series of elements. Group IV elements include Si and Ge. It will be appreciated that the term group IV element covers both a single group IV element and also the presence of two such elements which may combine to form a compound such as SiC or SiGe. There may be more than one ion present from each group, e.g. InGaAs and so on. Non carbon group IV nanowires are those that contain at least one non carbon group IV element only, for example a Si nanowire or SiC nanowire.

The term semiconducting nanowire is meant nanowire made of semiconducting materials from group II-VI elements or group III-V elements or group IV element.

The term nanowire is used herein to describe a solid, wire like structure of nanometer dimensions. Nanowires preferably have an even diameter throughout the majority of the nanowire, e.g. at least 75% of its length. The term nanowire is intended to cover the use of nanorods, nanopillars, nanocolumns or nanowhiskers some of which may have tapered end structures. The nanowires can be said to be in essentially in one-dimensional form with nanometer dimensions in their width or diameter and their length typically in the range of a few 100 nm to a few μm. Ideally the nanowire diameter is not greater than 500 nm. Typically, the nanowire will have two dimensions not greater than 500 nm, such as not greater than 350 nm, especially not greater than 300 nm, such as not greater than 200 nm.

Ideally, the diameter at the base of the nanowire and at the top of the nanowire should remain about the same (e.g. within 20% of each other). It will be appreciated that the wire has to narrow at the very top, typically forming a hemisphere.

It will be appreciated that the substrate comprises a plurality of nanowires. This may be called an array of nanowires.

Graphitic layers for substrates or top contacts are films composed of single or multiple layers of graphene or its derivatives. The term graphene refers to a planar sheet of sp^2-bonded carbon atoms in a honeycomb crystal structure. Derivatives of graphene are those with surface modification. For example, the hydrogen atoms can be attached to the graphene surface to form graphane. Graphene with oxygen atoms attached to the surface along with carbon and hydrogen atoms is called as graphene oxide. The surface modification can be also possible by chemical doping or oxygen/hydrogen plasma treatment.

The term epitaxy comes from the Greek roots epi, meaning "above", and taxis, meaning "in ordered manner". The atomic arrangement of the nanowire is based on the crystallographic structure of the substrate. It is a term well used in this art. Epitaxial growth means herein the growth on the substrate of a nanowire that mimics the orientation of the substrate.

Metal catalyst-assisted vapour-liquid-solid (VLS) method is a method to grow nanowires from metal catalysts which act as nucleation sites for the growth of nanowires. The metal catalysts are provided by depositing a thin layer of catalytic material over the substrate surface, which would be melted into nano-sized particles by increasing the temperature for the nanowire growth.

The term catalyst deposit refers to the catalyst material that remains on top of the growing nanowire. It can be considered a nanoparticle of catalyst.

Molecular beam epitaxy (MBE) is a method of forming depositions on crystalline substrates. The MBE process is performed by heating a crystalline substrate in a vacuum so as to energize the substrate's lattice structure. Then, an atomic or molecular mass beam(s) is directed onto the substrate's surface. The term element used above is intended to cover application of atoms, molecules or ions of that element. When the directed atoms or molecules arrive at the substrate's surface, the directed atoms or molecules encounter the substrate's energized lattice structure or a catalyst droplet as described in detail below. Over time, the oncoming atoms form a nanowire.

Detailed Description of Invention

This invention concerns the use of graphitic layers as a top contact electrode material to semiconductor nanowire arrays epitaxially grown in the presence of a metal catalyst, ideally via a metal catalyst-assisted vapour-liquid-solid (VLS) method. Ideally, the graphitic layer is transparent, conductive and flexible. The semiconductor nanowire array comprises a plurality of nanowires grown epitaxially on a substrate.

Having a nanowire grown epitaxially provides homogeneity to the formed material which may enhance various end properties, e.g. mechanical, optical or electrical properties.

Epitaxial nanowires may be grown from gaseous or liquid precursors. Because the substrate acts as a seed crystal, the deposited nanowire can take on a lattice structure and orientation identical to those of the substrate. This is different from other thin-film deposition methods which deposit polycrystalline or amorphous films, even on single-crystal substrates.

Substrate for nanowire growth

The substrate used to grow nanowires of the invention can be any convenient substrate such as semiconductor substrates. Semiconductor substrates used for epitaxial and vertical growth of nanowires may have the same type of crystal structure and crystal orientation as the base of the nanowire, as well as a close lattice match. They can be silicon or GaAs substrates such as with (111) oriented surface where the nanowires can be grown perpendicular to the substrates in the [111] (for cubic crystal structure) or [0001] (for hexagonal crystal structure) direction. GaAs (111) and Si (111) are especially preferred substrates.

Semiconductor substrates of interest are therefore based on group II-VI elements or group III-V elements or at least one non carbon group IV element, for example.

The substrate is preferably a graphitic substrate, more especially it is graphene. As used herein, the term graphene refers to a planar sheet of sp^2-bonded carbon atoms that are densely packed in a honeycomb (hexagonal) crystal lattice. This graphene substrate should contain no more than 10 layers of graphene or its derivatives, preferably no more than 5 layers (which is called as a few-layered graphene). Especially preferably, it is a one-atom-thick planar sheet of graphene.

The crystalline or "flake" form of graphite consists of many graphene sheets stacked together (i.e. more than 10 sheets). By graphitic substrate therefore, is meant one formed from one or a plurality of graphene sheets.

It is preferred if the substrate in general is 20 nm in thickness or less. Graphene sheets stack to form graphite with an interplanar spacing of 0.335 nm. The graphitic substrate preferred comprises only a few such layers and may ideally be less than 10 nm in thickness. Even more preferably, the graphitic substrate may be 5 nm or less in thickness. The area of the substrate in general is not limited. This might be as much as 0.5 mm^2 or more, e.g. up to 5 mm^2 or more such as up to 10 cm^2. The area of the substrate is thus only limited by practicalities.

The substrate may need to be supported in order to allow growth of the nanowires thereon, especially where that substrate is graphitic. The substrate can be supported on any kind of materials including conventional semiconductor substrates and transparent glasses. The use of silica or SiC is preferred. The support must be inert.

In a highly preferred embodiment, the substrate is a laminated substrate exfoliated from a Kish graphite, a single crystal of graphite or is a highly ordered pyrolytic graphite (HOPG). Alternatively, the substrate could be grown on a Ni film or Cu foil by using a chemical vapour deposition (CVD) method, which can be easily purchased from "Graphene supermarket", USA. The substrate could be a chemical vapour deposition (CVD)-grown graphene substrate on metallic films or foils made of e.g. Cu, Ni, or Pt.

These CVD-grown graphitic layers can be chemically exfoliated from the metal foil such as a Ni or Cu film by etching or by an electrochemical delamination method. The graphitic layers after exfoliation are then transferred and deposited to the supporting substrates for nanowire growth. During the exfoliation and transfer,

e-beam resist or photoresist may be used to support the thin graphene layers. These supporting materials can be easily removed by acetone after deposition.

Whilst it is preferred if the graphitic substrate is used without modification, the surface of the graphitic substrate can be modified. For example, it can be treated with plasma of hydrogen, oxygen, NO_2 or their combinations. Oxidation of the substrate might enhance nanowire nucleation. It may also be preferable to pretreat the substrate, for example, to ensure purity before nanowire growth. Treatment with a strong acid such as HF or BOE is an option. Substrates might be washed with iso-propanol, acetone, or n-methyl-2-pyrrolidone to eliminate surface impurities.

The cleaned graphitic surface can be further modified by doping. Dopant atoms or molecules may act as a seed for growing nanowires. A solution of $FeCl_3$, $AuCl_3$ or $GaCl_3$ could be used in a doping step.

The graphitic layers, more preferably graphene, are well known for their superior optical, electrical and mechanical properties. They are very thin but very strong, light, flexible, and impermeable. Most importantly in the present invention they are highly electrically and thermally conducting, flexible and transparent. Compared to other transparent conductors such as ITO, ZnO/Ag/ZnO, and TiO_2/Ag/TiO_2 which are commercially used now, graphene has been proven to be much more transparent (~ 98 % transmittance in the solar spectral range of interest from 250 to 900 nm in wavelength) and conducting (< 1000 Ohm sheet resistance for 1 nm thickness).

Growth of Nanowires

In order to prepare nanowires of commercial importance, it is essential that these grow epitaxially on the substrate. It is also ideal if growth occurs perpendicular to the substrate and ideally therefore in the [111] (for cubic crystal structure) or [0001] (for hexagonal crystal structure) direction. We noted above that this can be achieved using a substrate which is formed from the same material as the growing nanowires by providing the substrate cut in an appropriate fashion.

As noted above, there is no guarantee that this is possible with a particular substrate where that substrate material is different from the nanowire being grown.

The present inventors have determined, however, that epitaxial growth on graphitic substrates is possible by determining a possible lattice match between the atoms in the semiconductor nanowire and the carbon atoms in the graphene sheet.

The carbon-carbon bond length in graphene layers is about 0.142 nm. Graphite has hexagonal crystal geometry. This is shown in figure 1a. The present inventors have surprisingly realised that graphite can provide a substrate on which semiconductor nanowires can be grown as the lattice mismatch between the growing nanowire material and the graphitic substrate can be very low.

The inventors have realised that due to the hexagonal symmetry of the graphitic substrate and the hexagonal symmetry of the semiconductor atoms in the (111) planes of a nanowire growing in the [111] direction with a cubic crystal structure (or in the (0001) planes of a nanowire growing in the [0001] direction with a hexagonal crystal structure), a lattice match can be achieved between the growing nanowires and the substrate.

Figures 1a-1d show four different hexagonal structural configurations of the semiconductor atoms in the (111) (or (0001)) planes of a nanowire on top of the hexagonal lattice of carbon atoms in the graphene layer, placed in such a way that no lattice mismatch will occur. As possible semiconductor adsorption sites on top of graphene, we consider 1) above the center of the hexagonal carbon rings of graphene (H-site) and 2) above the bridge between carbon atoms (B-site), as indicated by arrows in figure 1a.

The figures show an idealised lattice-matched arrangement of the semiconductor atoms in the (111) planes of a cubic crystal ((0001) planes for hexagonal) when the atoms are placed on 1) H- and B-sites (figures 1a, 1b and 1d), and 2) H- or B-sites (figure 1c). Dashed lines emphasize the hexagonal symmetry of the lattice of semiconductor atoms in the (111) plane. The relative rotations of these hexagons for each atomic arrangement are written on the top of each figure. For (figure 1a) and (figure 1d) two relative orientations are possible, ±10.9° and ±16.1°, respectively (only the + rotations are shown in the images).

Figure 1e shows artificial lattice-matched lattice constants for the atomic arrangements in (a), (b), (c) and (d). Dashed and solid lines correspond to the hexagonal (a_1) and cubic ($a = a_1 \times \sqrt{2}$) crystal phases of these lattices, respectively.

The square (■) and the hexagon represent the cubic and the hexagonal phases, respectively, for Si, ZnO, and group III-V semiconductors. Squares (GaAs, AlAs, AlSb) with two different colours indicate that the semiconductor can adopt either of two atomic arrangements on graphene. The figure visualizes the vast possibilities for epitaxial growth of vertical semiconductor nanowires on graphitic substrates.

If the semiconductor atoms are placed above alternating H- and B-sites as in figure 1a, an exact lattice match can be achieved if the lattice constant, a, of a cubic semiconductor crystal (the lattice constant, a, is defined as the side length of the cubic unit cell) is equal to: 4.607 Å. A few cubic semiconductors exist with lattice constants close to this value, with the closest being SiC (a = 4.36 Å), AlN (a = 4.40 Å) and GaN (a = 4.51 Å). For hexagonal semiconductor crystals, exact lattice matches will be achieved if the lattice constant, a_1, is equal to: 3.258 Å. A few hexagonal semiconductors exist with lattice constants close to this value, with the closest being SiC (a_1 = 3.07 Å), AlN (a_1 = 3.11 Å), GaN (a_1 = 3.19 Å) and ZnO (a_1 = 3.25 Å) crystals.

If the semiconductor atoms are placed above alternating H- and B-sites as in figure 1b, an exact lattice match can be achieved if the lattice constant, a, of a cubic semiconductor crystal is equal to: 1.422 Å (carbon atom distance) x 3/2 x sqr(6) = 5.225 Å. This is close to the lattice constant of Si (a = 5.43 Å), GaP (a = 5.45 Å), AlP (a = 5.45 Å), InN (a = 4.98 Å) and ZnS (a = 5.42 Å). For hexagonal semiconductor crystals exact lattice matches will be achieved if the lattice constant, a_1, is equal to: 1.422 Å x 3/2 x sqr(3) = 3.694 Å. This is close to the a_1 lattice constants of the hexagonal forms of InN (a_1 = 3.54 Å) and ZnS (a_1 = 3.82 Å) crystals.

For the atomic configuration as in figure 1c an exact lattice match can be achieved if the lattice constant, a, of a cubic semiconductor crystal is equal to: 1.422 Å (carbon atom distance) x 3 x sqr(2) = 6.033 Å. This is close to the lattice constant of group III-V compounds such as InAs, GaAs, InP, GaSb, AlSb and AlAs, and II-VI compounds such as MgSe, ZnTe, CdSe, and ZnSe semiconductor crystals. In particular, this is close to the lattice constant of group III-V compounds such as InAs (a = 6.058 Å), GaSb (a = 6.096 Å) and AlSb (a = 6.136 Å), and II-VI compounds such as ZnTe (a = 6.103 Å) and CdSe (a = 6.052 Å) semiconductor crystals.

For hexagonal semiconductor crystals, exact lattice matches will be achieved if the lattice constant, a_1, is equal to: 1.422 Å (carbon atom distance) x 3 = 4.266 Å. This is close to the a_1 lattice constants of the hexagonal forms of the II-VI materials CdS (a_1 = 4.160 Å) and CdSe (a_1 = 4.30 Å) crystals.

If the semiconductor atoms are placed above alternating H- and B-sites as in figure 1d, an exact lattice match can be achieved if the lattice constant, a, of a cubic semiconductor crystal is equal to: 6.28 Å. This is close to the lattice constant of InSb (a = 6.479 Å), MgTe (a = 6.42 Å) and CdTe (a = 6.48 Å). For hexagonal semiconductor crystals, exact lattice matches will be achieved if the lattice constant, a_1, is equal to: 4.44 Å. This is close to the a_1 lattice constants of the hexagonal forms of InSb (a_1 = 4.58 Å), MgTe (a_1 = 4.54 Å) and CdTe (a_1 = 4.58 Å) crystals.

Without wishing to be limited by theory, due to the hexagonal symmetry of the carbon atoms in graphitic layers, and the hexagonal symmetry of the atoms of cubic or hexagonal semiconductors in the [111] and [0001] crystal direction, respectively, (a preferred direction for most nanowire growth), a close lattice match between the graphitic substrate and semiconductor can be achieved when the semiconductor atoms are placed above the carbon atoms of the graphitic substrate, ideally in a hexagonal pattern. This is a new and surprising finding and can enable the epitaxial growth of nanowires on graphitic substrates.

The four different hexagonal arrangements of the semiconductor atoms as described above, can enable semiconductor nanowires of such materials to be vertically grown to form free standing nanowires on top of a thin carbon-based graphitic material.

Whilst it is ideal that there is no lattice mismatch between a growing nanowire and the substrate, nanowires can accommodate much more lattice mismatch than thin films for example. The nanowires of the invention may have a lattice mismatch of up to about 10% with the substrate and epitaxial growth is still possible. Ideally, lattice mismatches should be 7.5% or less, e.g. 5% or less.

For some semiconductors like cubic InAs (a = 6.058 Å), cubic GaSb (a = 6.093 Å), cubic CdSe (a = 6.052 Å), and hexagonal CdSe (a_1= 4.30 Å) the lattice mismatch is so small (< ~1%) that excellent growth of these semiconductors can be expected.

For some semiconductors like GaAs (a = 5.653 Å) the lattice mismatch is quite similar when the semiconductor atoms are placed on the same sites as in figure 1a (a = 6.033Å and thus the lattice constant for GaAs is 6.3% smaller), or alternating H- and B-sites as in figure 1b (a = 5.255 Å and thus the lattice constant for GaAs is 8.2% larger), that both arrangements are possible. The process of the invention can enable semiconductor nanowires of the above mentioned materials to be vertically grown to form free standing nanowires on top of a thin carbon-based graphitic material as well as conventional substrates such as semi-conductors.

The nanowire grown in the present invention may be from 250 nm to several microns in length, e.g. up to 5 microns. Preferably the nanowires are at least 1 micron in length. Where a plurality of nanowires are grown, it is preferred if they all meet these dimension requirements. Ideally, at least 90% of the nanowires grown on a substrate will be at least 1 micron in length. Preferably substantially all the nanowires will be at least 1 micron in length.

Moreover, it will be preferred if the nanowires grown have the same dimensions, e.g. to within 10% of each other. Thus, at least 90% (preferably substantially all) of the nanowires on a substrate will preferably be of the same diameter and/or the same length (i.e. to within 10% of the diameter/length of each other). Essentially, therefore the skilled man is looking for homogeneity and nanowires than are substantially the same in terms of dimensions.

The length of the nanowires is often controlled by the length of time for which the growing process runs. A longer process typically leads to a (much) longer nanowire.

The nanowires have typically a hexagonal cross sectional shape. The nanowire may have a cross sectional diameter of 25 to 200 nm (i.e. its thickness). As noted above, the diameter is ideally constant throughout the majority of the nanowire. Nanowire diameter can be controlled by the manipulation of the ratio of the atoms used to make the nanowire as described further below.

Moreover, the length and diameter of the nanowires can be affected by the temperature at which they are formed. Higher temperatures encourage high aspect ratios (i.e. longer and/or thinner nanowires). The skilled man is able to manipulate the growing process to design nanowires of desired dimensions.

The nanowires of the invention are formed from at least one III-V compound, at least one II-VI compound or they can be nanowires grown from at least one group IV element selected from Si, Ge, Sn or Pb, especially Si and Ge. The formation therefore of pure group IV nanowires or nanowires such as SiC and SiGe is envisaged.

Group II elements are Be, Mg, Ca, Zn, Cd, and Hg. Preferred options here are Zn and Cd.

Group III options are B, Al, Ga, In, and Tl. Preferred options here are Ga, Al and In.

Group V options are N, P, As, Sb. All are preferred.

Group VI options include O, S, Se and Te. The use of Se and Te is preferred.

The manufacture of a group III-V compound is preferred. It will be appreciated that any compound which forms during nanowire growth need not be completely stoichiometric as the possibility of doping exists, as discussed below.

Preferred compounds for nanowire manufacture include AlAs, ZnO, GaSb, GaP, GaN, GaAs, InP, InN, InGaA, InAs, or AlGaAs or InAs, GaAs, InP, GaSb, InSb, GaP, ZnTe, SiC, CdSe and ZnSe, such as InAs, GaAs, InP, GaSb, InSb, GaP, ZnTe, CdSe and ZnSe . The use of GaAs or InAs is highly preferred. Other options include Si, ZnO, GaN, AlN and InN.

Whilst the use of binary materials is preferred, there is no reason why ternary or quaternary nanowires etc. cannot be grown by the method of the invention. Thus, ternary systems in which there are two group III cations with a group V anion are an option here, such as InGaAs and AlGaAs. The ternary compounds may therefore be of formula XYZ wherein X is a group III element, Y is a group III or V element different from X and Z, and Z is a group V element. The X to Y or Y to Z molar ratio in XYZ is preferably 0.1 to 0.9, i.e. the formula is preferably $X_xY_{1-x}Z$ (or $XY_{1-x}Z_x$) where subscript x is 0.1 to 0.9. Quaternary systems may be represented by the formula $A_xB_{1-x}C_yD_{1-y}$ where A and B are group III elements and C and D are group V elements. Again subscripts x and y are typically 0.1 to 0.9. Other options will be clear to the skilled man.

It is within the scope of the invention for the nanowires to be doped. Doping typically involves the introduction of impurity ions into the nanowire, e.g. during MBE growth. The doping level can be controlled from ~ $10^{15}/cm^3$ to $10^{20}/cm^3$. The nanowires can be undoped (intrinsic), p-doped or n-doped as desired. Doped semiconductors are extrinsic conductors whereas undoped ones are intrinsic.

The n(p)-type semiconductors have a larger electron (hole) concentration than hole (electron) concentration by doping an intrinsic semiconductor with donor (acceptor) impurities. Suitable donor (acceptors) for III-V compounds can be Te (Be and Zn). Si can be amphoteric, either donor or acceptor depending on the site where Si goes to, depending on the orientation of the growing surface and the growth conditions. Dopants can be introduced during the growth process or by ion implantation of the nanowires after their formation.

The nanowires of the invention can be grown to have a heterostructured form radially or axially. For example for an axial heterostructured nanowire, p-n junction can be axially formed by growing a p-type doped core first, and then continue with an n-doped core. For an radially heterostructured nanowire, p-n junction can be radially formed by growing the p-doped nanowire core first, and then the n-doped semiconducting shell is grown.

The nanowires of the invention grow epitaxially. They attach to the underlying substrate through covalent, ionic or quasi van der Waals binding. Accordingly, at the junction of the substrate and the base of the nanowire, crystal planes are formed epitaxially within the nanowire. These build up, one upon another, in the same crystallographic direction thus allowing the epitaxial growth of the nanowire. Preferably the nanowires grow vertically. The term vertically here is used to imply that the nanowires grow perpendicular to the support. It will be appreciated that in experimental science the growth angle may not be exactly 90° but the term vertically implies that the nanowires are within about 10° of vertical/perpendicular, e.g. within 5°. Because of the epitaxial growth via covalent, ionic or quasi van der Waals bonding, it is expected that there will be an intimate contact between the nanowires and the substrate, especially graphitic substrate. To enhance the contact property further, the substrate, such as the graphitic substrate can be doped to match the major carriers of grown nanowires.

Because nanowires are epitaxially grown involving physical and chemical bonding to substrates at high temperature, the bottom contact is preferably ohmic.

It will be appreciated that the substrate comprises a plurality of nanowires. Preferably the nanowires grow about parallel to each other. It is preferred therefore if at least 90%, e.g. at least 95%, preferably substantially all nanowires grow in the same direction from the same plane of the substrate.

It will be appreciated that there are many planes within a substrate from which epitaxial growth could occur. It is preferred if substantially all nanowires grow from the same plane. It is preferred if that plane is parallel to the substrate surface. Ideally the grown nanowires are substantially parallel. Preferably, the nanowires grow substantially perpendicular to the substrate.

The nanowires of the invention should preferably grow in the [111] direction for nanowires with cubic crystal structure and [0001] direction for nanowires with hexagonal crystal structure. If the crystal structure of the growing nanowire is cubic, then the (111) interface between the nanowire and the catalyst droplet represents the plane from which axial growth takes place. If the nanowire has a hexagonal crystal structure, then the (0001) interface between the nanowire and the catalyst droplet represents the plane from which axial growth takes place. Planes (111) and (0001) both represent the same (hexagonal) plane of the nanowire, it is just that the nomenclature of the plane varies depending on the crystal structure of the growing nanowire.

The nanowires are preferably grown by molecular beam epitaxy (MBE). Whilst it is possible to use metal organic vapour phase epitaxy (MOVPE), the use of MBE is preferred. In this method, the substrate is provided with a molecular beam of each reactant, e.g. a group III element and a group V element preferably supplied simultaneously. A higher degree of control of the nucleation and growth of the nanowires on the graphitic substrate might be achieved with the MBE technique by using migration-enhanced epitaxy (MEE) or atomic-layer MBE (ALMBE) where e.g. the group III and V elements can be supplied alternatively.

A preferred technique is solid-source MBE, in which very pure elements such as gallium and arsenic are heated in separate effusion cells, until they begin to slowly evaporate (e.g. gallium) or sublimate (e.g. arsenic). The gaseous elements

then condense on the substrate, where they may react with each other. In the example of gallium and arsenic, single-crystal GaAs is formed. The use of the term "beam" implies that evaporated atoms (e.g. gallium) or molecules (e.g. As_4 or As_2) do not interact with each other or vacuum chamber gases until they reach the substrate.

Doping ions can also be introduced easily using MBE. Figure 2 is a possible set up of a MBE machine.

MBE takes place in ultra high vacuum, with a background pressure of typically around 10^{-10} to 10^{-9} Torr. Nanostructures are typically grown slowly, such as at a speed of up to a few, such as about 10, μm per hour. This allows nanowires to grow epitaxially and maximises structural performance.

Catalyst

The nanowires of the invention are grown in the presence of a catalyst. The catalyst can be one of the elements making up the nanowire - so called self catalysed, or different from any of the elements making up the nanowire.

For catalyst-assisted growth the catalyst may be Au or Ag or the catalyst may be a metal from the group used in the nanowire growth (e.g. group II or III metal), especially one of the metal elements making up the actual nanowire (self catalysis). It is thus possible to use another element from group III as a catalyst for growing a III-V nanowire e.g. use Ga as a catalyst for an In (group V) nanowire and so on. Preferably the catalyst is Au or the growth is self catalysed (i.e. Ga for a Ga (group V) nanowire and so on). The catalyst can be deposited onto the substrate to act as a nucleation site for the growth of the nanowires. Ideally, this can be achieved by providing a thin film of catalytic material formed over the substrate surface. When the catalyst film is melted (often forming a eutectic alloy with one or more of the semiconductor nanowire constituents) as the temperature increases to the growth temperature, it forms nanometre sized particle-like droplets on the substrate and these droplets form the points where nanowires can grow. This is called vapour-liquid-solid growth (VLS) as the catalyst is the liquid, the molecular beam is the vapour and the nanowire provides the solid component. In some cases the catalyst

particle can also be solid during the nanowire growth, by a so called vapour-solid-solid growth (VSS) mechanism. As the nanowire grows (by the VLS method), the liquid (e.g. gold) droplet stays on the top of the nanowire. This is depicted in the figures. It remains at the top of the nanowire after growth and may therefore play a major role in contacting top graphitic layers as discussed herein.

As noted above, it is also possible to prepare self catalysed nanowires. By self catalysed is meant that one of the components of the nanowire acts as a catalyst for its growth.

For example, a Ga layer can be applied to the substrate, melted to form droplets acting as nucleation sites for the growth of Ga containing nanowires. Again, a Ga metal portion may end up positioned on the top of the nanowire. A similar process can be effected using group II or group III metals as catalysts for nanowires containing the catalyst as a component.

In more detail, a Ga/In flux can be supplied to the substrate surface for a period of time to initiate the formation of Ga/In droplets on the surface upon heating of the substrate. The substrate temperature can then be set to a temperature suitable for the growth of the nanowire in question. The growth temperature may be in the range 300 to 700°C. The temperature employed is, however, specific to the nature of the material in the nanowire, the catalyst material and the substrate material. For GaAs, a preferred temperature is 540 to 630°C, e.g. 590 to 630 °C, such as 610°C. For InAs the range is lower, for example 420 to 540°C, such as 430 to 540°C, e.g. 450°C.

Nanowire growth can be initiated by opening the shutter of the Ga/In effusion cell and the counter ion effusion cell, simultaneously once a catalyst film has been deposited and melted.

The temperature of the effusion cells can be used to control growth rate. Convenient growth rates, as measured during conventional planar (layer by layer) growth, are 0.05 to 2 μm per hour, e.g. 0.1 μm per hour.

The pressure of the molecular beams can also be adjusted depending on the nature of the nanowire being grown. Suitable levels for beam equivalent pressures are between 1×10^{-7} and 1×10^{-5} Torr.

The beam flux ratio between reactants (e.g. group III atoms and group V molecules) can be varied, the preferred flux ratio being dependent on other growth parameters and on the nature of the nanowire being grown.

It has been found that the beam flux ratio between reactants can affect crystal structure of the nanowire. For example, using Au as a catalyst, growth of GaAs nanowires with a growth temperature of 540 °C, a Ga flux equivalent to a planar (layer by layer) growth rate of 0.6 μm per hour, and a beam equivalent pressure (BEP) of 9×10^{-6} Torr for As_4 produces wurtzite crystal structure. As opposed to this, growth of GaAs nanowires at the same growth temperature, but with a Ga flux equivalent to a planar growth rate of 0.9 μm per hour and a BEP of 4×10^{-6} Torr for As_4, produces zinc blende crystal structure.

Nanowire diameter can in some cases be varied by changing the growth parameters. For example, when growing self-catalyzed GaAs nanowires under conditions where the axial nanowire growth rate is determined by the As_4 flux, the nanowire diameter can be increased/decreased by increasing/decreasing the Ga:As_4 flux ratio. The skilled man is therefore able to manipulate the nanowire in a number of ways.

It is thus an embodiment of the invention to employ a multistep, such as two step, growth procedure, e.g. to separately optimize the nanowire nucleation and nanowire growth.

A significant benefit of MBE is that the growing nanowire can be analysed *in situ*, for instance by using reflection high-energy electron diffraction (RHEED). RHEED is a technique typically used to characterize the surface of crystalline materials. This technology cannot be applied so readily where nanowires are formed by other techniques such as MOVPE.

One limitation of the techniques described above is that there is limited control over where nanowires grow on the surface of the substrate. Nanowires will grow where a catalyst droplet forms but there is little control over where those droplets might form. A further problem is that the size of the droplets cannot easily be controlled. If droplets form which are too small to initiate nucleation of a nanowire, yields of nanowires may be low. This is a particular problem when using

gold catalysis as the droplets formed by the gold can be too small to allow high yielding nanowire growth.

In order to prepare a more regular array of nanowires with better homogeneity in height and diameter of grown nanowires, the inventors envisage the use of a mask on the substrate. This mask can be provided with regular holes, where nanowires can grow homogeneously in size in a regular array across the substrate. The hole patterns in the mask can be easily fabricated using conventional photo/e-beam lithography or nanoimprinting. Focussed ion beam technology may also be used in order to create a regular array of nucleation sites on the graphitic surface for the nanowire growth.

Thus a mask can be applied to the substrate and etched with holes exposing the substrate surface, optionally in a regular pattern. Moreover, the size of the holes can be carefully controlled. Catalyst can then be introduced into those holes to provide nucleating sites for nanowire growth. By arranging the holes regularly, a regular pattern of nanowires can be grown.

Moreover, the size of the holes can be controlled to ensure that only one nanowire can grow in each hole. Finally, the holes can be made of a size where the droplet of catalyst that forms within the hole is sufficiently large to allow nanowire growth. In this way, a regular array of nanowires can be grown, even using Au catalysis.

The mask material can be any materials which do not damage the underlying substrate when deposited. The holes used in this embodiment may be slightly bigger than the nanowire diameter, e.g. up to 200 nm. The minimum hole size might be 50 nm, preferably at least 100-200 nm. The thickness of the mask can be 50 to 300 nm.

The mask itself can be made of an inert compound, such as silicon dioxide or silicon nitride. In particular, the hole-patterned mask comprises at least one insulating material such as SiO_2, Si_3N_4, HfO_2, or Al_2O_3 e.g. deposited by e-beam evaporation, CVD, PE-CVD, sputtering, or ALD. The mask can therefore be provided on the substrate surface by any convenient technique such as by electron beam deposition, CVD, plasma enhanced-CVD, sputtering, and atomic layer deposition (ALD).

In order to prepare positioned Au catalysed nanowires on a substrate, a thin film of Au, such as with a thickness less than 50 nm, can be deposited after etching the hole patterns in the mask. The deposition can be made with a photo or e-beam resist remaining on top of the mask after each hole etch. By removing the photo or e-beam resist in a so called "lift-off" process, a regular arrayed pattern of Au dots on the substrate surface can be fabricated. Optionally the mask may be partially or completely removed after fabrication.

In particular, the simple use of vapour-solid growth may enable nanowire growth. Thus, in the context of MBE, simple application of the reactants, e.g. In and As, to the substrate without any catalyst can result in the formation of a nanowire. This forms a further aspect of the invention which therefore provides the direct growth of a semiconductor nanowire formed from the elements described above on a graphitic substrate. The term direct implies therefore the absence of a film of catalyst to enable growth.

As noted above, the nanowires of the invention preferably grow as cubic (zinc blende) or hexagonal (wurtzite) structures. The inventors have found that it is possible to change the crystal structure of the growing nanowire by manipulating the amounts of the reactants fed to the substrate as discussed above. Higher feeds of Ga, for example, force a GaAs crystal into the cubic crystal structure. Lower feeds encourage a hexagonal structure. By manipulating reactant concentrations, the crystal structure within the nanowire can therefore be changed.

The introduction of different crystal structures enables differing electronic properties to be present in the nanowire. This may enable the formation of crystal phase quantum dots and allow other interesting electronic technologies to be developed.

It is also within the scope of the invention for the nature of the material forming the nanowire to be changed during the growing process. Thus, by changing the nature of the molecular beams, a portion of different structure would be introduced into a nanowire. An initial GaAs nanowire could be extended with an InAs nanowire section for example by changing from a Ga feed to an In feed. The GaAs/InAs nanowire could then be extended with a GaAs nanowire section by changing back to a Ga feed and so on. Again, by developing different structures with

differing electrical properties, the inventors offer nanowires with interesting and manipulable electronic properties which can be tailored by the manufacturer towards all manner of end applications.

Graphitic top contact

Once the nanowires have been grown on a substrate in the presence of a catalyst, it is envisaged that some of the nanowires will have a catalyst deposit on top of nanowire. Ideally, the majority of the nanowires will have such a deposit, preferably substantially all the nanowires will comprise this deposit.

The invention then involves placing a graphitic layer on top of the formed nanowires to make a top contact. It is preferred that the graphitic top contact layer is substantially parallel with the substrate layer. It will also be appreciated that the area of the graphitic layer does not need to be the same as the area of the substrate. It may be that a number of graphitic layers are required to form a top contact with a substrate with an array of nanowires.

The graphitic layers used can be the same as those described in detail above in connection with the substrate. The top contact is graphitic, more especially it is graphene. This graphene substrate should contain no more than 10 layers of graphene or its derivatives, preferably no more than 5 layers (which is called as a few-layered graphene). Especially preferably, it is a one-atom-thick planar sheet of graphene.

The crystalline or "flake" form of graphite consists of many graphene sheets stacked together (i.e. more than 10 sheets). It is preferred if the top contact is 20 nm in thickness or less. Even more preferably, the graphitic top contact may be 5 nm or less in thickness.

When graphene contacts directly to the semiconductor materials which are the key components of opto-electric devices, it usually forms a Schottky contact which hinders the electrical current flow by creating a barrier at the contact junction. Due to this problem, the research on graphene deposited on semiconductors has been mainly confined to the use of graphene/semiconductor Schottky junctions, e.g. the Schottky junction solar cell, up to now.

However, the inventors have realized that the growing of semiconductor nanowires can involve metal catalysis. In the VLS method, e.g. MBE or MOVPE, the metal catalysts such as Au, Ga, or In are preferably used as seeds for nanowire growth and they remain as a form of nanoparticles on top of nanowires after completion of the nanowire growth. These catalyst deposits can be used as an intermediate material between metallic graphene and semiconductor nanowires. By taking advantage of the remaining catalytic material, the Schottky contact formed at the interface between metallic graphitic top contact and the semiconductor nanowire can be avoided and ohmic contact can be established.

Application of the top contact to the formed nanowires can be achieved by any convenient method. Methods akin to those mentioned previously for transferring graphitic layers to substrate carriers may be used. The graphitic layers from Kish graphite, highly ordered pyrolytic graphite (HOPG), or CVD may be exfoliated by mechanical or chemical methods. Then they can be transferred into etching solutions such as HF or acid solutions to remove Cu (Ni, Pt, etc.) (especially for CVD grown graphitic layers) and any contaminants from the exfoliation process. The etching solution can be further exchanged into other solutions such as deionised water to clean the graphitic layers. The graphitic layers can then be easily transferred onto the formed nanowires as the top contact. Again e-beam resist or photoresist may be used to support the thin graphitic layers during the exfoliation and transfer processes, which can be removed easily after deposition.

It is preferred if the graphitic layers are dried completely after etching and rinsing, before they are transferred to the top of the nanowire arrays. To enhance the contact between graphitic layers and nanowires a mild pressure and heat can be applied during this "dry" transfer.

Alternatively, the graphitic layers can be transferred on top of the nanowire arrays, together with a solution (e.g. deionised water). As the solution dries off, the graphitic layers naturally form a close contact to underlying nanowires. In this "wet" transfer method, the surface tension of the solution during the drying process might bend or knock out the nanowire arrays. To prevent this, where this wet method is used, more robust nanowires are preferably employed. Nanowires having a diameter of > 80 nm might be suitable. Alternatively, hole patterned substrates

which support the vertical nanowire structure could be used. One may also use the critical-point drying technique to avoid any damage caused by surface tension during the drying process.

If there is a water droplet on a nanowire array and attempts to remove it involve, for example a nitrogen blow, the water drop will become smaller by evaporation, but the drop will always try to keep a spherical form due to surface tension. This could damage or disrupt the nanostructures around or inside the water droplet.

Critical point drying circumvents this problem. By increasing temperature and pressure, the phase boundary between liquid and gas can be removed and the water can be removed easily.

The top contact graphitic layer is preferably transparent, conductive and flexible. To enhance the electrical and mechanical contact of the graphitic layers to the metal particles on top of as-grown nanowires further, a post-annealing process may be used. After the deposition of the graphitic top contact, the sample can be annealed in an inert atmosphere, e.g. of argon, or vacuum. Temperatures can be up to 600°C. Annealing times can be up to 10 min.

Also doping of the graphitic top contact can be utilized. The major carrier of the graphitic top contact can be controlled as either holes or electrons by doping. It is preferable to have the same doping type in the graphitic top contact and in the semiconducting nanowires, especially at the region below the metal catalytic particles, which would give a better ohmic behaviour after the post-annealing process. For example, for a core-shell nanowire with p-doping in the shell, p-doping of the top graphitic layers matches the carrier type across the metal particles at the top of the nanowire shell.

It will be appreciated therefore that both top graphitic layer and the substrate can be doped. In some embodiments, the substrate and/or the graphitic layer is doped by a chemical method which involves with an adsorption of organic or inorganic molecules such as metal chlorides ($FeCl_3$, $AuCl_3$ or $GaCl_3$), NO_2, HNO_3, aromatic molecules or chemical solutions such as ammonia.

The surface of substrate and/or the graphitic layer could also be doped by a substitutional doping method during its growth with incorporation of dopants such as B, N, S, or Si.

The nanowires of the invention may be coated by known methods, e.g. with radial epitaxial shells. For example, a mix of intrinsic and extrinsic semiconductors can be formed by coating an intrinsic or extrinsic core nanowire with a shell of the other type of semiconductor. A more complex nanowire can also be formed from a mix of extrinsic and intrinsic conductors. An insulating intrinsic layer can be placed between p and n doped extrinsic layers for instance. A p-doped core can therefore be covered by an intrinsic semiconductor shell with an n-doped extrinsic conductor shell on the outside (or vice versa). This has particular application in light-emitting diode and solar cell technology.

Shell coating can be effected by MBE or other epitaxial technique (e.g. MOVPE) using appropriate growth parameters that will be known/clear to the skilled man.

Applications

Semiconductor nanowires with a top-contact using graphitic layers of the invention may have wide ranging utility. They are semi-conductors so can be expected to offer applications in any field where semiconductor technology is useful. They are primarily of use in integrated nanoelectronics and nano-optoelectronic applications.

An ideal device for their deployment might be a solar cell in particular. One possible device is a nanowire solar cell sandwiched between two graphene layers as the two terminals.

Such a solar cell has the potential to be efficient, cheap and flexible at the same time. This is a rapidly developing field and further applications on these valuable materials will be found in the next years. The same concept can be used to also fabricate other opto-electronic devices such as light-emitting diodes (LEDs), waveguides and lasers.

The invention will now be further discussed in relation to the following non limiting examples and figures.

Brief Description of the Figures

Figure 1a-d shows the atomic arrangements when atoms are placed on 1) H- and B- sites (Figure 1a, b, and d), and 2) H- or B-sites (Figure 1c). In Figure 1e the bandgap energies of the III-V semiconductors (as well as Si and ZnO) are plotted against their lattice constants. Vertical solid (dashed) coloured lines depict the lattice constant of an ideal crystal that would give perfect lattice match with graphene for a cubic (hexagonal) crystal with the four different atomic arrangements (Figure 1a-d) with respect to graphene. The plot visualizes the vast possibilities for epitaxial growth of vertical semiconductor nanowires on graphitic substrates. In the case of some semiconductors, the lattice mismatch with graphene is very small (e.g. InAs, GaSb, and ZnO) for one suggested atomic configuration. For other semiconductors like GaAs, the lattice mismatch is quite large and in-between two different atomic configurations (as in Figure 1b or Figure 1c).

Figure 2 shows a MBE experimental set up.

Figure 3a is an idealised depiction of Ga (self) catalysed GaAs nanowires grown on graphite.

Figure 3b is a 45° tilted view SEM image of two vertical Ga assisted GaAs nanowires grown by MBE on a flake of Kish graphite. The spherical particles are Ga droplets.

Figure 3c is a cross sectional TEM image of the graphite/nanowire interface of a vertical Ga-assisted GaAs nanowire grown epitaxially on top of Kish graphite.

Figure 4 shows a depiction of a mask on the graphite surface, which has been etched with holes.

Figure 5a shows a schematic image of semiconducting nanowires grown by a metal catalyst-assisted vapour-liquid-solid (VLS) method. The substrate is graphene deposited on a SiO_2 substrate.

Figure 5b shows a schematic image as in Fig.5a but here with graphene as a top contact material. It can be also envisaged as a nanowire solar cell with the two graphene layers as the two terminals.

Figure 6a shows a tilted view SEM image of Ga- assisted GaAs nanowire arrays grown on a Si(111) substrate by MBE.

Figure 6b shows a SEM image of GaAs nanowire arrays covered with a graphene layer deposited on top. The nanowire arrays were grown as in Figure 6a.

Figure 6c shows a magnified SEM image of GaAs nanowire arrays covered with a graphene layer partially deposited on top. The nanowire arrays were grown as in Figure 6a.

Example 1

Experimental procedure for growing vertical nanowires on graphitic substrates:

Nanowires were grown in a Varian Gen II Modular molecular beam epitaxy (MBE) system equipped with a Ga dual filament cell, an In SUMO dual filament cell, and an As valved cracker cell, allowing to fix the proportion of dimers and tetramers. In the present study, the major species of arsenic were As_4. Growth of NWs is performed either on a Kish graphite flake or on a graphene film (1 to 7 monolayers thick) grown by a chemical vapor deposition (CVD) technique directly on a Ni or Pt film deposited on an oxidized silicon wafer. The samples were prepared using two different procedures. In the first procedure, the samples were cleaned by iso-propanol followed by a blow dry with nitrogen, and then In-bonded to the silicon wafer. In the second procedure, a ~ 30 nm thick SiO_2 layer was deposited in an electron-beam evaporator chamber on the samples prepared using the first procedure where after holes of ~ 100 nm in diameter were fabricated in the SiO_2 using electron-beam lithography and plasma etching.

The samples were then loaded into the MBE system for the nanowire growth. The substrate temperature was then increased to a temperature suitable for GaAs/InAs nanowire growth: i.e. 610°C/450°C, respectively. The Ga/In flux was first supplied to the surface during a time interval typically in the range 5 s to 10

minutes, dependent on Ga/In flux and desired droplet size, while the As shutter was closed, to initiate the formation of Ga/In droplets on the surface. GaAs/InAs nanowire growth was initiated by simultaneously opening the shutter of the Ga/In effusion cell and the shutter and valve of the As effusion cell. The temperature of the Ga/In effusion cell was preset to yield a nominal planar growth rate of 0.1 μm per hour. To form the GaAs nanowires, an As_4 flux of 1.1×10^{-6} Torr is used, whereas the As_4 flux is set to 4×10^{-6} Torr to form InAs nanowires.

Example 2

Experimental procedure for growing vertical GaAs nanowires on GaAs (111)B or Si(111) substrates:

For growing Au-catalyzed GaAs nanowires on GaAs (111)B substrates, the substrate surface was first deoxidized at 620°C and then a 60 nm thick GaAs film was grown under growth conditions producing an atomically flat surface in the MBE system. It was transferred to an electron-beam evaporator for thin Au film deposition. The sample was then loaded into the MBE system again for nanowire growth. As_4 was used as the major species for As source. Under an As_4 flux of 6×10^{-6} Torr, the substrate temperature was increased to 540°C for GaAs nanowire growth. At this stage, thin Au film turned into Au particles and alloyed with the Ga from the substrate forming Au-Ga liquid particles. GaAs nanowire growth was initiated by opening the shutter of the Ga effusion cell. The temperature of the Ga effusion cell was preset to yield a nominal planar GaAs growth rate of 0.7 MLs^{-1}. Growth of GaAs nanowires was always terminated by shutting down the Ga and As fluxes, and immediately ramping down the substrate to room temperature.

For the growth of Ga self-catalyzed GaAs nanowires on Si(111) substrates, the Si substrates were etched in HF (5%) for 10 sec to remove the native oxide, rinsed in deionized water for 1 min, dried by blowing N_2 gas, and then directly loaded inside the MBE chamber. The major As specie used was As_4. The substrates were ramped up to the growth temperature of 620 °C. The GaAs nanowire growth started by opening the Ga and As shutters simultaneously. The GaAs nanowire growth was initiated by simultaneously opening the shutter of the Ga effusion cell and the shutter and valve of the As effusion cell.

Example 3

Experimental procedure for transferring the graphitic layers on top of nanowire arrays:

Graphitic layers (< 5 layers) grown on Cu foils were used. Since graphitic layers are formed on both sides of Cu foil during CVD growth, the graphitic layers formed on one side were removed by oxygen plasma to expose the Cu for etching. This was then dipped in a dilute iron nitrate ($Fe(NO_3)_3$) solution (< 5 %) to etch Cu away completely. After etching overnight (> 8hrs), the graphitic layers were floated on the etching solution, which were exchanged into deionised water. After further rinsing with deionised water several times, the graphitic layers were transferred on the nanowire arrays with deionised water. Deionised water was dried naturally in a clean room without any N_2 blow.

Claims

1. A composition of matter comprising a plurality of nanowires on a substrate, said nanowires having been grown epitaxially on said substrate in the presence of a metal catalyst such that a catalyst deposit is located at the top of at least some of said nanowires,

wherein said nanowires comprise at least one group III-V compound or at least one group II-VI compound or comprises at least one non carbon group IV element; and

wherein a graphitic layer is in contact with at least some of the catalyst deposits on top of said nanowires.

2. A composition as claimed in claim 1 wherein said nanowire grows in the [111] or [0001] direction.

3. A composition as claimed in any preceding claim wherein the nanowire comprises a group III-V compound.

4. A composition as claimed in any preceding claim in which the nanowires comprise AlAs, ZnO, GaSb, GaP, GaN, GaAs, InP, InN, InGaAs, InAs, or AlGaAs, such as GaSb, GaP, GaAs, or InAs.

5. A composition as claimed in any preceding claim wherein the substrate comprises a III-V semiconductor, e.g. GaAs, Si or is graphitic, such as graphene, graphane or graphene oxide, preferably wherein said graphene, graphane or graphene oxide comprises 10 or fewer atomic layers.

6. A composition as claimed in any preceding claim wherein the graphitic substrate and/or the graphitic layer is a laminated substrate exfoliated from a Kish graphite, a highly ordered pyrolytic graphite (HOPG), CVD-grown graphene layers on metallic films or foils such as Ni, Cu, or Pt films.

7. A composition as claimed in any preceding claim wherein the graphitic substrate and/or the graphitic layer is flexible and transparent.

8. A composition as claimed in any preceding claim wherein the surface of substrate and/or the graphitic layer is modified with a plasma treatment with a gas of oxygen, hydrogen, NO_2, or their combinations.

9. A composition as claimed in any preceding claim wherein the surface of substrate and/or the graphitic layer is modified by doping, e.g. using a solution of $FeCl_3$, $AuCl_3$ or $GaCl_3$.

10. A composition as claimed in any preceding claim wherein said surface of substrate and/or the graphitic layer is doped by adsorption of organic or inorganic molecules such as metal-chlorides ($FeCl_3$, $AuCl_3$ or $GaCl_3$), NO_2, HNO_3, aromatic molecules or ammonia.

11. A composition as claimed in any preceding claim wherein said surface of substrate and/or the graphitic layer is doped by substitutional doping method during its growth with incorporation of dopants such as B, N, S, or Si.

12. A composition as claimed in any preceding claim wherein said nanowires are no more than 500 nm in diameter and has a length of up to 5 microns.

13. A composition as claimed in any preceding claim wherein said substrate comprises a plurality of nanowires wherein said nanowires are substantially parallel.

14. A composition as claimed in any preceding claim wherein said catalyst is Au, Ag or the nanowires are self catalysed.

15. A composition as claimed in any preceding claim wherein said graphitic layer is graphene.

16. A composition as claimed in any preceding claim wherein said graphitic layer is doped with the same doping ions as the nanowires.

17. A process for the preparation of a composition of matter as claimed in claims 1 to 16 comprising:

(I) providing group II-VI elements or group III-V elements or at least one non carbon group IV element to the surface of a substrate, preferably via a molecular beam;

(II) epitaxially growing a plurality of nanowires from the surface of the substrate in the presence of a metal catalyst such that a catalyst deposit remains on the top of at least some of said nanowires;

(III) contacting said metal catalyst deposits with a graphitic layer such that a graphitic layer is in contact with at least some of the catalyst deposits on top of said nanowires.

18. A process as claimed in claim 17 where the substrate is coated with a hole-patterned mask, preferably where said catalyst is introduced on to the substrate surface exposed via the hole pattern.

19. A process as claimed in claim 17 or 18 where the hole-patterned mask comprises at least one insulating material such as SiO_2 , Si_3N_4, HfO_2, or Al_2O_3 e.g. deposited by e-beam evaporation, CVD, PE-CVD, sputtering, or ALD.

20. A process as claimed in claim 17 to 19 where the surface of the substrate exposed through the hole pattern is modified with a plasma treatment with a gas of oxygen, hydrogen, NO_2, or their combinations.

21. A process as claimed in claim 17 to 20 wherein the graphitic layer is subjected to a post-annealing process.

22. A device comprising a composition as claimed in claims 1 to 16, e.g. an optical or electronic device, e.g. a solar cell.