CLAIMS

1. A method of processing a substrate, comprising:

providing a first polymer dielectric layer formed on a top surface of the substrate, wherein the entire first polymer dielectric layer is in direct contact with the top surface of the substrate;

forming a first redistribution layer (RDL) on the first polymer dielectric layer, the first RDL comprising a second polymer dielectric layer with a metal layer embedded in the second polymer dielectric layer and at least one first opening in a top surface of the second polymer dielectric layer to expose at least a portion of the metal layer, the metal layer formed on an uppermost top surface of the first polymer dielectric layer;

constructing a three-dimensional (3D) metal-insulator-metal (MIM) capacitive stack on the first RDL in the at least one first opening in the top surface of the second polymer dielectric layer, the 3D MIM capacitive stack having a top electrode, a bottom electrode, and a capacitive dielectric layer interposed between the top electrode and the bottom electrode, the bottom electrode directly beneath the 3D MIM capacitive stack is in direct physical contact with the metal layer;

depositing a dielectric layer on the 3D MIM capacitive stack and on the second polymer dielectric layer; and

forming a spacer by removing the dielectric layer from the 3D MIM capacitive stack and from the first RDL except for a portion that is in direct contact with a sidewall of the 3D MIM capacitive stack, wherein the spacer contacts sidewalls of the top electrode, the bottom electrode, and the capacitive dielectric layer.

2. The method of processing the substrate of claim 1, further comprising:

forming a second RDL without a polymer dielectric layer on the first RDL and the 3D MIM capacitive stack, the second RDL forming an electrical contact with at least a portion of the top electrode of the 3D MIM capacitive stack and forming a direct physical connection with the metal layer via at least one second opening in the top surface of the second polymer dielectric layer.

3. The method of processing the substrate of claim 1, wherein the dielectric layer includes silicon oxide (SiO_2) or silicon nitride (Si_3N_4).

4. The method of processing the substrate of claim 1, wherein the first and second polymer dielectric layers includes polyimide, polybenzoxazole, phenolic, or epoxy.

5. The method of processing the substrate of claim 1, wherein the metal layer is copper or aluminum.

6. The method of processing the substrate of claim 1, wherein the capacitive dielectric layer includes hafnium oxide (HfO_2), silicon nitride (Si_3N_4), silicon carbide (SiC), aluminum nitride (AlN), titanium oxide (TiO_2) or tantalum oxide (Ta_2O_5).

7. The method of processing the substrate of claim 1, further comprising:

depositing the dielectric layer to a thickness of approximately 5 nm to approximately 100 nm.

8. A method of processing a substrate, comprising:

providing a first polymer dielectric layer formed on a top surface of the substrate wherein the entire first polymer dielectric layer is in direct contact with the top surface of the substrate;

forming a first redistribution layer (RDL) on the first polymer dielectric layer, the first RDL comprising a second polymer dielectric layer with a metal layer embedded in the second polymer dielectric layer and at least one first opening in a top surface of the second polymer dielectric layer to expose at least a portion of the metal layer, the metal layer formed on an uppermost top surface of the first polymer dielectric layer;

constructing a three-dimensional (3D) metal-insulator-metal (MIM) capacitive stack on the first RDL in the at least one first opening in the top surface of the second polymer dielectric layer, the 3D MIM capacitive stack having a top electrode, a bottom electrode, and a capacitive dielectric layer interposed between the top electrode and the bottom electrode, the bottom electrode directly beneath the 3D MIM capacitive stack is in direct physical contact with the metal layer;

depositing a dielectric layer on the 3D MIM capacitive stack and on the second polymer dielectric layer;

removing a first portion of the dielectric layer to expose at least a portion of the top electrode at a bottom of at least one second opening in the 3D MIM capacitive stack and a second portion of the dielectric layer to expose at least a portion of the metal layer at a bottom of at least one third opening in the second polymer dielectric layer;

after removing the first portion and the second portion of the dielectric layer, a third portion of the dielectric layer above the second polymer dielectric layer is continuous with a fourth portion of the dielectric layer on a sidewall of the at least one third opening in the second polymer dielectric layer and a fifth portion of the dielectric layer on a sidewall of the 3D MIM capacitive stack; and

forming a second RDL on the dielectric layer and the 3D MIM capacitive stack, the second RDL forming an electrical contact with the portion of the top electrode at the bottom of the at least one second opening in the 3D MIM capacitive stack and forming an electrical contact with the metal layer at the bottom of the at least one third opening in the second polymer dielectric layer.

9. The method of processing the substrate of claim 8, further comprising:

forming the second RDL without a polymer dielectric layer on the dielectric layer and the 3D MIM capacitive stack.

10. The method of processing the substrate of claim 8, wherein the dielectric layer includes silicon oxide (SiO_2) or silicon nitride (Si_3N_4).

11. The method of processing the substrate of claim 8, wherein the first or the second polymer dielectric layer includes polyimide, polybenzoxazole, phenolic or epoxy.

12. The method of processing the substrate of claim 8, wherein the metal layer is copper or aluminum.

13. The method of processing the substrate of claim 8, wherein the capacitive dielectric layer includes hafnium oxide (HfO_2), silicon nitride (Si_3N_4), silicon carbide (SiC), aluminum nitride (AlN), titanium oxide (TiO_2) or tantalum oxide (Ta_2O_5).

14. The method of processing the substrate of claim 8, further comprising: depositing the dielectric layer to a thickness of approximately 5 nm to approximately 100 nm.

15. A substrate, comprising:

a first polymer dielectric layer;

a metal layer on an uppermost top surface of the first polymer dielectric layer;

a second polymer dielectric layer on the first polymer dielectric layer and the metal layer, wherein the second polymer dielectric layer comprises at least one first opening and at least one second opening etched to a top surface of the metal layer;

a three-dimensional (3D) metal-insulator-metal (MIM) capacitive stack formed on the second polymer dielectric layer with a bottom electrode of the 3D MIM capacitive stack making direct physical contact with the metal layer via the at least one first opening in the second polymer dielectric layer, the 3D MIM capacitive stack having a top electrode, a bottom electrode, and a capacitive dielectric layer interposed between the top electrode and the bottom electrode;

a conformal dielectric layer on the 3D MIM capacitive stack and the second polymer dielectric layer, the conformal dielectric layer having at least one third opening to the metal layer formed in the at least one second opening in the second polymer dielectric layer and at least one fourth opening to the top electrode of the 3D MIM capacitive stack formed in the at least one first opening in the second polymer dielectric layer, wherein the at least one third opening only exposes a bottom of the at least one second opening and the at least one fourth opening only exposes a portion of the top electrode at a bottom of the at least one first opening;

wherein a first portion of the conformal dielectric layer above the second polymer dielectric layer is continuous with a second portion of the conformal dielectric layer on a sidewall of the at least one second opening in the second polymer dielectric layer and a third portion of the conformal dielectric layer on a sidewall of the 3D MIM capacitive stack;

a first contact formed on the second polymer dielectric layer, the first contact making direct physical contact with the metal layer in the at least one second opening in the second polymer dielectric layer; and

a second contact formed on the 3D MIM capacitive stack, the second contact making direct physical contact with the top electrode of the 3D MIM capacitive stack.

16. The substrate of claim 15, wherein the conformal dielectric layer includes silicon oxide (SiO_2) or silicon nitride (Si_3N_4).

17. The substrate of claim 15, wherein the first and second polymer dielectric layers include polyimide, polybenzoxazole, phenolic or epoxy.

18. The substrate of claim 15, wherein the metal layer is copper or aluminum.

19. The substrate of claim 15, wherein the capacitive dielectric layer includes hafnium oxide (HfO_2), silicon nitride (Si_3N_4), silicon carbide (SiC), aluminum nitride (AlN), titanium oxide (TiO_2) or tantalum oxide (Ta_2O_5).

20. The substrate of claim 15, wherein the conformal dielectric layer is approximately 5 nm to approximately 100 nm in thickness.