

Description

The invention relates to a circuit arrangement for linearly amplifying and demodulating an AM-modulated audio signal. Such circuit arrangements are known and are frequently used, for example, in broadcasting receivers for amplifying and demodulating an intermediate-frequency AM-modulated audio signal.

It is important that the gain remains linear over a large dynamic range, that is to say, the amplifier should be prevented from performing its limiting action in the case of a large signal field strength. For this purpose it is conventional practice to use automatic gain control. In the case of larger signal field strengths the gain of a stage is reduced so that the subsequent stages are prevented from performing their limiting actions.

However, automatic gain control has its drawbacks. A plurality of circuit elements is required for deriving, postponing, amplifying and/or smoothing the required control voltage. Amplifier stages must be controllable for which concessions must be made to the noise and/or distortion properties of the amplifier stages. Moreover, an effect of the AVC is that the lowest frequencies of the modulation signals are partly suppressed, resulting in an undesirable attenuation of the demodulated signal at the low end of the frequency characteristic.

It is an object of the invention to provide a circuit arrangement for linearly amplifying and demodulating an AM-modulated audio signal in which at least a part of the above-mentioned drawbacks of automatic gain control is obviated and to this end the circuit arrangement according to the invention is characterized by

- a logarithmic amplifier of the type having an input for receiving the AM-modulated audio input signal, a plurality for limiting amplifier stages which successively perform their limiting actions in response to an increase of the input signal, for each said limiting amplifier stage a demodulation circuit having its input connected to an output of the corresponding limiting amplifier stage, an adder circuit for summing the output signals of the demodulation circuits and an output, which is the output of the adder circuit for supplying a demodulated logarithmically distorted output signal;
- an antilog circuit having an input connected to the output of the logarithmic amplifier for substantially compensating the logarithmic distortion of the output signal of the logarithmic amplifier and for supplying the demodulated AM signal;

- and a DC-separation coupled to the antilog circuit and arranged to prevent the DC-component of the output signal of the logarithmic amplifier from being applied to the input of the antilog circuit.

It is also an object of the invention to provide a semiconductor element for use in such a circuit arrangement.

The invention is based on the recognition that considerable advantages are obtained in applications in which a linear signal gain is required, if the AM-modulated audio signal is first amplified and demodulated by such a logarithmic amplifier, the resultant field strength-dependent DC component is blocked and the logarithmically distorted signal is subsequently linearized again by means of an antilog circuit.

Logarithmic amplifiers of the type described above are known per se from IEEE, Journal of Solid State Circuits, Vol. SC-15, No. 3, June 1980, pp. 291-295 or from German Auslegeschrift 2,606,270 or US patent 3,605,027. These logarithmic amplifiers are used for amplifying and demodulating AM-modulated signals having a large dynamic range in which compression of large signal amplitudes is desired as, for example, in IF radar uses or in radiation detectors. Due to the logarithmic compression, AVC can then be avoided.

It is also known (GB-A-1,600,117) to combine a logarithmic amplifier with an antilog circuit for non-linearly amplifying, for example, squaring of signals.

For a satisfactory logarithmic characteristic the gain of each of the amplifier stages should be comparatively small (for example, < 15 db). On the other hand the amplitude of the signal applied to the antilog circuit should have the correct value for an optimum compensation of the logarithmic distortion. To satisfy the two requirements, the circuit arrangement according to the invention may be characterized in that the logarithmic amplifier comprises cascaded amplifier stages having a first output for supplying signals with a given gain to a subsequent stage, and a second output for supplying signals with a higher gain to the relevant demodulation circuit.

The antilog circuit is realised in a simple manner by means for applying the demodulated, logarithmically distorted output signal of the logarithmic amplifier to the series arrangement of a capacitor and a pn junction of a semiconductor element, a current source connected to the common connection between the capacitor and the pn junction for supplying a bias current in the forward direction to the pn junction and means for deriving the demodulated AM signal from the current through the pn junction. A further economy of ele-

ments can be realized if the pn junction is constituted by the base-emitter junction of a transistor, if the capacitor and the current source are connected to the emitter electrode of the transistor and if the output for the demodulated AM signal is coupled to the collector electrode of the transistor.

It is to be noted that it is known per se to use in FM receivers a logarithmic amplifier of the type with a cascade of amplifier stages successively performing their limiting actions in response to an increase of the input signal and with stepwise demodulation for supplying an FM field strength-dependent control quantity which is then used, for example, for the FM field strength-dependent mono-stereo control of a stereo decoder circuit. The FM signal which is non-linearly amplified by the cascade of amplifier stages is then applied to an FM detector for demodulating the FM signal.

The use of the circuit arrangement according to the invention in an AM-FM receiver has the advantage that the limiting amplifier stages can be used both for amplifying the FM signals and for amplifying the AM signals and that the entire logarithmic amplifier may serve for both receptions, namely for the non-linear amplification and detection of the AM signals and possibly for generating a field strength-dependent control quantity in the case of AM reception on the one hand and for generating the field strength-dependent control quantity in the case of FM reception on the other hand.

In FM receivers for use in motor vehicles it is known to use a suppression circuit (IAC) for suppressing interference pulses in the demodulated FM signal. When using such a suppression circuit the circuit arrangement according to the invention may further be characterized by a connection for supplying suppression pulses from the output for supplying the demodulated AM signal to the suppression circuit.

All this means that a considerable simplification can be obtained with the invention as compared with circuits arrangements in which substantially entirely separated sections for FM reception and for AM reception are used. This also means that it is possible to provide an integrated semiconductor element in a simple and inexpensive manner, which element can find universal use in an AM receiver, in an FM receiver, in an AM-FM receiver and in a receiver for signals which are both AM and FM-modulated. Such a semiconductor element will then preferably comprise the integratable circuit elements of the logarithmic amplifier, the antilog circuit and the FM detector, as well as a common input for all signals to be amplified and demodulated, an output for the demodulated FM signal, an output for the demodulated AM signal and an output for the field strength-dependent

control quantity.

The invention will now be described in greater detail, by way of example, with reference to the accompanying drawings in which

- 5 Fig. 1 is a block diagram of a circuit arrangement according to the invention;
- Fig. 2 is a second block diagram of a circuit arrangement according to the invention;
- Fig. 3 shows a characteristic curve to explain the operation of the circuit arrangement of Fig. 2;
- 10 Fig. 4 is a detailed circuit diagram of a circuit arrangement according to the invention;
- Fig. 5 is a modification of the circuit diagram of Fig. 4 and
- 15 Fig. 6 is a block diagram of a circuit arrangement according to the invention for receiving and processing AM or FM-modulated radio signals.

20 The circuit diagram of Fig. 1 shows a cascade of five limiting amplifier stages A1 to A5, with the input of the amplifier stage A1 being coupled to an input terminal 4/5 and each input of the subsequent stages A2 to A5 being coupled to the output of the previous stage A1 to A4. Each output of the amplifier stages A1 to A5 is also coupled to an input of a demodulation circuit D1 to D5 and the outputs of the demodulation circuits are coupled to inputs of an adder circuit S in which the output signals of the amplifier stages demodulated by the demodulation circuits are summed. The output signal V_{log} of the adder circuit S is applied via a terminal 15 and a DC separation symbolically shown by means of a capacitor C to an antilog circuit AL having an input terminal 16 and an output terminal 20 for supplying the linear, demodulated signal V_o . An amplitude-modulated input signal V_i is applied to the input terminal 4/5, for example, an AM-modulated intermediate-frequency signal of 470 KHz in a radio receiver for AM-modulated signals. The amplitude of the input signal V_i may vary due to two causes, namely due to the signal modulation (approximately 20 db) on the one hand but considerably more on the other hand (for example, 50-60 db) due to field strength variations with which the signal received via an aerial and RF preliminary stage (not shown) is beset. The highest field strength variations may be reduced by an AGC control on the RF preliminary stage, but the input signal V_i is still substantially uncontrolled.

50 The amplitude variations of the input signal V_i ensure that alternately more or fewer stages of the amplifier stages A1 to A5 perform their limiting actions. In the case of small input signals all stages are non-limiting, but in response to an increase of the input signal firstly the amplifier stage A5, subsequently the amplifier stage A4 and so forth will perform their limiting actions. The output signals of

the amplifier stages are stepwise demodulated in the demodulation circuits D1 ... D5 and subsequently summed in the adder circuit S.

The known combination of limiting amplifier stages, demodulation circuits and adder circuits constitutes a logarithmic amplifier/detector LA whose output signal $V_{\log}$ is a more or less satisfactory approximation of the logarithm of the amplitude of the input signal. The logarithmic relation between $V_{\log}$ and the amplitude of V_i is better approximated as the gain per stage of the stages A1 - A5 is smaller and the number of these stages is larger. On the other hand the dynamic range of the logarithmic amplifier is substantially determined by the number of amplifier stages multiplied by the gain per stage. For example, 6 stages having a gain of 12 db each may be chosen for an AM intermediate-frequency amplifier, which yields a dynamic range of approximately 70 db. It will be evident that the number of five stages shown in Fig. 1 is only given by way of example. For a good logarithmic variation a bipolar transistor differential amplifier stage with directly coupled emitters (see Fig. 4) is preferably used in the stages.

The output signal $V_{\log}$ of the logarithmic amplifier comprises the logarithmically distorted modulation signal as well as a DC component which is dependent on the average field strength of the received input signal. This field strength-dependent DC component is blocked by the DC separation in such a way that only the logarithmically distorted modulation signal appears at the input of the antilog circuit AL. This signal is converted in the antilog circuit to the original undistorted modulation signal. Consequently, where in known amplifiers the field strength dependence of the input signal is suppressed to a certain extent by an automatic gain control at one or more amplifier stages, this field strength dependence is completely suppressed in the circuit arrangement shown by the combination of logarithmic amplifier/demodulator, DC separation and antilog circuit. Whereas the logarithmic amplifier must have a large dynamic range, for example, 20 db for the signal variations and 50 db for the field strength variations, hence a total of 70 db, the dynamic range of the antilog circuit need only be suitable for the signal variations (20 db).

The input signal of the antilog circuit should have the correct value for an optimum linearization of the signal. For example, if the logarithmically distorted signal is applied to one silicon pn junction, $V_{\log}$ should increase by approximately 17-20 millivolts per octave variation of the signal V_i . To achieve this optimum value it may occur that either the gain per amplifier stage A1 ... A5 should be larger, which detracts from the correct logarithmic variation of the amplifier LA, or an additional am-

plifier stage must be introduced in the output of the adder circuit. A simpler solution may be that each amplifier stage A1 ... A4 in the cascade has two signal outputs, one having a low gain for driving the next amplifier stage and one having a higher gain for driving the associated demodulation circuit.

This is elucidated in Fig. 2 in which the same reference numerals as in Fig. 1 have been used for corresponding elements and in which the gain of the output with respect to the input of the relevant amplifier stage is indicated at the various outputs of the amplifier stages A1 ... A5. The gain G of stages A1, A2, A3 and A4 to the input of the next stage may be equal to, for example, 4 (= 12 db) and the gain of the stages A2, A3, A4 and A5 to the respective demodulation circuit is equal to $K \times G$ in which $K > 1$. K may be equal to, for example, 2 so that $K \times G = 8$ (= 18 db).

The amplifier stage which is the last to perform its limiting action in response to an increase of the input signal (i.e. the amplifier stage A1) has a gain to its demodulation output which is approximately a factor of

$$\frac{G}{G-1}$$

larger than the gain to the demodulation outputs of the other amplifier stages, i.e. it holds for $G = 4$ that

$$\frac{G}{G-1} = \frac{4}{3} = 2.5 \text{ db}$$

so that the gain of the stage A1 to its demodulation output is approximately 20.5 db.

It has been found that this measure yields an improvement of the logarithmic characteristic of the logarithmic amplifier at the higher signal amplitudes. This is shown in greater detail in Fig. 3. This Figure shows the characteristic curve of the output signal $V_{\log}$ on a linear scale as a function of the amplitude of V_i on a logarithmic scale. The curve C1 is the characteristic curve for six amplifier stages with $G = 4$ and equal gains to the demodulation outputs; the curve C2 is the same characteristic curve with a 2.5 db higher gain to the demodulation output of the amplifier stage A1. Instead of the amplifier stage A1, the demodulation circuit D1 may also have the desired

$$\frac{G}{G-1}$$

higher gain, for example, by choosing the value of resistor R1 to be described with reference to Fig. 4 to be smaller than the values of the corresponding resistors R2 ... Rn.

In the embodiment of Fig. 4 the cascade-arranged amplifier stages are denoted by A1 to An and the demodulation circuits are denoted by D1 to Dn. The amplifier stage A1 comprises two transistors 1 and 2 whose emitter electrodes are directly connected together. A DC source 3 is incorporated between these emitter electrodes and ground. The base electrodes of the transistors 1 and 2 are connected to two input terminals 4 and 5 of the amplifier stage A1; they also constitute the input terminals of the logarithmic amplifier. A positive power supply terminal is coupled via two series-arranged resistors 6 and 7 to the collector electrode of transistor 1 and via two series-arranged resistors 8 and 9 to the collector electrode of transistor 2. The junction points of the resistors 6 and 7 and of the resistors 8 and 9 are connected to the input terminals of the subsequent amplifier stage A2 and the collector electrodes of the transistors 1 and 2 are connected to the input terminals of the demodulation circuit D1.

The transistors 1 and 2 and their collector resistors and the common current source 3 constitute a limiting amplifier having a tanh transfer function. The gain to the next amplifier stage is determined by the value of the current source 3 and of the collector resistors 6 and 8. The larger gain to the demodulation circuit D1 is determined by the value of the current source 3 and of the series arrangements of collector resistors 6/7 and 8/9.

The demodulation circuit D1 comprises two transistors 10 and 11 with interconnected emitter electrodes and with collector electrodes connected to the positive power supply terminal. The base electrode of transistor 10 is connected to the collector electrode of transistor 1 and the base electrode of transistor 11 is connected to the collector electrode of transistor 2. The transistors 10 and 11 constitute a full-wave rectifier for the output signal of the amplifier stage A1. The interconnected emitter electrodes of these transistors are coupled to the adder circuit S via a resistor R1.

The amplifier stages A2 to An and the demodulation circuits D2 to Dn are identical to the stage A1 and to the detection circuit D1, respectively, on the understanding that the resistors 7 and 9 of the stage A1 have higher values than those of the corresponding resistors of the other stages in order to achieve the gain of the first stage which is higher by a factor of

$$\frac{G}{G-1}$$

and that in the last stage An the resistors 6, 7 and 8, 9 may be combined to one collector resistor because there is no output required for a subse-

quent amplifier stage. As will be elucidated with reference to Fig. 6, it is advantageous to connect an FM detector FD having an output terminal 29 to the output of the last stage An.

The adder circuit S comprises a common node P to which the resistor R1 and corresponding resistors R2 ... Rn are connected, as well as a current source 12 which is connected thereto. The node P is connected to an output terminal 15 via an emitter follower circuit comprising transistor 13 and emitter resistor 14. The output terminal 15 supplies the logarithmic voltage $V_{\log}$ and thus serves as the output of the logarithmic amplifier.

The output terminal 15 of the logarithmic amplifier is connected via a separating capacitor C to the input terminal 16 of the antilog circuit AL. It comprises a transistor 17 whose base electrode is connected to the input terminal 16 and whose emitter electrode is directly connected to ground. The collector electrode of the transistor 17 is connected to the positive power supply terminal via a collector resistor 18 and the base electrode is connected thereto via a current source 19. Finally, the collector electrode is connected to an output terminal 20 for supplying the linearized demodulated signal V_o . To decrease the collector impedance of the transistor 17, a common-base transistor, which constitutes a cascade with the transistor 17, can be arranged between the collector electrode of this transistor and the resistor 18.

To elucidate the operation of the separating capacitor C and the antilog circuit AL, it is assumed that the input signal at the terminals 4-5 can be represented by $A \cdot (1 + m \cdot \sin \mu t) \cdot \sin \omega t$ in which ω is the angular frequency of the AM-modulated carrier, $1 + m \cdot \sin \mu t$ is the sinusoidal AM modulation with angular frequency μ and modulation depth m , and A is the average carrier amplitude. This amplitude A changes due to field strength variations of the input signal.

Due to the demodulation and the logarithmic conversion of the logarithmic amplifier/demodulator, the signal $V_{\log}$ is proportional to $\ln\{A \cdot (1 + m \cdot \sin \mu t) \cdot \sin \omega t\} = \ln A + \ln(1 + m \cdot \sin \mu t)$.

The first term is the field strength-dependent DC component of $V_{\log}$ which is not transferred by the capacitor C. The voltage $\ln(1 + m \cdot \sin \mu t)$ is present across the base-emitter junction of the transistor 17 and the exponential voltage-current characteristic of this junction converts this voltage to a current $I \cdot (1 + m \cdot \sin \mu t)$ through collector resistor 18, in which I is the average collector current determined by the current source 19. Thus, the undistorted modulation is available at the output terminal 20.

It is to be noted that the term $\ln(1 + m \cdot \sin \mu t)$ actually comprises a modulation-dependent DC component which is of course blocked by the ca-

capacitor C and would thus lead to an incorrect linearization of the modulation signal. However, it can be shown that the current source 19, together with the exponential base-emitter junction of the transistor 17, regenerates the required DC component across this junction. The value of the direct current supplied by the source 19 also determines the amplitude of the output signal V_o .

If the modulation signal has a DC component of itself, as is the case with video signals, the current of the source 19 should be varied dependent on this DC component. This can be done by comparing a level of the video signal at the output terminal 20, which level should be constant, for example the peak sync level or the backporch level, with a reference level and by deriving a control voltage from the difference to control the current source 19 by means of this voltage.

As will be described with reference to Fig. 6, a control voltage V_{level} , which is field strength-dependent, is often required. This voltage can be derived from the voltage V_{log} at the terminal 15 via a low-pass filter 21 with which the AC component of V_{log} is obstructed. Such a control voltage may be obtained in a simpler manner by means of the antilog circuit of Fig. 5. In this case the voltage V_{log} is directly applied to the base electrode of the transistor 17 via the terminal 16; instead of the capacitor C of Fig. 4 a capacitor C' is now arranged between the emitter electrode of transistor 17 and ground and instead of the current source 19 the antilog circuit of Fig. 5 comprises a current source 19' arranged between the emitter electrode and ground. The circuit operates substantially analogously to that of Fig. 4 but in the circuit of Fig. 5 the voltage V_{level} may be directly taken off the capacitor C. Moreover, since both the logarithmic amplifier and the antilog circuit can be fully incorporated in one IC in a simple manner, except for the capacitors C and C', which should be connected externally, only one IC pin is required for the capacitor C' in Fig. 5, whereas two IC pins are required for the capacitor C in Fig. 4.

To reduce the temperature dependence of the circuit of Figs. 4/5, the current sources 3, 12 and 19 and 19' may be temperature-dependent, preferably in such a way that the current is proportional to the absolute temperature.

Fig. 6 shows a radio receiver for AM and FM-modulated signals. The receiver comprises an FM tuner 23 and an AM tuner 24 which can both be connected to an aerial 25. An AM/FM switch 26 supplies a power supply voltage to the FM tuner for FM reception and to the AM tuner for AM reception.

Both tuners 23 and 24 supply their FM and AM-modulated intermediate-frequency signals, respectively, to the input 4/5 of an IF circuit 27

which may have a form as described with reference to one or more of the previous Figures. The IF circuit 27 has an output 28 of the amplifier stage AN for supplying the FM intermediate-frequency signal limited and amplified by the amplifier stages A1 ... AN. An FM demodulator 29 for demodulating the IF signal during FM reception is coupled to the output 28. The demodulated FM signal is interference suppressed in an interference pulse suppression circuit (IAC) 30 which may have a form as described in US Patent 3,739,285 in the name of the Applicant and the interference-suppressed signal is decoded in a stereo decoder 31 which applies via two AM/FM switches 32 and 33 the left and right stereo signals, respectively, to LF amplifiers 34 and 35 and loudspeakers 36 and 37, respectively, connected thereto.

During AM reception the AM-modulated IF signal is applied to the input 4/5 of the IF circuit 27. As described, the output 20 supplies the linearly amplified and demodulated AM signal V_o . This signal is freed from unwanted high-frequency components in a low-pass filter 38 and the LF signal thus filtered is applied via the AM/FM switches 32 and 33 to the LF amplifiers 34 and 35.

The V_o output of the IF circuit 27 not only serves for supplying the demodulated signal during AM reception, but it is also used for FM reception. In fact, this output supplies pulses during FM reception which are produced by pulse interferences in the FM signal and these pulses are applied to the suppression circuit 30 so as to block the signal supply from the FM detector to the stereo decoder for a short period. As described in US Patent 3,739,285, the blocking pulses may be derived alternatively from the FM-IF signal instead of from the demodulated FM signal.

The field strength-dependent DC voltage V_{level} present at the output 22 of the IF circuit can also be used for FM and AM reception. To this end V_{level} is applied to the stereo decoder 31 for an abrupt or gradual transition from stereo to mono reproduction when the level of the received FM signal becomes too weak for a satisfactory stereo reproduction. V_{level} is also applied as an AVC voltage to the AM tuner 24 in order to reduce the RF gain of the AM tuner when receiving extremely strong AM signals.

With the exception of several circuit elements in the FM detector, all elements of the sections surrounded by a broken line in Figs. 4 and 5 may be combined in one integrated semiconductor element in which the terminals 4, 5, 15, 16, 29 (Fig. 4) and 4, 5, 20, 22, 29 (Fig. 5) may be IC pins. This provides a very universal IC which can be used in AM receivers, FM receivers, AM/FM receivers and in receivers for signals which are both AM and FM-modulated.

It is to be noted that not all amplifier stages A1 ... An of the logarithmic amplifier should be arranged in cascade. In this connection reference is made to the Applicant's Patent Application EP-A-0 331 246 of the same priority date.

Claims

1. A circuit arrangement for linearly amplifying and demodulating an AM-modulated audio signal, characterized by
 - a logarithmic amplifier (LA) of the type having an input (4/5) for receiving the AM-modulated audio input signal, a plurality for limiting amplifier stages (A1..A5) which successively perform their limiting actions in response to an increase of the input signal, for each said limiting amplifier stage a demodulation circuit (D1..D5) having its input connected to an output of the corresponding limiting amplifier stage, an adder circuit (S) for summing the output signals of the demodulation circuits and an output (15), which is the output of the adder circuit, for supplying a demodulated logarithmically distorted output signal (V_{log});
 - an antilog circuit (AL) having an input (16) connected to the output (15) of the logarithmic amplifier for substantially compensating the logarithmic distortion of the output signal of the logarithmic amplifier and for supplying the demodulated AM signal;
 - and a DC-separation (C, C') coupled to the antilog circuit and arranged to prevent the DC-component of the output signal of the logarithmic amplifier from being applied to the input of the antilog circuit.
2. A circuit arrangement as claimed in Claim 1, characterized in that the logarithmic amplifier comprises cascaded amplifier stages having a first output for supplying signals with a given gain (G) to a subsequent stage, and a second output for supplying signals with a higher gain (KG) to the relevant demodulation circuit.
3. A circuit arrangement as claimed in Claim 1, characterized by means for applying the demodulated, logarithmically distorted output signal (V_{log}) of the logarithmic amplifier to the series arrangement of a capacitor (C, C') and a pn junction of a semiconductor element (17), a current source (19, 19') connected to the common connection between the capacitor and the

pn junction for supplying a bias current in the forward direction to the pn junction and means (18) for deriving the demodulated AM signal from the current through the pn junction.

4. A circuit arrangement as claimed in Claim 3, characterized in that the pn junction is constituted by the base-emitter junction of a transistor (17), in that the capacitor (C') and the current source (19') are connected to the emitter electrode of the transistor and in that the output (20) for the demodulated AM signal is coupled to the collector electrode of the transistor.
5. A circuit arrangement as claimed in Claim 3 or 4, characterized in that the output signal (V_{log}) of the logarithmic amplifier (LA) varies approximately 17-20 mV per octave of the input signal (V_i) of the logarithmic amplifier.
6. A circuit arrangement as claimed in any one of the preceding Claims, characterized by means (23) for applying an FM-modulated signal to the input (4/5) for supplying the AM-modulated signal, an FM detector (FD) connected to an output of one of the amplifier stages (AN) of the logarithmic amplifier and a low-frequency circuit (32-37) for processing the demodulated AM signal supplied by the antilog circuit and the demodulated FM signal supplied by the FM detector.
7. A circuit arrangement as claimed in Claim 6, characterized by means for deriving a field strength-dependent control quantity (V_{lev}) from the output signal of the logarithmic amplifier and means for supplying the field strength-dependent control quantity to an arrangement (31) having an FM signal field strength-dependent function and to an arrangement (24) having an AM signal field strength-dependent function.
8. A circuit arrangement as claimed in Claim 6, comprising a suppression circuit (30) for suppressing interference pulses in the demodulated FM signal, characterized by a connection for supplying suppression pulses from the output (20) for supplying the demodulated AM signal (V_o) to the suppression circuit.
9. An integrated semiconductor element for use in a circuit arrangement as claimed in any one of the preceding Claims, comprising integrable circuit elements of a logarithmic amplifier (LA) of the type having a number of amplifier stages successively performing their limiting



It is to be noted that not all amplifier stages A1 ... An of the logarithmic amplifier should be arranged in cascade. In this connection reference is made to the Applicant's Patent Application EP-A-0 331 246 of the same priority date.

Claims

1. A circuit arrangement for linearly amplifying and demodulating an AM-modulated audio signal, characterized by
 - a logarithmic amplifier (LA) of the type having an input (4/5) for receiving the AM-modulated audio input signal, a plurality for limiting amplifier stages (A1..A5) which successively perform their limiting actions in response to an increase of the input signal, for each said limiting amplifier stage a demodulation circuit (D1..D5) having its input connected to an output of the corresponding limiting amplifier stage, an adder circuit (S) for summing the output signals of the demodulation circuits and an output (15), which is the output of the adder circuit, for supplying a demodulated logarithmically distorted output signal (V_{log});
 - an antilog circuit (AL) having an input (16) connected to the output (15) of the logarithmic amplifier for substantially compensating the logarithmic distortion of the output signal of the logarithmic amplifier and for supplying the demodulated AM signal;
 - and a DC-separation (C, C') coupled to the antilog circuit and arranged to prevent the DC-component of the output signal of the logarithmic amplifier from being applied to the input of the antilog circuit.
2. A circuit arrangement as claimed in Claim 1, characterized in that the logarithmic amplifier comprises cascaded amplifier stages having a first output for supplying signals with a given gain (G) to a subsequent stage, and a second output for supplying signals with a higher gain (KG) to the relevant demodulation circuit.
3. A circuit arrangement as claimed in Claim 1, characterized by means for applying the demodulated, logarithmically distorted output signal (V_{log}) of the logarithmic amplifier to the series arrangement of a capacitor (C, C') and a pn junction of a semiconductor element (17), a current source (19, 19') connected to the common connection between the capacitor and the pn junction for supplying a bias current in the forward direction to the pn junction and means (18) for deriving the demodulated AM signal from the current through the pn junction.
4. A circuit arrangement as claimed in Claim 3, characterized in that the pn junction is constituted by the base-emitter junction of a transistor (17), in that the capacitor (C') and the current source (19') are connected to the emitter electrode of the transistor and in that the output (20) for the demodulated AM signal is coupled to the collector electrode of the transistor.
5. A circuit arrangement as claimed in Claim 3 or 4, characterized in that the output signal (V_{log}) of the logarithmic amplifier (LA) varies approximately 17-20 mV per octave of the input signal (V_i) of the logarithmic amplifier.
6. A circuit arrangement as claimed in any one of the preceding Claims, characterized by means (23) for applying an FM-modulated signal to the input (4/5) for supplying the AM-modulated signal, an FM detector (FD) connected to an output of one of the amplifier stages (AN) of the logarithmic amplifier and a low-frequency circuit (32-37) for processing the demodulated AM signal supplied by the antilog circuit and the demodulated FM signal supplied by the FM detector.
7. A circuit arrangement as claimed in Claim 6, characterized by means for deriving a field strength-dependent control quantity (V_{lev}) from the output signal of the logarithmic amplifier and means for supplying the field strength-dependent control quantity to an arrangement (31) having an FM signal field strength-dependent function and to an arrangement (24) having an AM signal field strength-dependent function.
8. A circuit arrangement as claimed in Claim 6, comprising a suppression circuit (30) for suppressing interference pulses in the demodulated FM signal, characterized by a connection for supplying suppression pulses from the output (20) for supplying the demodulated AM signal (V_a) to the suppression circuit.
9. An integrated semiconductor element for use in a circuit arrangement as claimed in any one of the preceding Claims, comprising integrable circuit elements of a logarithmic amplifier (LA) of the type having a number of amplifier stages successively performing their limiting



actions in response to an increase of the input signal, a demodulation circuit for each stage and an adder circuit which is common for all stages, and an antilog circuit (AL), as well as an input pin (4/5) coupled to the an input of the logarithmic amplifier for supplying the signals to be demodulated, and an output pin (20) coupled to an output of the antilog circuit for supplying AM-demodulated signals.

10. An integrated semiconductor element as claimed in Claim 9, further comprising integrable circuit elements of an FM detector (FD) and an output pin (29) coupled to a output of the FM detector for supplying FM-demodulated signals.

11. An integrated semiconductor element as claimed in Claim 9 or 10, further comprising an output pin (22) coupled to an output of the logarithmic amplifier for supplying a field strength-dependent control quantity (V_{lev}).

Patentansprüche

1. Schaltungsanordnung zum linearen Verstärken und Demodulieren eines AM-modulierten Tonsignals, dadurch gekennzeichnet, daß sie die nachfolgenden Elemente aufweist:

- einen logarithmischen Verstärker (LA) von dem Typ mit einem Eingang (4/5) zum Empfangen des AM-modulierten Ton-Eingangssignals, mit einer Anzahl begrenzender Verstärkerstufen (A1...A5), die bei zunehmendem Eingangssignal nacheinander ihre begrenzende Wirkung durchführen, mit einer Demodulationsschaltung (D1...D5) für jede genannte Begrenzungsverstärkerstufe, wobei der Eingang der Demodulationsschaltung mit einem Ausgang der entsprechenden Begrenzungsverstärkerstufe verbunden ist, mit einer Addierschaltung (S) zum Summieren der Ausgangssignale der Demodulationsschaltungen und mit einem Ausgang (15), der der Ausgang der Addierschaltung ist, zum Liefern eines demodulierten logarithmisch verformten Ausgangssignals (V_{log});
- eine Antilogschaltung (AL), von der ein Eingang (16) mit dem Ausgang (15) des logarithmischen Verstärkers verbunden ist, zum im wesentlichen Ausgleichen der logarithmischen Verformung des Ausgangssignals des logarithmischen Verstärkers und zum Liefern des demodulierten AM-Signals;

- und eine mit der Antilogschaltung gekoppelte Gleichstrom-Trennstufe (C, C') zur Vermeidung davon, daß der Gleichstromanteil des Ausgangssignals des logarithmischen Verstärkers dem Eingang der Antilogschaltung zugeführt wird.

2. Schaltungsanordnung nach Anspruch 1, dadurch gekennzeichnet, daß der logarithmische Verstärker kaskadengeschaltete Verstärkerstufen aufweist mit einem ersten Ausgang zum mit einer bestimmten Verstärkung (G) Liefern von Signalen zu einer nachfolgenden Stufe und mit einem zweiten Ausgang zum mit einer größeren Verstärkung (KG) Liefern von Signalen zu der betreffenden Demodulationsschaltung.

3. Schaltungsanordnung nach Anspruch 1, gekennzeichnet durch Mittel zum Zuführen des demodulierten logarithmisch verformten Ausgangssignals (V_{log}) des logarithmischen Verstärkers zu der Reihenschaltung aus einem Kondensator (C, C') und einem PN-Übergang eines Halbleiterelementes (17), durch eine an den Knotenpunkt des Kondensators und des PN-Übergangs angeschlossene Stromquelle (19, 19') zum Liefern eines Vorstroms in der Vorwärtsrichtung zu dem PN-Übergang und durch Mittel (18) zum Ableiten des demodulierten AM-Signals aus dem Strom durch den PN-Übergang.

4. Schaltungsanordnung nach Anspruch 3, dadurch gekennzeichnet, daß der PN-Übergang durch den Basis-Emitter-Übergang eines Transistors (17) gebildet wird, daß der Kondensator (C') und die Stromquelle (19') an die Emittierelektrode des Transistors angeschlossen sind und daß der Ausgang (20) für das demodulierte AM-Signal mit der Kollektorelektrode des Transistors gekoppelt ist.

5. Schaltungsanordnung N3 oder 4, dadurch gekennzeichnet, daß das Ausgangssignal (V_{log}) des logarithmischen Verstärkers (LA) etwa 17-20 mV je Oktave des Eingangssignals (V_i) des logarithmischen Verstärkers schwankt.

6. Schaltungsanordnung nach einem der vorstehenden Ansprüche, gekennzeichnet durch Mittel (23) zum Zuführen eines FM-modulierten Signals zu dem Eingang (4/5) zum Liefern des AM-modulierten Signals, durch einen FM-Detektor (FD), der mit einem Ausgang einer der Verstärkerstufen (AN) des logarithmischen Verstärkers verbunden ist, sowie



durch eine NF-Schaltung (32-37) zum Verarbeiten des von der Antilogschaltung gelieferten demodulierten AM-Signals und des von dem FM-Detektor gelieferten demodulierten FM-Signals.

7. Schaltungsanordnung nach Anspruch 6, gekennzeichnet durch Mittel zum Ableiten einer feldstärkeabhängigen Regelgröße (V_{lev}) aus dem Ausgangssignal des logarithmischen Verstärkers und durch Mittel zum Liefern der feldstärkeabhängigen Regelgröße zu einer Anordnung (31) mit einer FM-signalfeldstärkeabhängigen Funktion und zu einer Anordnung mit einer AM-signalfeldstärkeabhängigen Funktion. 10
8. Schaltungsanordnung nach Anspruch 6 mit einer Austastschaltung (30) zum Aystasten von Störimpulsen in dem demodulierten FM-Signal, gekennzeichnet durch eine Verbindung zum Liefern von Austastimpulsen von dem Ausgang (20) zum Liefern des demodulierten AM-Signals (V_o) zu der Austastschaltung. 20
9. Integriertes Halbleiterelement zum Gebrauch in einer Schaltungsanordnung nach einem der vorstehenden Ansprüche, mit integrierbaren Schaltungselementen eines logarithmischen Verstärkers (LA) vom Typ mit einer Anzahl bei zunehmendem Eingangssignal nacheinander in ihren Begrenzungszustand geratender Verstärkerstufen, mit einer Demodulationsschaltung je Stufe und mit einer allen Stufen gemeinsamen Addierschaltung, und mit einer Antilogschaltung (AL), sowie mit einem Eingangsstift (4/5) der mit einem Eingang des logarithmischen Verstärkers gekoppelt ist zum Liefern der zu demodulierenden Signale, und mit einem Ausgangsstift (20), der mit einem Ausgang der Antilogschaltung gekoppelt ist zum Liefern von AM-demodulierten Signalen. 30
10. Integriertes Halbleiterelement nach Anspruch 9, weiterhin mit integrierbaren Schaltungselementen eines FM-Detektors (FD) und mit einem Ausgangsstift (29), der mit einem Ausgang des FM-Detektors gekoppelt ist zum Liefern von FM-demodulierten Signalen. 35
11. Integriertes Halbleiterelement nach Anspruch 9 oder 10, weiterhin mit einem Ausgangsstift (22), der mit einem Ausgang des logarithmischen Verstärkers gekoppelt ist zum Liefern einer feldstärkeabhängigen Regelgröße (V_{lev}). 40

Revendications

1. Montage de circuit destiné à amplifier linéairement et démoduler un signal audio à modulation AM, caractérisé par
 - un amplificateur logarithmique (LA) comportant une entrée (4, 5) destinée à recevoir le signal d'entrée audio à modulation AM, une pluralité d'étages amplificateurs limiteurs (A1, ..., A5) qui exécutent successivement leurs actions limitatrices en réaction à une augmentation du signal d'entrée, pour chaque étage amplificateur limiteur un circuit de démodulation (D1, ..., D5) dont l'entrée est connectée à une sortie de l'étage amplificateur limiteur correspondant, un circuit additionneur (S) pour sommer les signaux de sortie des circuits de démodulation et une sortie (15), qui est la sortie du circuit additionneur, pour fournir un signal de sortie démodulé logarithmiquement déformé (V_{log});
 - un circuit antilog (AL) comportant une entrée (16) connectée à la sortie (15) de l'amplificateur logarithmique pour compenser en substance la distorsion logarithmique du signal de sortie de l'amplificateur logarithmique et pour fournir le signal AM démodulé,
 - et une séparation en continu (C, C') couplée au circuit antilog et disposée de manière à empêcher la composante continue du signal de sortie de l'amplificateur logarithmique d'être appliquée à l'entrée du circuit antilog.
2. Montage de circuit suivant la revendication 1, caractérisé en ce que l'amplificateur logarithmique comprend des étages amplificateurs en cascade comportant une première sortie destinée à fournir des signaux avec un gain donné (G) à un étage ultérieur et une seconde sortie destinée à fournir des signaux avec un gain supérieur (KG) au circuit de démodulation en question.
3. Montage de circuit suivant la revendication 1, caractérisé par des moyens pour appliquer le signal de sortie démodulé logarithmiquement déformé (V_{log}) de l'amplificateur logarithmique au montage en série d'un condensateur (C, C') et d'une jonction PN d'un élément semi-conducteur (17), une source de courant (19, 19') connectée à la connexion commune entre le condensateur et la jonction PN pour fournir un courant de polarisation en sens direct à la jonction PN et des moyens (18) pour dériver le



- signal (AM) démodulé du courant passant par la jonction PN.
4. Montage de circuit suivant la revendication 3, caractérisé en ce que la jonction PN est constituée par la jonction base/émetteur d'un transistor (17), le condensateur (C') et la source de courant (19') sont connectés à l'électrode d'émetteur du transistor et la sortie (20) pour le signal (AM) démodulé est couplée à l'électrode de collecteur du transistor.
 5. Montage de circuit suivant la revendication 3 ou 4, caractérisé en ce que le signal de sortie (V_{log}) de l'amplificateur logarithmique (LA) varie approximativement de 17 à 20 mV par octave du signal d'entrée (V_i) de l'amplificateur logarithmique.
 6. Montage de circuit suivant l'une quelconque des revendications précédentes, caractérisé par des moyens (23) pour appliquer le signal à modulation FM à l'entrée (4/5) pour fournir le signal à modulation (AM), un détecteur FM (FD) connecté à une sortie d'un des étages amplificateurs (AN) de l'amplificateur logarithmique et un circuit à basse fréquence (32-37) pour traiter le signal AM démodulé fourni par le circuit antilog et le signal FM démodulé fourni par le détecteur FM.
 7. Montage de circuit suivant la revendication 6, caractérisé par des moyens destinés à dériver une quantité de commande dépendant de l'intensité du champ (V_{lev}) du signal de sortie de l'amplificateur logarithmique et des moyens pour fournir la quantité de commande dépendant de l'intensité du champ à un dispositif (31) présentant une fonction dépendant de l'intensité du champ du signal FM et à un dispositif (24) comportant une jonction dépendant de l'intensité du champ du signal AM.
 8. Montage de circuit suivant la revendication 6, comprenant un circuit de suppression (30) pour supprimer des impulsions d'interférences dans le signal FM démodulé, caractérisé par une connexion destinée à fournir des impulsions de suppression de la sortie (20) destinée à fournir le signal AM démodulé (V_o) au circuit de suppression.
 9. Élément semi-conducteur intégré à utiliser dans un montage de circuit suivant l'une quelconque des revendications précédentes, comprenant des éléments de circuit intégrables d'un amplificateur logarithmique (LA) du type comportant un certain nombre d'étages amplificateurs exécutant successivement leurs actions limitatrices en réponse à une augmentation du signal d'entrée, un circuit de démodulation pour chaque étage et un circuit additionneur qui est commun pour tous les étages, et un circuit antilog (AL) ainsi qu'une broche d'entrée (4/5) couplée à l'entrée ou à une entrée de l'amplificateur logarithmique afin de fournir les signaux à démoduler, et une broche de sortie (20) couplée à une sortie du circuit antilog afin de fournir des signaux démodulés AM.
 10. Élément semi-conducteur intégré suivant la revendication 9, comprenant, en outre, des éléments de circuit intégrables d'un détecteur FM (FD) et une broche de sortie (29) couplée à une sortie du détecteur FM pour fournir des signaux démodulés FM.
 11. Élément semi-conducteur intégré suivant la revendication 9 ou 10, comprenant, en outre, une broche de sortie (22) couplée à une sortie de l'amplificateur logarithmique afin de fournir une quantité de commande dépendant de l'intensité du champ (V_{lev}).