A SEMICONDUCTOR MEMORY DEVICE AND A METHOD OF MANUFACTURE THEREOF

The present invention relates to a semiconductor memory device and in particular to a dynamic random access memory (DRAM), and a method of manufacture thereof.

The DRAM employs as a memory cell a series circuit which consists of a storage capacitor and a switching transistor (MISFET). In order to increase the quantity of information (the number of bits) and also to enhance the access time, the density of integration of the DRAM has to be increased. The most effective way to increase the integration density of the DRAM is to reduce the occupying area of the storage capacitor. However, any reduction in the area, results in a decrease in the capacitance of the capacitor. This leads to an increase in the soft errors ascribable to alpha particles (α particles), and also to the shortening of a refresh cycle.

There have been proposed several ideas for reducing the occupying area of the storage capacitor without decreasing the capacitance. As one of them, a DRAM including new storage capacitors (termed "trench capacitors" or "corrugated capacitors") whose capacitances are formed, not only on the surface of a semiconductor substrate, but also inwardly of the semiconductor substrate, has been proposed in Japanese Patent

Application No. 53883/75. The new storage capacitors are formed as follows. Each moat (also termed "U-groove" or "trench") is formed in one major surface of a semiconductor substrate. An insulator film is formed on the exposed surface of the semiconductor substrate within the moat. Further, a capacitor electrode covering the insulator film is formed. The MIS type capacitor is constructed of the semiconductor substrate, the insulator film and the capacitor electrode within the moat.

We have studied the above manufactured DRAM but have found that there are a number of problems in increasing the integration density of the DRAM.

The first problem is the spread of a depletion layer. In the storage capacitor, the part which stores charges serving as information is the moat portion within the semiconductor substrate. In the case where the distance between the respectively adjacent storage capacitors is reduced still further in order to enhance the density of integration, respective depletion layers which stretch from the side walls of the moats forming the adjacent storage capacitors couple with each other. When a potential difference exists between the adjacent storage capacitors, the charges migrate from the capacitor of higher potential to the capacitor of

lower potential. That is, the charges leak between the adjacent capacitors. This leads to the inversion of the information, and in turn, to lowering in reliability. The problem has hampered the enhancement of the integration density of the DRAM.

The second problem is the increase in the influence of α particles. As compared with a conventional storage capacitor which is flat, the three-dimensional capacitor structure based on the moat can store a large amount of charges within the semiconductor substrate. At the same time, however, the structure is more influenced by minority carriers which develop due to α particles within the semiconductor substrate. That is, as the moat extending inwards from one major surface of the semiconductor substrate becomes deeper, the degree of influence by the minority carriers increases more conspicuously. It is difficult to attain a large amount of charges enough to neglect the influence of the minority carriers created by the α particles. The reason is that increasing the depth of the moat is limited. The problem has hampered the enhancement of the reliability of the DRAM.

The third problem is the difficulty of flattening. The widthwise dimension of the moat immediately after having been formed in the semiconductor substrate is at least approximately 1 μm with the technical

level of a product. Since the thickening the capacitor electrode forms a cause for the breaking of a word line, the moat cannot be entirely filled with the material of the capacitor electrode and that of the insulator film. In consequence, a depression arises in the upper part of the moat. Thus, the word lines and bit lines which are formed over the moats are liable to break as well as causing variations in the width or length of the wiring. These problems cause variations in the electrical characteristics of the DRAM articles and the occurrence of non-conforming articles.

It is an object of the present invention to provide a DRAM formed with storage capacitors in moats, which is suited to enhancement in the density of integration.

Another object of the present invention is to prevent the charge leakage phenomenon between adjacent storage capacitors in a DRAM which is formed with the storage capacitors in moats.

Another object of the present invention is to reduce the influence of minority carriers created by α particles, upon storage capacitors in a DRAM which is formed with the storage capacitors in moats.

Another object of the present invention is to prevent the leakage current between a storage

capacitor and a substrate, in order to prolong the time for which information can be retained.

It is yet another object of the present invention to prevent depressions over the moats to form storage capacitors therein, in a DRAM which is formed with the storage capacitors in the moats.

According to a first aspect of the present invention there is provided a semiconductor memory device including:

(a) a semiconductor substrate which has one major surface;

(b) memory cells each of which comprises a MISFET and a capacitor connected in series with said MISFET, said MISFET including a gate electrode and source or drain region, said capacitor including a first conductor layer, a first insulator film formed on said first conductor layer and a second conductor layer formed on said first insultaor layer, at least one of said conductor layers being made of at least a polycrystalline silicon layer, and said first conductor layer being connected to one of said source or drain region and being arranged independently for said each capacitor of said memory cell;

(c) moats which are formed on said major surface

side of said semiconductor substrate by partly removing said semiconductor substrate, which are provided in correspondence with said capacitors and each of which has its inside surface covered with a second insultor film;

(d) a first part of said capacitor being provided on a whole surface of said second insulator film in said moat, a second part thereof other than said first part being provided on a third insulator film formed on said semiconductor substrate except a part where said first conductor layer of said second part is connected to one of said source or drain regions, said second and third insulator films being integrally provided;

(e) word lines which extend in one direction over said semiconductor substrate, and each of which is connected with the gate electrodes of the MISFETs; and

(f) data lines which extend in a direction intersecting said word lines over said semiconductor substrate, and each of which is connected with the others of the source or drain regions of the MISFETs, said memory cells being provided in correspondence with respective intersection points between said word lines and said data lines.

According to a second aspect of the present invention there is provided amethod of manufacturing a semiconductor memory device, said semiconductor memory

device including memory cells each consisting of a MISFET and a capacitor and moats formed in correspondence with the capacitors, said capacitor consisting of a first conductor layer, a first insulator film formed on said first conductor layer and a second conductor layer formed on said first insulator film, at least one of said conductor layers being made of at least a polycrystalline layer, said method including the steps of:

(a) forming a mask for forming said moats, on one major surface of a semiconductor substrate;

(b) forming said moats on the major surface side of said semiconductor substrate by partly removing said semiconductor substrate by partly removing said semiconductor substrate by the use of said mask;

(c) covering an inside surface of said each moat with a second insulator film and covering at least a part of the major surface of said semiconductor substrate with a third insulator film, said second and third insulator films being integrally formed;

(d) forming said first conductor layer on said second insulator film within said moat, on said third insulator film and on said semiconductor substrate, said first conductor layer being formed independently for said each memory cell and being connected to said MISFET in its area contacting with said semiconductor substrate; and

(e) forming said first insulator film on at least said first conductor layer, and forming said second conductor layer on said first insulator layer.

According to a third aspect of the present invention there is provided a semiconductor memory device including:

(a) a semiconductor substrate which has one major surface;

(b) memory cells each of which comprises a MISFET and a capacitor connected in series with said MISFET, said MISFET including a gate electrode and source or drain region, said capacitor including a first conductor layer, a first insulator film formed on said first conductor layer and a second conductor layer formed on said first insulator layer, said first conductor layer being connected to one of said source or drain region and being arranged independently for said each capacitor of said memory cell;

(c) moats which are formed on said major surface side of said semiconductor substrate, the inside surfaces of which are covered with a second insulator film the respective capacitors each being formed wholly within a respective moat;

(d) word lines which extend in one direction over said semiconductor substrate, and each of which is

connected with the gate electrodes of the MISFETs; and

(e) data lines which extend in a direction intersecting said word lines over said semiconductor substrate, and each of which is connected with the others of the source or drain regions of the MISFETs, said memory cells being provided in correspondence with respective intersection points between said word lines and said data lines.

The present invention will now be described in greater detail by way of example with reference to the accompanying drawings, wherein:-

Figure 1 is an equivalent circuit diagram showing the essential portions of a first embodiment of a DRAM;

Figure 2A is a plan view showing the essential portions of a memory cell in order to explain the DRAM of the first embodiment;

Figure 2B is a sectional view taken along line X-X in Figure 2A;

Figure 3 is a plan view showing the essential portions of a memory array which is constructed of the memory cells as shown in Figures 2A and 2B;

Figures 4A to 12B are views for explaining a method of manufacturing the DRAM shown in Figures 2A and 2B;

Figure 13A is a plan view showing the essential

portions of a memory cell in order to explain a second embodiment of the DRAM;

Figure 13B is a sectional view taken along line X-X in Figure 13A;

Figures 14A to 15B are views for explaining a method of manufacturing the DRAM in Figures 13A and 13B

Figure 16A is a plan view showing the essential portions of a memory cell in order to explain a third embodiment of the DRAM;

Figure 16B is a sectional view taken along line X-X in Figure 16A;

Figures 17A to 18B are views for explaining a method of manufacturing the DRAM shown in Figures 16A and 16B; and

Figure 19 is a sectional view showing a modification of the third embodiment of the DRAM.

Referring first to Figure 1 the first embodiment of the DRAM includes:

sense amplifiers SA_1, SA_2, each of which serves to amplify the minute potential difference between a predetermined memory cell and a predetermined dummy cell; bit lines BL_{11} and BL_{12} which extend in an identical direction from the sense amplifier SA_1, bit lines BL_{21} and BL_{22} which extend in an identical direction from the sense amplifier SA_2, these bit lines BL serving to transmit information; word lines WL_1 and WL_2 which extend in a direction intersecting the bit lines; word lines WL_3 and WL_4 which extend in the same direction as that of the word lines WL_1 and WL_2.

The DRAM also includes: memory cells M_{11}, M_{12}, M_{21}, M_{22} ....., which hold charges serving as

the information, the respective memory cells M_{11}, M_{12}, M_{21}, M_{22} ..... consisting of MISFETs Q_{11}, Q_{12}, Q_{21}, Q_{22} ..... and capacitors C_{11}, C_{12}, C_{21}, C_{22} ..... Each of the MISFETs Q_{11}, Q_{12}, Q_{21}, Q_{22} ..... has one end connected to the predetermined bit line BL, and has a gate electrode connected to the predetermined word line WL. Each of the capacitors C_{11}, C_{12}, C_{21}, C_{22} ..... has one end connected to the other end of the corresponding one of the MISFETs Q_{11}, Q_{12}, Q_{21}, Q_{22} ....., and has the other end connected to a fixed potential V_{SS} (zero V) terminal.

The DRAM also includes dummy cells D_{11}, D_{12}, D_{21}, D_{22}, ... for holding charges with which whether the information of the memory cells is "1" or "0" can be judged. The respective dummy cells D_{11}, D_{12}, D_{21}, D_{22} .... are composed of MISFETs Q_{D11}, Q_{D12}, Q_{D21}, Q_{D22} ....., capacitors C_{D11}, C_{D12}, C_{D21}, C_{D22} ....., and MISFETs CQ. Each of the MISFETs Q_{D11}, Q_{D12}, Q_{D21}, Q_{D22} ..... has one end connected to the predetermined bit line BL, and has a gate electrode connected to the predetermined word line WL. Each of the capacitors C_{D11}, C_{D12}, C_{D21}, C_{D22}, ... has one end connected to the other end of the

corresponding one of the MISFETs Q_{D11}, Q_{D12}, Q_{D21}, Q_{D22} ....., and has the other end connected to the fixed potential V_{SS} terminal. The MISFETs CQ are provided for discharging (clearing) the charges stored in the capacitors C_{D11}, C_{D12}, C_{D21}, C_{D22} .....

A terminal ϕ_D is provided for applying a discharge signal to the gate electrode of the MISFET CQ.

The structure of the DRAM shown in the first embodiment will now be explained in greater detail with reference to Figures 2A and 2B and also Figure 3. In Figure 3, in order to clarify the drawing, insulator films to be formed between conductive layers are not shown.

The structure of the DRAM includes:

a p-type semiconductor substrate 1 which is made of single-crystal silicon (Si); a field insulator film 2 which is formed between the adjacent memory cells in one major surface of the semiconductor substrate 1, and which serves to electrically isolate them. The field insulator

film 2 integrally surrounds two memory cells which are connected to a bit line 22 through an identical contact hole 21. The memory cell array is such that the memory cells are arranged in the shape of a matrix as shown in Figure 3, with repeated fundamental units each of which consists of the two memory cells integrally surrounded with the field insulator film. The MISFETs Q of the two memory cells share an n^+-type semiconductor region 19 which is connected to the bit line 22.

The capacitor C of the memory cell is composed of a first electrode (hereinbelow, termed "first capacitor plate") 9 indicated by a dot-and-dash line, a second electrode (hereinbelow, termed "second capacitor plate") 16, and an insulator film 11 interposed therebetween. The first and second capacitor plates 9 and 16 are made of a conductor.

The first capacitor plate 9 is connected to the MISFET Q of the memory cell. The second capacitor plate 16 has the fixed potential V_{SS} applied thereto. The capacitor C is essentially formed so as to be buried in a moat (U-groove) 6 which, in turn, is formed in a manner to extend from a predetermined part of the major surface of the semiconductor substrate 1 thereinto. To the end of increasing the capacitance of the capacitor C, the moat 6 is not made an oblong, but it is made a

shape clearly shown in Figure 2A. An insulator film is formed inside the moat 6, namely, on the surfaces of the semiconductor substrate 1 corresponding to the side surface and bottom surface of the moat 6, and which serves to electrically isolate the semiconductor substrate 1 and the first capacitor plate 9. The insulator film 7 is thicker than an insulator film 3A. Whatever voltage is applied to the first capacitor plate 9, no information is stored in the peripheral part of the moat 6 within the semiconductor substrate 1. When the potential of the first capacitor plate 9 is zero V, the capacitance between the semiconductor substrate 1 and the first capacitor plate 9 is very low. When the potential of the first capacitor plate 9 is 5 V, merely a depletion layer spreads in the surface of the semiconductor substrate 1, and charges to form an inversion layer are not supplied from the semiconductor region 19.

A contact hole 8 is provided by removing a predetermined part of the insulator film 3A in order to connect the first capacitor plate 9 and one semiconductor region 19 constituting the MISFET. The first capacitor plate 9 is formed on the insulator film 7, the insulator film 3A and the semiconductor region 19. The contact holes 8 are omitted from Figure 3. For example, zero V or 5 V is applied to

the first capacitor plate 9 in correspondence with the information. The respective first capacitor plates 9 of the adjacent memory cells are structurally and electrically isolated. As shown by dot-and-dash lines in Figure 3, the first capacitor plates 9 are independently arranged for the respective memory cells. The insulator film 11 and the second capacitor plate 16 of the memory cells are common to the memory cells in the identical memory cell array, and are integrally formed. As seen from Figure 3, the insulator film 11 and the second capacitor plate 16 are not formed in the selected regions in which the MISFETs Q of the memory cells are provided. The charges as the information are stored in that part of the insulator film 11 which is sandwiched between the first capacitor plate 9 and the second capacitor plate 16. A filling material 14 is buried in the moat 6. It serves to alleviate a depression which will appear over the moat 6 in the case where this moat 6 is not filled up with a conductive material and an insulator material.

The second capacitor plate 16 and the filling material 14 are electrically isolated from a gate electrode and word line 18(WL) by insulator films 15 and 15A.

The MISFET Q comprises a gate insulator film 17, the gate electrode 18, and the n^+-type semiconductor

regions 19 each of which is a source or drain region. The gate insulator film 17 is provided on that part of the major surface of the semiconductor substrate 1 in which the MISFETs are formed. The gate electrode 18 is unitary with the word line WL for applying a voltage to this gate electrode 18. The semiconductor regions 19 are provided on both the sides of the gate electrode 18 in the surface of the semiconductor substrate 1 corresponding to the MISFET forming part. The semiconductor region 19 is defined by the gate electrode 18, the field insulator film 2 and the first capacitor plate 9. The word line WL extends over the moat 6 whose surface is flattened.

An insulator film 20 is formed between the gate electrode 18 or word line WL and the bit line 22, and which electrically isolates them. The contact hole 21 serves to connect the semiconductor region 19 and the bit line 22. The bit line 22 is arranged so as to extend on the insulator film 20 and to connect with the semiconductor regions 19 through the contact holes 21 in predetermined parts.

The operation of the first embodiment of the DRAM will now be described with reference to Figures 2A and 2B, by exemplifying the memory cell which consists of the MISFET Q and the capacitor C.

The case of writing information into the memory cell will be explained. When a control voltage is applied to the gate electrode constituting the MISFET Q of the memory cell, this MISFET Q is turned ON. A voltage corresponding to the information is applied to the bit line (BL) 22 which is connected to the semiconductor region 19 of the MISFET Q remote from the capacitor C with respect to the gate electrode. Thus, the voltage of the bit line (BL) 22 corresponding to the information is applied to the first capacitor plate 9 through the MISFET Q. When a potential difference exists between the first capacitor plate 9 and the second capacitor plate 16 held at the fixed potential V_{SS}, charges to serve as the information are stored or written in the capacitor C. Thereafter, in order to retain the information in the memory cell, the MISFET Q is turned OFF.

In the case of reading out the information of the memory cell, the reverse operation to the above writing operation may be performed.

According to the first embodiment, the capacitor of the memory cell can be formed within the moat which is electrically isolated from the semiconductor substrate, with the result that the leakage phenomenon between this capacitor and the capacitor of the adjacent memory cell can be prevented.

In order to electrically isolate the adjacent memory cells more, a channel stopper region of, e.g., the p^+-type may well be formed in the part of the semiconductor substrate 1 under the field insulator film 2.

The method of manufacturing the DRAM of the first embodiment will now be described in greater detail with reference to Figures 4 to 12, which show the various steps in the process of manufacture. It should be noted that the B Figures are sectional views taken along lines X-X in the corresponding A Figures.

A p-type semiconductor substrate 1 made of single-crystal silicon (Si) is prepared. As shown in Figures 4A and 4B, the semiconductor substrate 1 is covered selectively with a field insulator film (SiO_2 film) 2 being 0.6 - 1 μm thick in order to electrically isolate adjacent memory cells and the semiconductor elements (not shown) of peripheral circuits, for example, an addressing circuit, a reading circuit and a writing circuit. The field insulator film 2 is formed by a conventional selective thermal oxidation technique for the surface of the semiconductor substrate 1 employing a silicon nitride film as an oxidation

impermeable mask.

Although not shown, a p^+-type channel stopper region should desirably be formed on the surface of the semiconductor substrate 1 under the field insulator film 2. In this regard, before the field insulator film 2 is formed, a p-type impurity such as boron is ion-implanted into the semiconductor substrate 1 by the use of the oxidation impermeable mask. During the thermal oxidation, the boron is diffused to form the channel stopper region.

After the step illustrated in Figures 4A and 4B, an insulator film 3 is formed on the whole surface of the semiconductor substrate 1. As the insulator film 3, a silicon dioxide (SiO_2) film being 300 Å thick and formed by the thermal oxidation of the surface of the semiconductor substrate 1 is used by way of example. Thereafer, an insulator film 4 to serve as an oxidation impermeable mask is formed on the insulator film 3. As the insulator film 4, a silicon nitride (Si_3N_4) film being 500 Å thick and formed by the chemical vapour deposition (CVD) is used by way of example. Thereafter, an insulator film 5 which serves as a mask for dry etching for forming moats and which is thicker than the insulating film 3 is formed on the insulator film 4. As the insulator film 5, a silicon dioxide film being 8000 Å and formed by the CVD is used by way of example. The insulator

film 5 is patterned to form the mask for providing the moats 6 which constitute the capacitors of memory cells. Using this mask, the insulator films 4 and 3 are successively removed, and then, the semiconductor substrate 1 is removed, by the anisotropic dry etching such as reactive ion etching (RIE) with CCl_4-gas. Thus, the moats 6 are formed as shown in Figures 5A and 5B. The widthwise dimension W of the moat 6 is approximately 1 - 1.5 μm, while the depth D thereof from the surface of the semiconductor substrate 1 is approximately 3 μm. The ratio of the etching rates of silicon and silicon dioxide for the CCl_4-gas is 4 : 1. The depth D can be varied by varying the thickness of the insulator film 5.

After the steps illustrated in Figures 5A and 5B, the insulator film 5 having served as the mask for the dry etching is removed, and the insulator film 4 to serve as the mask for the thermal oxidation is exposed. Using the insulator film 4 as the mask, the surface of the semiconductor substrate 1 exposed in the moat 6 is thermally oxidized, thereby to form an SiO_2 film 7 of 4000 - 6000 Å sufficiently thicker than the insulator film 3 on the inside surface, i. e., the side surface and bottom surface of the moat 6. The SiO_2 film 7 electrically isolates the semiconductor substrate 1 and the first capacitor plate. This state is shown in Figures 6A and 6B.

After the step illustrated in Figures 6A and 6B, the insulator films 4 and 3 are successively removed. The exposed surface of the semiconductor substrate 1 is thermally oxidized to form a new SiO_2 film 3A which is 300 Å thick. The predetermined part of the SiO_2 film 3A is removed to form a contact hole 8. This contact hole serves to connect the first capacitor plate and one semiconductor region to constitute a MISFET. Thereafter, polycrystalline silicon which is a conductive material is deposited on the whole area of the semiconductor substrate 1 to a thickness of 1000 Å, and phosphorus is introduced thereinto in order to establish a low resistivity. The polycrystalline silicon is patterned to form the first capacitor plate 9 constituting the capacitor of the memory cell as shown in Figures 7A and 7B. The thickness of the polycrystalline silicon film is approximately 500 - 1000 Å. An n-type semiconductor region 10 of 60 Ω/□ is formed by the diffusion of phosphorus into the semiconductor substrate 1 from the polycrystalline silicon within the contact hole 8.

After the steps illustrated in Figures 7A and 7B, an insulator film (not shown) made of silicon dioxide and having a thickness of 60 Å by way of example is formed on the exposed surface of the first capacitor plate 9. This insulator film is formed by the thermal

oxidation of the surface of the polycrystalline silicon film which makes the first capacitor plate 9. This insulator film serves to moderate a stress which develops due to the difference between the coefficients of thermal expansion of the first capacitor plate 9 and an insulator film 11 to be formed by a later step, and also to reduce the leakage current of the insulator film 11. Thereafter, the insulator film 11 for storing charges to serve as information is formed on the whole surface of the resultant semiconductor substrate 1 by the CVD. As the insulator film 11, a film of silicon nitride higher in the dielectric constant than silicon dioxide is used by way of example, and its thickness is approximately 150 Å. Thereafter, in order to reduce the leakage current of the insulator film 11, an insulator film (not shown) made of silicon dioxide and having a thickness of 20 Å is formed on the insulator film 11 by, e. g., the thermal oxidation of the insulator film 11. Subsequently, in order to form the second capacitor plate which constitutes the capacitor of the memory cell, polycrystalline silicon 12 is deposited on the whole surface of the resultant semiconductor substrate 1. Phosphorus is introduced into the polycrystalline silicon in order to lower the resistivity thereof. The thickness of the polycrystalline silicon film 12 is approximately 3500 Å. As shown in

Figure 8, an insulator film 13 is formed for the electrical isolation between the polycrystalline silicon 12 and a conductive material to be deposited thereon. This insulator film 13 is, for example, an SiO_2 film of 500 Å which is formed by the thermal oxidation of the surface of the polycrystalline silicon 12. The CVD may well be employed as the method of forming the insulator film 13.

After the steps illustrated in Figure 8, in order to fill up the moats 6, a filling material 14 is deposited on the whole surface of the resultant semiconductor substrate 1 to a thickness of, e. g., 5000 Å. The filling material 14 other than parts buried in the moats 6 is removed. The surface of the filling material 14 and the exposed surface of the polycrystalline silicon 12 are made substantially even. Thus, depressions over the moats 6 are alleviated. The filling material 14 is, for example, polycrystalline silicon. The removal of the filling material 14 is executed by isotropic etching, for example, plasma etching. The insulator film 13 protects the polycrystalline silicon 12 during the removal of the filling material 14. It is effective that the polycrystalline silicon 12 and the filling material 14 are the same material. Thereafter, the surface of the filling material 14 is thermally oxidized. Simultaneously, the surface of the polycrystalline silicon

12 is further oxidized. An insulator film 15 (SiO_2 film) which is 2000 Å thick is formed by the thermal oxidation. The insulator film 15 and the polycrystalline silicon 12 in an area to form the MISFET are removed, and the second capacitor plate 16 to constitute the capacitor of the memory cell is formed. Thereafter, an insulator film (SiO_2 film) 15A is formed as shown in Figure 9 in such a way that the exposed part of the polycrystalline silicon on the side surface of the second capacitor plate 16 is thermally oxidized using the insulator film 11 as a mask. The insulator film 11 is partly removed as shown in Figure 9 before the insulator film 15A is formed. As a result, the insulator film 11 is divided into a part underlying the second capacitor plate 16 and a part overlying the area to form the MISFET. A high precision of registration is not necessary for this etching.

After the steps illustrated in Figure 9, the insulator films 11 and 3 in the area to form the MISFET of the memory cell are removed. In the removed area, an insulator film 17 is formed as shown in Figures 10A and 10B to the end of forming a gate insulator film to constitute the MISFET. The insulator film 17 is formed by thermally oxidizing the surface of the semiconductor substrate 1 exposed by the removal of the insulator films 11, 3.

It is an SiO_2 film which is 300 Å thick.

After the steps illustrated in Figures 10A and 10B, a conductive material is deposited in order to form a gate electrode constituting the MISFET of the memory cell, as well as a word line. As the conductive material, there is employed polycrystalline silicon, a high-melting metal such as molybdenum (Mo) or tungsten (W), a silicide which is the compound between the high-melting metal and silicon, or a double-layer structure which consists of the polycrystalline silicon and the high-melting metal silicide overlying it. As regards thicknesses, a value of 3000 - 4000 Å is preferable for the polycrystalline silicon layer, and a high-melting metal silicide layer of 3000 Å and a polycrystalline silicon layer of 2000 Å are preferable for the double-layer structure consisting of the high-melting metal silicide (WSi_2) layer and the polycrystalline silicon layer. To be used as the high-melting metal silicides are tungsten silicide, molybdenum silicide, tantalum silicide and titanium silicide. The conductive material is patterned to form the gate electrodes and word lines 18. Using the gate electrodes and word lines 18 as an impurity introducing mask, an n^+-type impurity is ion-implanted into the semiconductor substrate 1 of the area to form the MISFET of the memory cell. The impurity is diffused

by the drive-in diffusion, to form n^+-type semiconductor regions 19. Thus, the MISFET Q is formed as shown in Figures 11A and 11B.

After the steps illustrated in Figures 11A and 11B, an insulator film 20 is formed on the whole surface of the resultant semiconductor substrate in order to electrically isolate the gate electrodes and word lines 18 and bit lines. Used as the insulator film 20 is, for example, a phosphosilicate glass (PSG) film which is 6000 - 8000 Å. The PSG film can alleviate the growth of undulations due to the multi-layering, and can capture sodium (Na) ions affecting the characteristics of a semiconductor integrated circuit device. The insulator films 20 and 17 on the other semiconductor region 19, which is remote with respect to the gate electrode 18 from one semiconductor region of the MISFET Q connected to the capacitor of the memory cell, are removed. Thus, a contact hole 21 for connecting the semiconductor region 19 and the bit line is formed. Thereafter, as shown in Figures 12A and 12B, the bit line 22 is formed so as to connect with the semiconductor region 19 through the contact hole 21. For example, an aluminium (Al) layer being 7000 Å thick is used as the bit line 22. Thereafer, a PSG film and a silicon nitride film by the plasma CVD overlying it are formed as a final passivation

film.

The semiconductor integrated circuit device of the present embodiment is completed by these series of manufacturing steps.

Referring now to the second embodiment of the DRAM shown in Figures 13A and 13B, a different insulator film is used for that field insulator film in the first embodiment which lies between the two memory cells connected to the same bit line and having the capacitors adjacent to each other.

Throughout the figures concerning the second embodiment, portions having the same functions as in the first embodiment are assigned the same symbols, and they shall not be repeatedly explained. In Figure 13A, gate electrodes and word lines 18(WL) are indicated by solid lines in order to clarify the illustration.

Referring to Figures 13A and 13B, the DRAM includes an insulator film 23 which is formed on the surface of the semiconductor substrate 1 within the moat 6A and which is thicker than the insulator film 3A. The insulator film 23 electrically isolates the semiconductor substrate 1 and the first capacitor plate 9. The insulator film 23A electrically isolates the capacitors of two memory cells which are connected to the same bit line (BL) 22 and whose capacitors

are adjacent to each other. The insulator film 23A between the capacitors can be readily provided by the thermal oxidation from the inside surface of the moat 6A during the formation of the insulator film 23.

According to the present embodiment, the capacitors can be arranged within the moats which are electrically isolated from the semiconductor substrate.

In addition, the field insulator film having the bird's beak is not required for the isolation between the capacitors of the adjacent memory cells.

The method of manufacturing the DRAM of the second embodiment will now be described in greater detail with reference to Figures 14 and 15 which show the various steps in the process of manufacture. It should be noted that the sectional views of the B Figures are taken along lines X-X in the corresponding A Figures.

In similar manner to the process of manufacture of the first embodiment, a p-type semiconductor substrate 1 is first prepared. A field insulator film is formed for electrically isolating semiconductor elements (not shown) which constitute

the peripheral circuits of the memory cells of the semiconductor substrate 1, for example, an addressing circuit, a reading circuit and a writing circuit. This point is the same as in the first embodiment. In the memory cell of the semiconductor substrate 1, a field insulator film 2A is formed as shown in Figures 14A and 14B. The field insulator film 2A is formed as in the first embodiment except the portion between the two memory cells which are connected to the same bit line and whose capacitors are adjacent to each other. The field insulator film 2A is formed by the well-known selective thermal oxidation of the semiconductor substrate 1. It is an SiO_2 film which is 0.6 - 1 μm thick.

After the step illustrated in Figures 14A and 14B, moats 6A are formed by the same method as in the first embodiment, employing the insulator films 3, 4 and 5. The width and depth of the moat 6A may be similar to those in the first embodiment. As seen from Figure 15A, the shape of the insulator films 4 and 5 is such that the field insulator film 2A is partly exposed. A mask for forming the moats 6A is composed of the field insulator film 2A and the insulator film 5. The moats 6A can be formed in partial self-alignment with the field insulator film 2A. This leads to increase in the capacitances of the capacitors. The distance between the respective

moats 6A of the two memory cells connected to the same bit line and having the adjacent capacitors should preferably be small, for example, 1 μm.

Thereafter, the insulator film 5 is removed to expose the insulator film 4. Using the insulator film 4, the semiconductor substrate 1 exposed in the moats 6A is thermally oxidized. Thus, insulator films 23 and 23A made of an SiO_2 film are formed. The insulator film 23 extends along each moat 6A and is sufficiently thicker (4000 - 6000 Å) than the insulator film 3A, and it electrically isolates the semiconductor substrate 1 and the first capacitor plate. The insulator film 23A especially achieves the electrical isolation between the capacitors (moats 6A) of the two memory cells connected to the same bit line and having the adjacent capacitors. This insulator film 23A has heat-treatment conditions etc. controlled in order that the semiconductor substrate 1 of the corresponding part may become SiO_2 perfectly.

After the steps illustrated in Figures 15A and 15B, the steps of the manufacturing method of the first embodiment illustrated in Figures 5A and 5B, et seq. are similarly performed, whereby the semiconductor integrated circuit device of the present invention is finished up.

Referring now to the third embodiment of

the DRAM shown in Figures 16A and 16B, the insulator film 3A of the second embodiment is replaced with a still thicker insulator film 23B.

Throughout the figures concerning the third embodiment, parts having the same functions as in the first and second embodiments are assigned the same symbols, and they shall not be repeatedly explained. In Figure 16A, gate electrodes and word lines 18(WL) are indicated by solid lines for clear illustration.

The DRAM of the third embodiment includes an insulator film 23B which is formed between the semiconductor substrate 1 and the first capacitor plate 9 outside the moat 6 so as to be sufficiently thicker than the insulator film 3A employed in the first and second embodiments. The insulator film 23B electrically isolates the semiconductor substrate 1 and the first capacitor plate. Even when a voltage corresponding to information is applied to the first capacitor plate 9, charges to serve as the information are scarcely stored in the surface of the semiconductor substrate 1. No charge to serve as the information of the memory cell exists in the semiconductor substrate 1.

According to a modified form of the third embodiment, the capacitor can be provided in only the moat which is

electrically isolated from the semiconductor substrate. As will be stated below, the process of the third embodiment becomes more complicated than those of the first and second embodiments. Since, however, the insulator film 23B is thick, the capacitance between the first capacitor plate 9 and the semiconductor substrate 1 is quite negligible. Thus, the DRAM of the third embodiment is less liable to the influence of the potential fluctuation of the surface of the semiconductor substrate 1 by minority carriers created by α particles.

In addition, no field insulator film is required for the isolation of the capacitors of the adjacent memory cells.

The method of manufacturing the DRAM of the third embodiment will now be described in greater detail with reference to Figures 17 and 18 which show the various steps in the process of manufacture. It should be noted that the sectional views of the B Figures are taken along lines X-X in the corresponding A Figures.

As in the second embodiment, a p-type semiconductor

substrate 1 is prepared. As shown in Figures 17A and 17B, an insulator film 2A similar to that of the second embodiment is formed on the semiconductor substrate 1.

After the step illustrated in Figures 17A and 17B, the step of the second embodiment shown in Figures 15A and 15B is performed to simultaneously form moats 6 and insulator films 23, 23A. The insulator films 23 and 23A have equal thicknesses (4000 - 6000 Å). Thereafter, an insulator film 4 is removed, and an insulator film 4A to serve as a mask for thermal oxidation is formed by the CVD on parts other than the portions of the moats 6 and the semiconductor substrate 1 on which the first capacitor plates are formed. For example, a silicon nitride film 500 Å thick is used as the insulator film 4A. Using the insulator film 4A, the semiconductor substrate 1 is thermally oxidized to form insulator films 23B for electrically isolating the semiconductor substrate 1 and the first capacitor plates as shown in Figures 18A and 18B.

After the steps illustrated in Figures 18A and 18B, the steps of the manufacturing method of the first embodiment shown in Figures 5A and 5B et seq. are similarly performed, whereby the semiconductor integrated circuit device of the present embodiment is finished up.

The insulator film 4 can be used instead of the

insulator film 4A without being removed. In this case, after the formation of the moats 6, the insulator film 4 is selectively etched and removed to provide a mask having the same shape as that of the insulator film 4A.

In the above embodiments, the capacitor is provided within the moat which is electrically isolated from the semiconductor substrate. Thus, depletion layers which extend into the semiconductor substrate from the respective capacitors of the adjacent memory cells can be removed. Accordingly, the phenomenon of leakage to the respective capacitors of the adjacent memory cells is prevented. Moreover, minority carriers to be created within the semiconductor substrate by α particles can be prevented from affecting charges to serve as information. Further the capacitor of high capacitance can be formed in a small occupying area.

Since the capacitor is formed on the insulator film, not in the semiconductor substrate, no leakage current is involved between the capacitor and the substrate, and the information retention time can be remarkably prolonged.

Since the capacitors of the adjacent memory cells in a predetermined direction can be electrically

isolated without using the field insulator film the density of integration in a memory array portion can be enhanced.

Even when the moat has a widthwise dimension above approximately 1 μm, it is filled up with the first capacitor plate, the second capacitor plate and the filling material. The upper part of the moat is flattened, and the working dispersions of the word line and the bit line to be formed over the moat can be reduced.

The following modifications of the above described embodiments are possible.

As the filling material 14, it is also possible to employ silicon dioxide instead of the polycrystalline silicon.

As shown in the modified form of the third embodiment of Figure 19, the polycrystalline silicon of the second capacitor plate 16 may well be used for filling up the moat 6 so as to flatten the surface thereof, without employing any filling material 14. In this case, the insulator film 13 is thick. This measure dispenses with the steps of depositing and etching the filling material 14 and the step of forming the insulator film 15. Regarding the first and second embodiments, the polycrystalline silicon of the second

capacitor plate 16 may be similarly buried in the moat 6 so as to flatten the surface thereof without using the filling material 14.

As the insulator film 11 of the capacitor, a silicon dioxide (SiO_2) film can also be employed.

Whilst all the above described embodiments relate to the DRAMs of the folded bit line type, the present invention is also applicable to DRAMs of the open bit line type.

The conductivity types of the semiconductor substrate and the semiconductor regions may well be the opposite to those in each embodiment. The memory cells may well be provided within semiconductor regions (wells) which are formed in the semiconductor substrate and which have the conductivity type opposite to that of the semiconductor substrate.

CLAIMS

1. A semiconductor memory device including:

(a) a semiconductor substrate which has one major surface;

(b) memory cells each of which comprises a MISFET and a capacitor connected in series with said MISFET, said MISFET including a gate electrode and source or drain region, said capacitor including a first conductor layer, a first insulator film formed on said first conductor layer and a second conductor layer formed on said first insultaor layer, at least one of said conductor layers being made of at least a polycrystalline silicon layer, and said first conductor layer being connected to one of said source or drain region and being arranged independently for said each capacitor of said memory cell;

(c) moats which are formed on said major surface side of said semiconductor substrate by partly removing said semiconductor substrate, which are provided in correspondence with said capacitors and each of which has its inside surface covered with a second insultor film;

(d) a first part of said capacitor being provided on a whole surface of said second insulator film in said moat, a second part thereof other than said first part being provided on a third insulator film formed on said

semiconductor substrate except a part where said first conductor layer of said second part is connected to one of said source or drain regions, said second and third insulator films being integrally provided;

(e) word lines which extend in one direction over said semiconductor substrate, and each of which is connected with the gate electrodes of the MISFETs; and

(f) data lines which extend in a direction intersecting said word lines over said semiconductor substrate, and each of which is connected with the others of the source or drain regions of the MISFETs, said memory cells being provided in correspondence with respective intersection points between said word lines and said data lines.

2. A semiconductor memory device according to claim 1, wherein both said first and second conductor layers are polycrystalline silicon layers, and said second and third insulator films are silicon dioxide films.

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3. A semiconductor memory device according to claim 2, wherein the surface of said second conductor layer of said first part of said capacitor is substantially flat.

4. A semiconductor memory device according to claim 1, wherein said second insulator film is thicker than said third insulator film.

5. A semiconductor memory device according to claim 1, wherein said second insulator film is substantially equal in thickness to said third insulator film.

6. A semiconductor memory device according to claim 1, wherein said first insulator film and said second conductor layer are provided as being common to the capacitors of the plurality of memory cells.

7. A semiconductor memory device according to claim 1, further including :

(g) a filling material which is formed over said second conductor layer of said first part of said capacitor, which is provided so as to fill up a depression of the surface of said second conductor layer of said first part and which is electrically isolated from said second conductor layer.

8. A semiconductor memory device according to claim 7, wherein said filling material is provided so as to have a surface which is substantially even with the surface of said second conductor layer of said second part of said capacitor.

9. A semiconductor memory device according to claim 8, wherein said filling material is polycrystalline silicon which is electrically isolated from said second conductor layer by a fourth insulator film formed on said second conductor layer.

10. A semiconductor memory device according to claim 8, wherein said filling material is silicon dioxide.

11. A semiconductor memory device according to claim 1, further including:

(h) a fifth insulator film which isolates the adjacent memory cells, and which surrounds at least an area where said capacitor is formed and an area where said MISFET is formed, except the source or drain region of said MISFET connected to said data line.

12. A semiconductor memory device according to claim 11, wherein said fifth insulator film is a silicon dioxide film.

13. A semiconductor memory device according to claim 12, wherein said fifth insulator film which isolates the adjacent two moats corresponding to said capacitors of said memory cells connected to the identical bit line is substantially equal to said second insulator film, is about twice as thick as said second insulator film and is formed integrally with said second insulator film.

14. A semiconductor memory device according to claim 12, wherein at least a part of said moat is defined by said fifth insulator film.

15. A method of manufacturing a semiconductor memory device, said semiconductor memory device including memory cells each consisting of a MISFET and a capacitor and moats formed in correspondence with the capacitors, said capacitor consisting of a first conductor layer, a first insulator film formed on said first conductor layer and a second conductor layer formed on said first insulator film, at least one of said conductor layers being made of at least a polycrystalline layer, said method including the steps of:

(a) forming a mask for forming said moats, on one major surface of a semiconductor substrate;

(b) forming said moats on the major surface side of said semiconductor substrate by partly removing said semiconductor substrate by the use of said mask;

(c) covering an inside surface of said each moat with a second insulator film and covering at least a part of the major surface of said semiconductor substrate with a third insulator film, said second and third insulator films being integrally formed;

(d) forming said first conductor layer on said second

insulator film within said moat, on said third insulator film and on said semiconductor substrate, said first conductor layer being formed independently for said each memory cell and being connected to said MISFET in its area contacting with said semiconductor substrate; and

(e) forming said first insulator film on at least said first conductor layer, and forming said second conductor layer on said first insulator layer.

16. A method of manufcturing a semiconductor memory device according to claim 15, wherein both said first and second conductor layers are polycrystalline silicon layers.

17. A method of manufacturing a semiconductor memory device according to claim 16, wherein said second conductor layer is formed so that its surface may become substantially flat.

18. A method of manufacturing a semiconductor memory device according to claim 15, wherein :

said mask comprises a first mask and a second mask which is formed on said first mask, both said masks having the same shape;

said step (b) comprises:

(i) forming said moats by partly removing said semiconductor substrate by the use of said second mask; and

(ii) removing said second mask; and

said step (c) comprises:

(i) forming said second insulator film on the inside surface of said each moat by thermally oxidizing the exposed semiconductor substrate by the use of said first mask, said first mask being an oxidation impermeable mask;

(ii) removing said first mask; and

(iii) forming said third insulator film by thermally oxidizing said major surface of said semiconductor substrate, said third insulator film being thinner than said second insulator film.

19. A method of manufacturing a semiconductor memory device according to claim 15, wherein:

said mask comprises a first mask and a second mask which is formed on said first mask, both said masks having the same shape;

said step (b) comprises:

(i) forming said moats by partly removing said semiconductor substrate by the use of said second mask; and

(ii) removing said second mask; and

said step (c) comprises:

(i) selectively removing said first mask;

(ii) forming said second insulator film on the inside surface of said each moat and said third insulator film on said major surface of said semiconductor substrate by thermally oxidizing the exposed semiconductor substrate by the use of the selectively removed first mask, said second and third insulator films having substantially equal thicknesses, said first mask being an oxidation impermeable mask; and

(iii) removing said first mask.

20. A method of manufacturing a semiconductor memory device according to claim 15, further including:

(f) forming a filling material over said second conductor layer, said filling material being formed so as to fill up a depression of a surface of that part of said second conductor layer which is formed in said each moat, said filling material being electrically isolated from said second conductor layer.

21. A method of manufacturing a semiconductor memory device according to claim 20, wherein said filling material is formed so that its surface may be substantially even with the surface of said second conductor layer formed over said major surface of said semiconductor substrate.

22. A method of manufacturing a semiconductor memory device according to claim 20, wherein:

said filling material is polycrystalline silicon; and

said step (f) comprises:

(i) covering the surface of said second conductor layer with a fourth insulator film; and

(ii) forming said filling material on said fourth insulator film.

23. A method of manufacturing a semiconductor memory device according to claim 15, further including:

(g) forming, before said step (a), a fifth insulator film on said major surface of said semiconductor substrate by selective thermal oxidation thereof, said fifth insulator film isolating the adjacent memory cells.

24. A method of manufacturing a semiconductor memory device according to claim 23, wherein said moats are formed by partly removing said semiconductor substrate by employing said mask and said fifth insulator film as a mask.

25. A method of manufacturing a semiconductor memory device according to claim 23, wherein:

said mask comprises a first mask and a second mask which is formed on said first mask, both said masks having the same shape;

said step (b) comprises:

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(i) forming said moats by partly removing said semiconductor substrate by employing said second mask and said fifth insulator film as a mask; and

(ii) removing said second mask; and

said step (c) includes:

(i) forming at least said second insulator film on said semiconductor substrate by thermally oxidizing the exposed semiconductor substrate by employing said first mask and said fifth insulator film as a mask, said first mask being an oxidation impermeable mask.

26. A method of manufacturing a semiconductor memory device according to claim 23, wherein said memory cells are isolated by said second and fifth insulator films, said second insulator film isolates nearest parts of the two adjacent moats among said moats of said memory cells, said second insulator film is formed on the inside surface said each moat by thermally oxidizing the exposed semiconductor substrate said second insulator film formed on said inside surface of one of said two adjacent moats is integral with said second insulator film formed on said inside surface of the other moat, and said fifth insulator film isolates parts other than said parts isolated by said second insulator film.

27. A semiconductor memory device including:

(a) a semiconductor substrate which has one major surface;

(b) memory cells each of which comprises a MISFET and a capacitor connected in series with said MISFET, said MISFET including a gate electrode and source or drain region, said capacitor including a first conductor layer, a first insulator film formed on said first conductor layer and a second conductor layer formed on said first insulator layer, said first conductor layer being connected to one of said source or drain region and being arranged independently for said each capacitor of said memory cell;

(c) moats which are formed on said major surface side of said semiconductor substrate, the inside surfaces of which are covered with a second insulator film, the respective capacitors each being formed wholly within a respective moat;

(d) word lines which extend in one direction over said semiconductor substrate, and each of which is connected with the gate electrodes of the MISFETs; and

(e) data lines which extend in a direction intersecting said word lines over said semiconductor substrate, and each of which is connected with the others of the source or drain regions of the MISFETs, said memory cells being provided in correspondence with respective intersection points between said word lines and said data lines.

28 A semiconductor memory device according to claim 27, wherein at least one of said first and second conductor layers is a polycrystalline silicon layer.

29. A semiconductor memory device according to claim 27, wherein said first and second conductor layers are made of respective polycrystalline layers.

30. A semiconductor memory device according to any one of the preceding claims 27 to 29, wherein said second insulator film is a silicon dioxide film.

31. A semiconductor memory device according to any one of the preceding claims 27 to 30 wherein said second insulator film is thicker than said first insulator film.

32. A semiconductor memory device according to any one of the preceding claims 27 to 31, wherein said first insulator film and said second conductor layer are

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provided as being common to the capacitors of the plurality of memory cells.

33. A semiconductor memory device according to any one of the preceding claims 27 to 32, further including:

(f) a filling material which is formed over said second conductor layer of said first part of said capacitor, which is provided so as to fill up a depression of the surface of said second conductor layer of said first part and which is electrically isolated from said second conductor layer.

34. A semiconductor memory device according to claim 33, wherein said filing material is silicon dioxide.

35. A semiconductor memory device according to any one of the preceding claims 27 to 34, further including:

(g) a third insulator film integrally formed with said second insulator film for isolating adjacent moats corresponding to said capacitors of said memory cells, said third insulator film being about twice as thick as said second insulator film.

36. A dynamic random access memory constructed substantially as herein described with reference to and as illustrated in Figures 1 to 3; or Figure 13; or Figure 16 or Figure 19 of the accompanying drawings.

37. A method of manufacturing a dynamic random access memory substantially as herein described in Figures 4 to

12; or Figures 14 and 15 or Figures 17 and 18 of the accompanying drawings.

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