CLAIMS

1. A method of partitioning a via in a multilayer printed circuit board (200) as to produce an electrically isolating portion between two electrically conducting portions in said via, the method comprising the steps of:

- placing (1) at least one island of a first plating resist layer (233) on a first layered structure comprising a first conductive layer (205) and a first dielectric layer (222) and placing (1) at least one island of a second plating resist layer (234) on a second layered structure comprising a second conductive layer (206) and a second dielectric layer (223);

- laminating (2) the first and second layered structures with a third intermediate layered structure comprising at least one third dielectric layer (213) adapted so that the islands of the first and second plating resist layers (233,234) become embedded in the at least one third dielectric layer (213);

- drilling (3) a first hole (240) in the printed circuit board (200) so that the first hole (240) passes through the islands of the first and the second plating resist layer (233,234);

- placing (4) said printed circuit board (200) in a copper seed catalyzing bath so that copper is placed on the interior of the first hole (240) except for the portions (252,253) with the plating resist layer (233,234);

- placing (5) the printed circuit board (200) in a electrolytic copper plating bath where the copper

placed on the at least one third dielectric layer portion (255) of the first hole (240) is electrically isolated from the first and second conductive layers (205,206) so that additional copper is placed on the interior of the first hole (240) except for the portions (252,253) of the first and second plating resist layers (233,234) and except for the portion (255) of the at least one third dielectric layer (213);

- removing (6) the copper placed on the at least one third dielectric layer portion (255) of the first hole (240).

2. A method of claim 1 wherein the third processing step of removing copper from the at least one third dielectric layer portion (255) of the first hole (240) is done by micro etching.

3. A method of any of the preceding claims wherein the at least one third dielectric layer (213) is made of an impregnated fiber weave adapted to embed the islands of the first and second plating resist layers (233,234).

4. A method of any of the preceding claims wherein the first hole (240) is partly penetrating the printed circuit board (200).

5. A method of any of the claims 1-3 wherein the first hole (240) is a through hole through the printed circuit board (200).

6. A method of claim 5 where the step of drilling (3) the first hole comprises the additional step of drilling with a larger drill from the opposite side of the printed circuit board (500) as to produce two portions (530, 535) of the via with different

diameters and where the two via portions (530, 535) meet each other in a position between the first and second plating resist layers (541,542).

7. An apparatus comprising at least one microprocessor and a computer-readable medium including computer-readable instructions, when executed by the at least one microprocessor, are configured to control fabrication equipment to perform the method steps described in any of the preceding claims.

~~8. A multilayer printed circuit board (200) with at least one via (240) having an electrically isolating portion between two electrically conducting portions in said via (240) and where said at least one via is produced according to the method steps described in any of the claims 1 to 6.~~