

CLAIMS

1. A method of video coding a block of a picture, comprising:
 obtaining a residual signal resulting from inter-picture prediction or intra-picture
 5 prediction;
 inferring use of a Discrete Cosine Transform type 2 (DCT2) transform core for a block of a
 sequence of the residual signal;
 processing the transformation of the block using the inferred transform core.
- 10 2. The method according to claim 1, wherein use of DCT2 is inferred from a sequence level
 DCT2 enabled flag in a Sequence Parameter Set (SPS).
3. The method according to claim 2, wherein the sequence level DCT2 enabled flag is
 denoted `sps_dct2_enabled_flag`.
- 15 4. The method according to claim 2 or 3, wherein the sequence level DCT2 enabled flag is
 comprised in a SPS level syntax as follows:

<code>seq_parameter_set_rbsp() {</code>	Descriptor
<code>...</code>	<code>ue(v)</code>
<code>sps_dct2_enabled_flag</code>	
<code>if (! sps_dct2_enabled_flag) {</code>	
<code>sps_mts_intra_enabled_flag</code>	<code>u(1)</code>
<code>sps_mts_inter_enabled_flag</code>	<code>u(1)</code>
<code>}</code>	
<code>...</code>	<code>u(1)</code>
<code>}</code>	

- 20 wherein `sps_dct2_enabled_flag` represents the sequence level DCT2 enabled flag.
5. The method according to any one of claims 2 to 4,
 wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2
 transform core is used for transformation.
- 25 6. The method according to any one of claims 2 to 5,
 wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2

transform core is used for transformation, only.

7. The method according to any one of claims 2 to 6, wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 is used for both horizontal direction
5 transformation as well as vertical direction transformation.
8. The method according to any one of claims 2 to 7, wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 is used in sub block transformation.
- 10 9. The method according to claim 8, wherein in case one side of a residual Transform Unit, tu is greater than 32, a corresponding transform core is set as DCT2.
10. The method according to any one of claims 2 to 9, wherein in case the sequence level DCT2 enabled flag is equal to 1 specifies that the DCT2 transform core is used for
15 transformation, only, both the sub block transform as well as Multiple Transform Selection, MTS, transform are inferred as off.
11. The method according to any one of claim 2 to 8,
wherein the sequence level DCT2 enabled flag being equal to 0 specifies that other
20 transform cores than DCT2 are used for the transformation.
12. The method according to claim 11,
wherein the other transform cores comprise a Discrete Sine Transform type 7 (DST7)
and/or a Discrete Cosine Transform type 8 (DCT8).
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13. The method according to claim 11 or 12, wherein the sequence level DCT2 enabled flag being equal to 0
specifies that it is inferred using at least one of DST7 or DCT8 for transformation.
- 30 14. The method according to any one of claims 11 to 13,
wherein in case the sequence level DCT2 enabled flag being equal to 0, it is determined whether Multiple Transform Selection for Sequence Parameter Set is enabled via a flag.
15. The method according to claim 14,

- wherein in case the `sps_mts_intra_enabled_flag` is present,
in case the `sps_mts_intra_enabled_flag` is equal to 1 it is specified that a
Transform Unit (TU) Multiple Transform Selection (MTS) flag, denote `tu_mts_flag`,
is present in the residual coding syntax for intra coding units;
- 5 in case the `sps_mts_intra_enabled_flag` is equal to 0 it is specified that a
`tu_mts_flag` is not present in the residual coding syntax for intra coding units;
wherein in case the `sps_mts_intra_enabled_flag` is not present, the
`sps_mts_intra_enabled_flag` is inferred to be 0.
- 10 16. An encoder (20) comprising processing circuitry for carrying out the method according
to any one of claims 1 to 15.
17. A decoder (30) comprising processing circuitry for carrying out the method according to
any one of claims 1 to 15.
- 15 18. An decoder (20) comprising:
an obtaining unit, configured to obtain a residual signal resulting from inter-picture
prediction or intra-picture prediction;
an inferring unit, configured to infer use of a Discrete Cosine Transform type 2 (DCT2)
transform core for a block of a sequence of the residual signal; and
- 20 a processing unit, configured to process the transformation of the block using the inferred
transform core.
19. The decoder according to claim 18, wherein the inferring unit is configured to infer use
25 of DCT2 from a sequence level DCT2 enabled flag in a Sequence Parameter Set (SPS).
20. The decoder according to claim 19, wherein the sequence level DCT2 enabled flag is
denoted `sps_dct2_enabled_flag`.
- 30 21. The decoder according to claim 19 or 20, wherein the sequence level DCT2 enabled flag
is comprised in a SPS level syntax as follows:

<code>seq_parameter_set_rbsp() {</code>	Descriptor
<code>...</code>	<code>ue(v)</code>
<code>sps_dct2_enabled_flag</code>	

if (! sps_dct2_enabled_flag) {	
sps_mts_intra_enabled_flag	u(1)
sps_mts_inter_enabled_flag	u(1)
}	
...	u(1)
}	

wherein sps_dct2_enabled_flag represents the sequence level DCT2 enabled flag.

22. The decoder according to any one of claims 19 to 21,
5 wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 transform core is used for transformation.
23. The decoder according to any one of claims 19 to 22,
 wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2
10 transform core is used for transformation, only.
24. The decoder according to any one of claims 19 to 23, wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 is used for both horizontal as well as vertical direction transformation.
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25. The decoder according to any one of claims 19 to 24, wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 is used in sub block transformation.
26. The decoder according to claim 25, wherein in case one side of a residual Transform Unit
20 (tu) is greater than 32, a corresponding transform is set as DCT2.
27. The decoder according to any one of claims 19 to 26, wherein in case the sequence level DCT2 enabled flag is equal to 1 specifies that the DCT2 transform core is used for transformation, only, both the sub block transform as well as Multiple Transform Selection
25 (MTS) transform are inferred as off.
28. The decoder according to any one of claims 19 to 25,
 wherein the sequence level DCT2 enabled flag being equal to 0 specifies that other transform cores than DCT2 are used for the transformation.

29. The decoder according to claim 28,
wherein the inferring unit is configured to infer using a Discrete Sine Transform type 7 (DST7) and/or a Discrete Cosine Transform type 8 (DCT8) for transformation.
- 5 30. The decoder according to claim 28 or 29, wherein the sequence level DCT2 enabled flag being equal to 0
specifies that it is inferred using DST7/DCT8 for transformation, only.
- 10 31. The decoder according to any one of claims 28 to 30,
wherein in case the sequence level DCT2 enabled flag being equal to 0, it is determined whether Multiple Transform Selection for Sequence Parameter Set is enabled via a flag.
32. The decoder according to claim 31,
15 wherein in case the `sps_mts_intra_enabled_flag` is present,
in case the `sps_mts_intra_enabled_flag` is equal to 1 it is specified that a Transform Unit (TU) Multiple Transform Selection (MTS) flag, denote `tu_mts_flag`, is present in the residual coding syntax for intra coding units;
in case the `sps_mts_intra_enabled_flag` is equal to 0 it is specified that a
20 `tu_mts_flag` is not present in the residual coding syntax for intra coding units;
wherein in case the `sps_mts_intra_enabled_flag` is not present, the `sps_mts_intra_enabled_flag` is inferred to be 0.
33. An encoder (20) comprising:
25 an obtaining unit, configured to obtain a residual signal resulting from inter-picture prediction or intra-picture prediction;
an inferring unit, configured to infer use of a Discrete Cosine Transform type 2 (DCT2) transform core for a block of a sequence of the residual signal; and
a processing unit, configured to process the transformation of the block using the inferred
30 transform core.
34. The encoder according to claim 33, wherein the inferring unit is configured to infer use of DCT2 from a sequence level DCT2 enabled flag in a Sequence Parameter Set (SPS).

35. The encoder according to claim 34, wherein the sequence level DCT2 enabled flag is denoted `sps_dct2_enabled_flag`.

36. The encoder according to claim 34 or 35, wherein the sequence level DCT2 enabled flag
5 is comprised in a SPS level syntax as follows:

<code>seq_parameter_set_rbsp() {</code>	Descriptor
<code>...</code>	<code>ue(v)</code>
<code>sps_dct2_enabled_flag</code>	
<code>if (! sps_dct2_enabled_flag) {</code>	
<code>sps_mts_intra_enabled_flag</code>	<code>u(1)</code>
<code>sps_mts_inter_enabled_flag</code>	<code>u(1)</code>
<code>}</code>	
<code>...</code>	<code>u(1)</code>
<code>}</code>	

wherein `sps_dct2_enabled_flag` represents the sequence level DCT2 enabled flag.

37. The encoder according to any one of claims 34 to 36,
10 wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 transform core is used for transformation.

38. The encoder according to any one of claims 34 to 37,
15 wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 transform core is used for transformation, only.

39. The encoder according to any one of claims 34 to 38, wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 is used for both horizontal as well as vertical directions in shape adaptive transform selection.

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40. The encoder according to any one of claims 34 to 39, wherein the sequence level DCT2 enabled flag being equal to 1 specifies that DCT2 is used in sub block transformation.

41. The encoder according to claim 40, wherein in case one side of a residual Transform Unit,
25 `tu` is greater than 32, a corresponding transform is set as DCT2.

42. The encoder according to any one of claims 34 to 41, wherein in case the sequence level

DCT2 enabled flag is equal to 1 specifies that the DCT2 transform core is used for transformation, only, both the sub block transform as well as Multiple Transform Selection (MTS) transform are inferred as off.

- 5 43. The encoder according to any one of claims 34 to 40,
 wherein the sequence level DCT2 enabled flag being equal to 0 specifies that other transform cores than DCT2 are used for the transformation.
- 10 44. The encoder according to claim 43,
 wherein the inferring unit is configured to infer using a Discrete Sine Transform type 7 (DST7) and/or a Discrete Cosine Transform type 8 (DCT8) for transformation.
- 15 45. The encoder according to claim 43 or 44, wherein the sequence level DCT2 enabled flag being equal to 0
 specifies that it is inferred using DST7/DCT8 for transformation, only.
- 20 46. The encoder according to any one of claims 43 to 45,
 wherein in case the sequence level DCT2 enabled flag being equal to 0, it is determined whether Multiple Transform Selection for Sequence Parameter Set is enabled via a flag.
- 25 47. The encoder according to claim 46,
 wherein in case the sps_mts_intra_enabled_flag is present,
 in case the sps_mts_intra_enabled_flag is equal to 1 it is specified that a Transform Unit, TU, Multiple Transform Selection, MTS flag, denote tu_mts_flag, is present in the residual coding syntax for intra coding units;
 in case the sps_mts_intra_enabled_flag is equal to 0 it is specified that a tu_mts_flag is not present in the residual coding syntax for intra coding units;
 wherein in case the sps_mts_intra_enabled_flag is not present, the sps_mts_intra_enabled_flag is inferred to be 0.
- 30 48. A decoder, comprising:
 one or more processors; and
 a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when executed by

the processors, configures the decoder to carry out the method according to any one of claims 1 to 15.

49. An encoder, comprising:

- 5 one or more processors; and
 a non-transitory computer-readable storage medium coupled to the processors and storing programming for execution by the processors, wherein the programming, when executed by the processors, configures the encoder to carry out the method according to any one of claims 1 to 15.

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50. A computer-readable non-transitory medium storing a program, including instructions which when executed on a processor cause the processor to perform the method according to any of claims 1 to 15.

- 15 51. A non-transitory storage medium comprising a bitstream encoded by the encoder of claim 49.