

LATERAL HIGH VOLTAGE TRANSISTOR

ABSTRACT

A device and a method for forming a device are disclosed. The device includes a substrate with a high voltage (HV) device region. The HV device region is defined with first and second device isolation regions and an internal dielectric region which are shallow trench isolation (STI) regions. A HV transistor is disposed in the HV device region. The HV transistor includes a gate dielectric layer on the substrate, a gate disposed on the gate dielectric layer, and a source region disposed in the substrate adjacent to the gate and first device isolation region while a drain region disposed in the substrate adjacent to the second device isolation region. A drift well and a body well are disposed in the substrate. At least one buried RESURF region is disposed under the internal dielectric region.

Fig. 1a