PACKAGED INTEGRATED CIRCUIT DEVICES WITH THROUGH-BODY CONDUCTIVE VIAS, AND METHODS OF MAKING SAME

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

This subject matter disclosed herein is generally directed to the field of packaging integrated circuit devices, and, more particularly, to packaged integrated circuit devices with through-body conductive vias and various methods of making same.

2. DESCRIPTION OF THE RELATED ART

Integrated circuit technology uses electrical devices, *e.g.*, transistors, resistors, capacitors, etc., to formulate vast arrays of functional circuits. The complexity of these circuits requires the use of an ever-increasing number of linked electrical devices so that the circuit may perform its intended function. As the number of transistors increases, the integrated circuitry dimensions shrink. One challenge in the semiconductor industry is to develop improved methods for electrically connecting and packaging circuit devices which are fabricated on the same and/or on different wafers or chips. In general, it is desirable in the semiconductor industry to construct transistors which occupy less surface area on the silicon chip/die.

In the manufacture of semiconductor device assemblies, a single semiconductor die is most commonly incorporated into each sealed package. Many different package styles are used, including dual inline packages (DIP), zig-zag inline packages (ZIP), small outline J-bends (SOJ), thin small outline packages (TSOP), plastic leaded chip carriers (PLCC), small outline integrated circuits (SOIC), plastic quad flat packs (PQFP) and interdigitated leadframe (IDF). Some semiconductor device assemblies are connected to a substrate, such as a circuit board, prior to encapsulation. Manufacturers are under constant pressure to reduce the size of the packaged integrated circuit device and to increase the packaging density in packaging integrated circuit devices.

In some cases, packaged integrated circuit devices have been stacked on top of one another in an effort to conserve plot space. Prior art techniques for conductively coupling the stacked packaged integrated circuit devices to one another typically involved the formation of solder balls or wire bonds to establish this connection. What is desired is a new and improved technique for conductively coupling stacked packaged integrated circuit devices to one another.

BRIEF DESCRIPTION OF THE DRAWINGS

The present subject matter may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

Figure 1 is a schematic depiction of an illustrative packaged integrated circuit die with a plurality of conductive through-body vias as described herein;

Figure 2 is a schematic depiction of an illustrative packaged integrated circuit comprised of multiple die with a plurality of conductive through-body vias as described herein;

Figure 3 is a schematic cross-sectional view of an illustrative stacked packaged device disclosed herein;

Figure 4 is a schematic cross-sectional view of another illustrative stacked packaged device disclosed herein;

Figure 5 is a schematic cross-sectional view of yet another illustrative stacked packaged device disclosed herein;

Figures 6A-6H schematically depict one illustrative method of forming the stacked packaged devices disclosed herein; and

Figures 7A-7I schematically depict another illustrative method of forming the stacked packaged devices disclosed herein.

While the subject matter disclosed herein is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications,

equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the present subject matter are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

Although various regions and structures shown in the drawings are depicted as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features and doped regions depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the subject matter disclosed herein.

Figure 1 depicts one illustrative embodiment of a packaged integrated circuit device 100 as described herein. The packaged integrated circuit device 100 comprises an integrated circuit die 12 having a plurality of bond pads 14, conductive wiring lines 16 (sometimes referred to as a redistribution layer (RDL)), and at least one conductive interconnection 18 (sometimes referred to as conductive vias) that extend through a body 20 of encapsulant material, *e.g.*, mold compound material. The conductive via 18 defines a conductive flow path through the thickness of the body 20, *i.e.*, between the front 13 and back 15 of the body 20. The conductive via 18 and the integrated circuit die 12 may be conductively coupled to one another using a variety of known techniques and structures. In the depicted example, the conductive wiring line 16 conductively couples the conductive via 18 to the integrated circuit die 12. A plurality of schematically depicted solder balls 24 are formed on the packaged integrated circuit device 100 in accordance with known processing techniques. The solder balls 24, or other like connections, may be employed to conductively couple the packaged integrated circuit device 100 to another

structure, *e.g.*, a printed circuit board. In Figure 1, the die 12 is embedded in the body of encapsulant material 20. As used herein, when it is stated that one or more die 12 are embedded in a body of encapsulant material, it is to be understood that only portions of the body of the die 12 need to be positioned in the encapsulant material. It is not required that the encapsulant material surround all sides of the body of the die 12, although that configuration may be employed if needed depending upon the particular application.

Figure 2 depicts one illustrative embodiment of a packaged integrated circuit device 200 as described herein. The packaged integrated circuit device 200 comprises a plurality of integrated circuit die 12 (two are shown) embedded in a single body 20 of encapsulant material, *e.g.*, mold compound material. In the illustrative example depicted herein, each of the die 12 have the same physical size. However, as will be understood by those skilled in the art after a complete reading of the present application, the die 12 are not required to be the same physical size, nor do they have to perform the same function. Each of the die 12 shown in Figure 2 have a plurality of bond pads 14, conductive wiring lines 16 (sometimes referred to as a redistribution layer (RDL)), and at least one conductive interconnection 18 (sometimes referred to as conductive vias) that extend through the body 20 of encapsulant material. Since the device 200 comprises a plurality of integrated circuit die 12, it may be considered to be a multi-chip module (MCM). As in Figure 1, a plurality of schematically depicted solder balls 24 are formed on the packaged integrated circuit device 200 in accordance with known processing techniques. The solder balls 24, or other like connections, may be employed to conductively couple the packaged integrated circuit device 200 to another structure, *e.g.*, a printed circuit board.

In the depicted embodiment, each of the conductive vias 18 in Figure 2 extend through the thickness of the body 12. The conductive coupling between and among the conductive vias 18 and the embedded integrated circuit die 12 may b established using any of a variety of known techniques and structures. In the example shown in Figure 2, at least one of the conductive vias 18 is conductively coupled to one of the integrated circuit die 12 by one or more wiring lines 16, while another of the conductive vias 18 is conductively coupled to the other integrated circuit die 12 by one or more wiring lines 16 as well.

As will be recognized by those skilled in the art after a complete reading of the present application, the methods and techniques disclosed herein may be applied to virtually any type of integrated circuit device that may be formed on the die 12. Additionally, the configuration and

location of the schematically depicted bond pads 14, the conductive wiring lines 16, and the through-body conductive interconnections 18 may vary depending upon the particular application.

Figures 3-5 are schematic cross-sectional views of a plurality of stacked and packaged integrated circuit devices. In the illustrative example depicted in Figure 3, the stacked package 300 comprises a plurality of individual embedded die 10A-10D. In the illustrative example depicted in Figure 3, only four illustrative individual embedded die 10A-10D are depicted. As set forth above, it is to be understood that in referring to an embedded die or an individual embedded die, the structure need only comprise at least one integrated circuit die with a portion of the die body positioned in the body 20 of encapsulant material. However, as will be recognized by one skilled in the art after a complete reading of the present application, the number of individual embedded die 10 in the stacked package 300 may vary depending upon the particular application, *i.e.*, the number of individual embedded die 10 within such a stack 300 may be more or less than the illustrative four depicted in Figure 3.

Each of the illustrative individual embedded die 10A-10D in Figure 3 comprise an integrated circuit die 12, a plurality of bond pads 14, conductive wiring lines 16 (sometimes referred to as a redistribution layer (RDL)), a plurality of conductive interconnections 18 (sometimes referred to as conductive vias) that extend through the body 20 of encapsulated material. A plurality of conductive structures 22 are provided between adjacent individual embedded die 10 to provide an electrically conductive path between the various embedded die 10A-10D. A plurality of schematically depicted solder balls 24 are formed on the packaged die 10D in accordance with known processing techniques. The solder balls 24, or other like connections, may be employed to conductively couple the stacked package 300 to another structure, *e.g.*, a printed circuit board.

As will be recognized by those skilled in the art after a complete reading of the present application, the methods and techniques disclosed herein may be applied to virtually any type of integrated circuit device that may be formed on the die 12 and packaged in a stacked configuration. Additionally, the configuration and location of the schematically depicted bond pads 14, conductive interconnections 18 and conductive structures 22 shown in Figure 3 may vary depending upon the particular application. In the embodiment depicted in Figure 3, all of

the packaged die are oriented with the front side 13 of the embedded die 10 facing a backside 15 of an adjacent embedded die 10.

Figure 4 depicts another illustrative embodiment of a stacked packaged device 400. Similar to the embodiment shown in Figure 3, the embodiment in Figure 4 comprises four illustrative individual embedded die 10A-10D. In Figure 4, the individual embedded die 10A-10D are assembled as groups 10E and 10F prior to assembling these groups into the structure shown in Figure 4. The first group 10E comprises the individual embedded die 10A and 10B, while the second group 10F comprises the individual embedded die 10C and 10D. A plurality of conductive interconnections or vias 32 extend through the bodies 20 of the plurality of die 10 that comprise the first group 10E, while a plurality of conductive interconnections or vias 34 extend through the bodies 20 of the plurality of the die 10 that comprise the second group 10F.

A plurality of conductive structures 22 provide an electrically conductive path between the two groups 10E and 10F. The individual embedded die 10 within each group may be secured to one another using an adhesive material 28. Note that, in the illustrative example depicted in Figure 4, the backside 15 of adjacent embedded die 10 are positioned facing one another. As will be recognized by those skilled in the art after a complete reading of the present application, the number of groups, *e.g.*, groups 10E and 10F, that may be stacked as depicted in Figure 4 may vary depending upon the particular application, *i.e.*, more or less than the illustrative two groups depicted in Figure 4 may be assembled into the final stacked package 400. Similarly, the number of individually embedded die 10 within each group may be greater than the illustrative two depicted in the groups 10e and 10F in Figure 4.

The structures depicted in Figures 3 and 4 may be combined if desired. For example, Figure 5 depicts an illustrative stacked packaged device 500 wherein the bottom two embedded die 10A-10B are packaged as a group 10E, while the upper two embedded die 10C-10D are packaged as depicted in Figure 3. Thus, it is readily apparent that the methodologies and devices disclosed herein provide great flexibility as it relates to creating stacked packaged devices to thereby reduce plot space consumption and improve packaging densities. Moreover, in Figures 3-5, each of the individual embedded die 10 are depicted as having a single integrated circuit die 12 embedded therein. In accordance with one aspect of the present disclosure, the individual embedded die 10 may comprise a plurality of individual integrated circuit die 12, like the multi-chip embodiment depicted in Figure 2. That is, the methods and devices disclosed herein may

be employed with individual embedded die 10 that comprise single or multiple integrated circuit die 12. For ease of reference, the following description will make reference to an individual embedded die 10 comprised of a single integrated circuit die 12, although the methods may readily be applied to embedding a plurality of integrated circuit die 12 in a single body 20 of encapsulant material of an individual embedded die.

Figures 6A-6H depict one illustrative method of forming the devices disclosed herein. In Figure 6A, a plurality of known good integrated circuit die 12 are placed front side 13 down above an illustrative sacrificial structure 30. In one illustrative example, the sacrificial structure 30 may be a film frame with dicing tape positioned across the film frame. The structure 30 is sacrificial in the sense that it will later be removed. In Figure 6B, a body 20 of encapsulant material, *e.g.*, mold compound, is formed around the integrated circuit die 12 and above the structure 30, *i.e.*, the integrated circuit die 12 is embedded in the body 20. Traditional molding techniques, *e.g.*, injection molding, may be performed to form the body 20 of encapsulant material. Thereafter, as shown in Figure 6C, the sacrificial structure 30 may be removed. In the illustrative example described herein, the structure 30 may simply be peeled away due to the use of the adhesive tape as part of the structure 30.

Next, as shown in Figure 6D, the conductive lines 16 are formed above the front side 13 of the integrated circuit die 12 and body 12 in accordance with traditional techniques. Of course, the conductive lines 16 may have any desired configuration and they may be made from any desired material. Then, as indicated in Figure 6E, a plurality of openings or vias 17 are formed through the body 20 as indicated. The openings 17 may be formed by a variety of known techniques, *e.g.*, laser drilling, etching etc. In some applications, a masking layer (not shown) may be formed as part of the process of forming the openings 17. The openings 17 may be of any desired shape or configuration. Note that, in the illustrative example depicted herein, the openings 17 are formed from the backside 15 toward the front side 13 of the body 20 of the embedded die 10. Also note that, in this particular example, the openings 17 expose, but do not extend through, the conductive interconnections 16 formed on the front side 13 of the embedded die 10. Thereafter, as shown Figure 6F, the openings 17 are filled with a conductive material, *e.g.*, copper, aluminum, silver, etc., to form the conductive interconnections 18. The conductive material may be formed in the openings 17 using any of a variety of known techniques, *e.g.*, plating, deposition, etc., and a variety of different conductive materials may be employed, depending upon the particular application.

In Figure 6G, a plurality of conductive structures 22 are formed on the embedded die 10A-10B using known techniques. In some cases, the conductive structures 22 may be formed as part of the process of forming the conductive interconnections 18. Then, as shown in Figure 6H, a dicing or singulating process is performed along cut line 37 to produce the illustrative individual embedded die 10A and 10B.

Next, the individual embedded die 10A-10B are subject to a variety of tests to confirm their acceptability for their intended application. Once the embedded die 10A-10B have successfully passed such tests, they are ready to be shipped to customers. In other applications, the tested embedded die 10A-10B may be assembled into a stacked packaged device 300, 400, 500 as depicted herein. In the example depicted in Figure 3, a plurality of individual embedded die 10 are positioned as depicted in Figure 3 and a reflow process is performed to establish the electrical connection between the conductive structures 22 on an individual embedded die, *e.g.*, die 10A, and the conductive interconnections 18 on an adjacent embedded die, *e.g.*, die 10B. The illustrative solder balls 24 may be formed on the illustrative die 10 using traditional techniques. The solder balls 24 may be formed at any desired point during the process flow. For example, the solder balls 24 may be formed after all of the embedded die 10A-10D are assembled as depicted in Figure 3. Alternatively, the solder balls 24 may be formed above the individual embedded die 10D prior to assembling the individual embedded die 10D with the other individual embedded die as depicted in Figure 3.

Figures 7A-7I depict another illustrative method of forming the devices disclosed herein. The steps depicted in Figures 7A-7D are the same as those previously described with respect to Figures 6A-6D. Thus, a detailed discussion of Figures 7A-7D will not be repeated. In Figure 7E, a plurality of the structures depicted in Figure 7D are secured to one another using an adhesive material 28. Thereafter, in Figure 7F, a plurality of openings or vias 31 are formed through the bodies 20 of the combined structure depicted in Figure 7E. The openings 31 may be formed by a variety of known techniques, *e.g.*, laser drilling, etching etc. In some applications, a masking layer (not shown) may be formed as part of the process of forming the openings 31. The openings 31 may be of any desired shape or configuration. Note that, in the illustrative example depicted herein, the openings 31 extend through the conductive interconnections 16 formed on the front side 13 of each of the individual structures. Thereafter, as shown Figure 7G, the openings 31 are filled with a conductive material, *e.g.*, copper, aluminum, silver, etc., to form the through body conductive vias 32. The conductive material may be formed in the openings

31 using any of a variety of known techniques, *e.g.*, plating, deposition, etc., and a variety of different conductive materials may be employed, depending upon the particular application.

In Figure 7H, a plurality of conductive structures 22 are formed on the structure depicted in Figure 7G using known techniques. In some cases, the conductive structures 22 may be formed as part of the process of forming the conductive interconnections 32. Next, as shown in Figure 7I, a dicing or singulating process is performed along cut line 37 to produce the illustrative groups 10E and 10F of the individual embedded die.

Next, the groups of embedded die 10E-10F are subject to a variety of tests to confirm their acceptability for their intended application. Once the groups 10E-10F have successfully passed such tests, they are ready to be shipped to a customer. In some applications, the groups of embedded die 10E-10F may be assembled into a stacked packaged device as described herein. In the example depicted in Figure 4, the groups of embedded die 10E and 10F are positioned as depicted in Figure 4 and a reflow process is performed to establish the electrical connection between the conductive structures 22 on the first group 10E and the conductive vias 32 on an adjacent group 10F. The illustrative solder balls 24 may be formed on an illustrative individual embedded die in the group 10F using traditional techniques. The solder balls 24 may be formed at any desired point during the process flow. For example, the solder balls 24 may be formed after the two illustrative groups 10E-10F are assembled as depicted in Figure 4. Alternatively, the solder balls 24 may be formed above one of the individual embedded die in the group 10F prior to assembling the two groups together as depicted in Figure 4.

As will be recognized by those skilled in the art after a complete reading of the present application, the present disclosure may provide very efficient means for packaging individual die and providing stacked packaged integrated circuit devices. Much of the processing performed herein may be performed on multiple die at a single time as opposed to performing such operations on individual die one at a time. For example, although two illustrative die 12 are depicted in Figures 6A-6H and 7A-7I, the processing steps described herein may be performed on any desired number of die, depending upon the processing capability of the processing tools employed. In short, wafer level processing techniques may be employed to increase the efficiency of packaging operations, *i.e.*, the processing operations may be performed on multiple die at the same time.

CLAIMS

What is claimed:

1. A device, comprising:

a first subassembly and a second subassembly individually having a front side and a back side, the back sides of the first and second subassemblies facing each other, the first and second subassemblies individually having:

an encapsulant material;

a semiconductor die embedded in the encapsulant material, the semiconductor die having an active surface generally flush with the front side of the first or second subassembly and a back surface embedded in the encapsulant material;

a conductive line on the front side of the individual first and second subassemblies and on the active surface of the semiconductor die;

an adhesive material between and in direct contact with the encapsulant material at the back sides of the first and second subassemblies; and

a conductive via that extends from the front side of the first subassembly, through the adhesive material, to the front side of the second subassembly, the conductive via being in direct contact with the conductive lines of both the first and second subassemblies.

2. The device of claim 1, wherein the conductive via extends between the conductive lines of the first and second subassemblies.

3. The device of claim 1, wherein the first and second subassemblies are stacked vertically above one another.

4. The device of claim 1, wherein the active surface of the semiconductor die in the first subassembly faces away from the active surface of the semiconductor die in the second subassembly.

5. The device of claim 1, wherein each of the first and second subassemblies comprises a single integrated circuit die.

6. The device of claim 1, wherein each of the first and second subassemblies comprises a plurality of integrated circuit die.

7. The device of claim 1, wherein the back surface of the semiconductor die in the first subassembly is spaced apart from the adhesive material between the first and second subassemblies.

8. A semiconductor device package, comprising:

a first semiconductor structure;

a second semiconductor structure proximate to the first semiconductor structure;

a conductive structure between and in direct contact with both the first and second semiconductor structure;

wherein the individual first and second semiconductor structure include:

a first subassembly and a second subassembly individually having a front side and a back side, the back sides of the first and second subassemblies facing each other, the first and second subassemblies individually having:

an encapsulant material;

a semiconductor die embedded in the encapsulant material, the semiconductor die having an active surface generally flush with the front side of the first or second subassembly and a back surface embedded in the encapsulant material;

a conductive line on the front side of the individual first and second subassemblies and on the active surface of the semiconductor die;

an adhesive material between and in direct contact with the encapsulant material at the back sides of the first and second subassemblies; and

a conductive via that extends from the front side of the first subassembly, through the adhesive material, to the front side of the second subassembly, the conductive via being in direct contact with the conductive lines of both the first and second subassemblies.

9. The semiconductor device package of claim 8, wherein the conductive structure is between and in direct contact with (1) the conductive line of the second subassembly of the first semiconductor structure and (2) the conductive line of the first subassembly of the second semiconductor structure.

10. The semiconductor device package of claim 8, wherein the conductive structure is between and in direct contact with (1) the conductive line of the second subassembly of the first semiconductor structure and (2) the conductive line of the first subassembly of the second semiconductor structure, and wherein the semiconductor device package further includes a solder ball attached to the conductive line of the first subassembly of the first semiconductor structure.

11. The semiconductor device package of claim 8, wherein the conductive vias individually extend between the conductive line of the first subassembly and the conductive line of the second subassembly in both the first and second semiconductor structures.

12. The semiconductor device package of claim 8, wherein the active surface of the semiconductor die in the first subassembly faces away from the active surface of the semiconductor die in the second subassembly in both the first and second semiconductor structures.

13. The semiconductor device package of claim 8, wherein each of the first and second subassemblies comprises a single integrated circuit die in the individual first and second semiconductor structures.

14. The semiconductor device package of claim 8, wherein each of the first and second subassemblies comprises a plurality of integrated circuit die in the individual first and second semiconductor structures.

15. The semiconductor device package of claim 8, wherein the back surfaces of the semiconductor dies in the first and second subassemblies are individually spaced apart from the adhesive material in the individual first and second semiconductor structures.

16. A method of manufacturing a semiconductor device, comprising:

encapsulating a first semiconductor die with a first encapsulant into a first subassembly having a first front side and a first back side, the first semiconductor die having a first active surface generally flush with the first front side and a first back surface embedded in the first encapsulant;

encapsulating a second semiconductor die with a second encapsulant into a second subassembly having a second front side and a second back side, the second semiconductor die having a second active surface generally flush with the second front side and a second back surface embedded in the second encapsulant;

attaching the first subassembly to the second subassembly with an adhesive material, the first and second back sides of the first and second subassemblies facing each other;

forming a conductive line on the individual first and second front sides of the individual first and second subassemblies; and

forming a conductive via that extends from the first front side of the first subassembly, through the adhesive material, to the front side of the second subassembly, the conductive via being in direct contact with the conductive lines of both the first and second subassemblies.

17. The method of claim 16, wherein forming the conductive via includes forming an opening in the first encapsulant, the second encapsulant, and the adhesive material and filling the opening with a conductive material.

18. The method of claim 16, wherein encapsulating a first semiconductor die and encapsulating a second semiconductor die includes encapsulating both the first and second semiconductor dies with an encapsulant and singulating the encapsulated first and second semiconductor dies to form the first and second subassemblies.

19. The method of claim 16, wherein:

the method further includes placing the first and second semiconductor dies on a sacrificial structure with the first and second active surfaces in direct contact with the sacrificial structure;

encapsulating a first semiconductor die and encapsulating a second semiconductor die includes encapsulating both the first and second semiconductor dies with an encapsulant while the first and second semiconductor dies are on the sacrificial structure;

thereafter, removing the sacrificial structure from the first and second semiconductor dies; and

singulating the encapsulated first and second semiconductor dies to form the first and second subassemblies.

20. The method of claim 16, wherein:

the method further includes placing the first and second semiconductor dies on a sacrificial structure with the first and second active surfaces in direct contact with the sacrificial structure, the sacrificial structure including at least one of a film frame and a dicing tape;

encapsulating a first semiconductor die and encapsulating a second semiconductor die includes encapsulating both the first and second semiconductor dies with an encapsulant while the first and second semiconductor dies are on the sacrificial structure;

thereafter, removing the sacrificial structure from the first and second semiconductor dies; and

singulating the encapsulated first and second semiconductor dies to form the first and second subassemblies.

21. The method of claim 16, wherein:

the method further includes placing the first and second semiconductor dies on a sacrificial structure with the first and second active surfaces in direct contact with the sacrificial structure;

encapsulating a first semiconductor die and encapsulating a second semiconductor die includes encapsulating both the first and second semiconductor dies with an encapsulant while the first and second semiconductor dies are on the sacrificial structure;

thereafter, removing the sacrificial structure from the first and second semiconductor dies;

singulating the encapsulated first and second semiconductor dies to form the first and second subassemblies; and

forming the conductive via includes forming an opening in the first encapsulant, the second encapsulant, and the adhesive material and filling the opening with a conductive material.