semiconductor and silicon-dioxide layers 23, 22 to be controlled with precision.

SUMMARY

The present disclosure aims to completely or partially remedy the aforementioned drawbacks, and relates to a process for fabricating a plurality of semiconductor-on-insulator structures, said insulator being a layer of silicon dioxide of thickness smaller than 50 nm, said structures comprising a semiconductor layer placed on the silicon-dioxide layer, said process comprising a step of heat treating the plurality of structures, which heat treatment step is designed to partially dissolve the silicon-dioxide layer, said process being noteworthy in that the pressure of the non-oxidising atmosphere is lower than 0.1 bar.

In one aspect, there is provided a fabrication process for fabricating a plurality of semiconductor-on-insulator structures, comprising: providing a plurality of semiconductor-on-insulator structures each including a carrier substrate, a semiconductor layer, and an insulator layer between the carrier substrate and the semiconductor layer, the insulator being a layer of silicon dioxide having a thickness smaller than 50 nm; and after providing the plurality of semiconductor-on-insulator structures, heat treating the plurality of semiconductor-on-insulator structures and partially dissolving the silicon dioxide layer of each of the semiconductor-on-insulator structures in a non-oxidizing atmosphere so as to reduce the thickness of the silicon dioxide layer of each of the semiconductor-on-insulator structures, wherein a pressure of the non-oxidizing atmosphere is lower than 0.1 bar.

The structures intended to be heat-treated are placed in an oven containing a plurality of structures, so that one side of each structure faces a side of another structure.

Thus, during the heat treatment, the silicon-dioxide layer partially dissolves, part of the semiconductor layer is consumed, and a semiconductor monoxide is released. In the case of a semiconductor layer made of silicon, silicon monoxide is released during the heat treatment.

Furthermore, the rate at which the silicon-dioxide layer dissolves depends on the concentration of semiconductor monoxide in the vicinity of the free surface of the semiconductor layer.

The Applicant has observed that the arrangement of the structures in the oven generates a nonuniform semiconductor-monoxide concentration in the oven. Said concentration is higher at the centre of the free surface of a semiconductor layer than at its edge. The dissolution reaction is then slower at the centre of the structure than at its edge. The nonuniformity in the semiconductor-monoxide concentration in turn leads to nonuniformity in the thickness of the silicon-dioxide layer and in the thickness of the semiconductor layer.

CLAIMS

1. A fabrication process for fabricating a plurality of semiconductor-on-insulator structures, comprising:

providing a plurality of semiconductor-on-insulator structures each including a carrier substrate, a semiconductor layer, and an insulator layer between the carrier substrate and the semiconductor layer, the insulator being a layer of silicon dioxide having a thickness smaller than 50 nm; and

after providing the plurality of semiconductor-on-insulator structures, heat treating the plurality of semiconductor-on-insulator structures and partially dissolving the silicon dioxide layer of each of the semiconductor-on-insulator structures in a non-oxidizing atmosphere so as to reduce the thickness of the silicon dioxide layer of each of the semiconductor-on-insulator structures, wherein a pressure of the non-oxidizing atmosphere is lower than 0.1 bar.

2. The fabrication process according to Claim 1, wherein the non-oxidizing atmosphere is an inert atmosphere.

3. The fabrication process according to Claim 2, wherein the non-oxidizing atmosphere contains argon and/or nitrogen.

4. The fabrication process according to Claim 3, wherein the non-oxidizing atmosphere is controlled so that it contains less than 1 ppm oxygen.

5. The fabrication process according to Claim 4, wherein the pressure of the non-oxidizing atmosphere is higher than 0.01 bar.

6. The fabrication process according to Claim 5, wherein the semiconductor layer of each of the semiconductor-on-insulator structures has a thickness greater than 230 nm prior to heat treating the plurality of semiconductor-on-insulator structures.

7. The fabrication process according to Claim 6, wherein the semiconductor layer of each of the semiconductor-on-insulator structures is made of silicon.

8. The fabrication process according to Claim 7, wherein the heat treating of the plurality of semiconductor-on-insulator structures is carried out at a temperature between 900°C and 1350°C.

9. The fabrication process according to Claim 8, wherein the heat treating of the plurality of semiconductor-on-insulator structures is carried out for a time between 10 minutes and 8 hours.

10. The fabrication process according to Claim 9, wherein the thickness of the silicon dioxide layer of each of the semiconductor-on-insulator structures is smaller than 25 nm prior to heat treating the plurality of semiconductor-on-insulator structures.

11. The fabrication process according to Claim 10, wherein the thickness of the silicon dioxide layer of each of the semiconductor-on-insulator structures is smaller than 15 nm prior to heat treating the plurality of semiconductor-on-insulator structures.

12. The fabrication process according to Claim 1, wherein the non-oxidizing atmosphere is controlled so that it contains less than 1 ppm oxygen.

13. The fabrication process according to Claim 1, wherein the pressure of the non-oxidizing atmosphere is higher than 0.01 bar.

14. The fabrication process according to Claim 1, wherein the semiconductor layer of each of the semiconductor-on-insulator structures has a thickness greater than 230 nm prior to heat treating the plurality of semiconductor-on-insulator structures.

15. The fabrication process according to Claim 14, wherein the semiconductor layer of each of the semiconductor-on-insulator structures has a thickness greater than 250 nm prior to heat treating the plurality of semiconductor-on-insulator structures.

16. The fabrication process according to Claim 15, wherein the semiconductor layer of each of the semiconductor-on-insulator structures has a thickness greater than 280 nm prior to heat treating the plurality of semiconductor-on-insulator structures.

17. The fabrication process according to Claim 1, wherein the semiconductor layer of each of the semiconductor-on-insulator structures is made of silicon.

18. The fabrication process according to Claim 1, wherein the heat treating of the plurality of semiconductor-on-insulator structures is carried out at a temperature between 900°C and 1350°C.

19. The fabrication process according to Claim 1, wherein the heat treating of the plurality of semiconductor-on-insulator structures is carried out for a time between 10 minutes and 8 hours.

20. The fabrication process according to Claim 1, further comprising controlling the thickness of the silicon dioxide layer of each of the semiconductor-on-insulator structures to within less than +/- 1 Å and a non-uniformity smaller than 2 Å.