ASSEMBLY OF AN OPTO-ELECTRONIC ENGINE

DESCRIPTION OF THE INVENTION:

Technical Field of the Invention

[0001] The present invention relates to hardware design in communication and computing technology domain. More specifically, the invention relates to assembly of an opto-electronic engine.

Background of the Invention

[0002] Eventually, when the system has ability to process significant load of data, the system needs to be provided with adequate data at a required rate. In traditional systems, number of instructions executed by the processor will be proportional to the rate at which data is received. In such cases, scheduling algorithms associated with operating systems will be able to enable effective resource utilization. The resource utilization of a processing system is impaired when the system has a higher capacity to execute the instructions, but the instructions to be executed are fetched at a lower speed due to the limitations imposed by the connections. Hence, there is a need for a communication system which is designed for high performance computing applications. For efficient enablement of the system there is a need for utilizing multiple technologies along with packaging methodologies. Further, to supplement the systems which are designed for high performance computing applications, there is a need for developing a high data rate communication mechanism both for inter-system communication and intra-system communication.

Object of the invention

[0003] The principal object of the invention is to achieve improved processing power for existing processor chips by integrating high data rate transmission/reception opto-electronic engine and high bandwidth memory with processing system efficiently through free space/ optical fibre in a single package.

[0004] Another object of the invention is to enable assembly of an opto-electronic engine using multiple layers of assembly to achieve functional integration. The advantages of separating the assembly into layers are (i) optimizing analog, digital, sensing, optical sections independently (ii) incorporating multiple technologies for materials (iii) improving the product yield (iv) testing each layer separately ensuring functionality and (v) ability to replace dysfunctional layer without affecting the total product.

[0005] These and other objects and characteristics of the present invention will become apparent from the further disclosure to be made in the detailed description given below.

Summary of the invention

[0006] To the enablement of the present disclosure and related ends, the at least one aspect comprises the feature(s) hereinafter completely described and particularly and/or specifically pointed out in the specification at the section of claims. The following drawings and description set forth in detail enable certain exemplary features of the at least one aspect(s). Described features are indicative, however, of but a few of the many ways in which the following principles of various aspects may be employed, and this description is intended to include all such aspects and their equivalents.

[0007] It is a known fact that the shortest interconnect is a vertical connection. However, there are many challenges to be solved for vertical integration of systems. In the present disclosure, the problem associated with single layer assembly is solved by using a multi-

layer assembly. First layer comprises a FPGA/CPU/GPU and optics on a high accuracy substrate to enable optical alignment.. Second layer comprises an interposer or a substrate that can dissipate the high amount of heat generated by the digital circuits and the third layer comprises low cost organic analog interposer.

[0008] This summary provided herein is to introduce a section of concepts in a simple and clear form which are further described in the Detailed Description. This summary provided herein is not intended to particularly identify key features or essential features of the claimed invention or subject matter, nor is it intended to be used as a support or as an aid in determining the scope of the claimed subject matter.

[0009] The above summary is descriptive and exemplary only and is not intended to be in any way restricting. In addition to the descriptive aspects, embodiments, and features described in the above summary, further features and embodiments will become apparent by reference to the accompanied drawings and the following detailed description.

Brief Description of Drawings

[0010] The foregoing and any other features of embodiments will become more evident from the following detailed description of embodiments when read along with the associated drawings. In the drawings, like elements refer to like reference numerals.

[0011] In the following description, a number of specific details are put forward in order to enable a thorough comprehension of various embodiments of the invention. However, it is evident to one skilled in the art that the embodiments of the invention may be put to practice with an equivalent arrangement or without using these specific details. In other examples, in order to avoid unnecessary obscuring of the embodiments of the invention, devices, and well-known structures are clearly shown in the form of a block diagram.

[0012] FIG. 1 illustrates a generic block diagram of an opto-electronic engine, according to one embodiment of the invention.

[0013] FIG. 2 illustrates a first layer of the opto-electronic engine, according to one embodiment of the invention.

[0014] FIG.3 illustrates a second layer of the opto-electronic engine, according to one embodiment of the invention.

[0015] FIG.4 illustrates a third layer of the opto-electronic engine, according to one embodiment of the invention.

[0016] FIG. 5 assembly of the opto-electronic engine, according to one embodiment of the invention.

[0017] FIGs. 6A-6B assembly of the opto-electronic engine with a micron memory, according to one embodiment of the invention.

Detailed Description of the Invention

[0018] Reference to the description of the present subject will be made in detail, out of which one or more examples are shown in figures. Each one of the examples may be given to elaborate the subject matter and not serve as a limitation. Various modifications, alterations, and changes that are obvious to a person skilled in the art to which the invention relates to are deemed to be within the scope, contemplation, and spirit of the invention.

[0019] The word “exemplary” will be used in this document to mean “illustration, instance or serving as an example”. Any detail described herein in the description as “exemplary” is not necessarily defined as preferred or advantageous over other aspects.

[0020] In this invention, the term “application” may also include executable content files namely: markup language files, object code, patches, byte code, and scripts. Additionally, an “application” referred to in this subject matter may also include non executable files in nature, for instance, data files that may need to be opened or other documents that may need to be accessed.

[0021] In this description, the terms “module”, “unit”, “component”, “system” and “database” and other similar things are aimed to refer to any kind of computer-related entity, which may include either software, hardware, firmware in execution or a combination of hardware and software. A component may either be an application running on a computing device or the computing device itself. For instance, a component may be including but not limited to being, an object, a processor, a process running on a processor, a thread of execution, an executable, a computer, and/or a program. A component may be contained on either one computer and/or distributed within two or more computers. One or more components may be located within a thread of execution and/or within a process. There may be communication between these components through local and/or remote processes associated with any signal having at least one data packets (e.g., the data may interact between two different components in a distributed system, local system, and/or across a vast network such as the Internet). Furthermore, these components may be executed via numerous computer-readable media that have various data structures stored.

[0022] In this invention, the words “wireless handset”, “wireless communication device”, “wireless device”, “communication device”, and “the wireless telephone” may be used interchangeably. A variety of wireless capabilities associated with a number of portable computing devices are enabled with greater bandwidth availability after the emergence of the third generation (“3G”) and fourth-generation (“4G”) technology. Hence, a portable

computing device may comprise a smart phone, a hand-held device with a wireless connection, a cellular telephone, a PDA, a navigation device, or a pager.

[0023] As used in the application, the words ‘circuit’ or ‘circuitry’ refers to one or more of the following: (a) circuits such as microprocessor(s) or a part of a microprocessor(s), that may require firmware or software for its operation, which may not require the firmware or software to be present physically and (b) hardware-only circuit implementations (like implementations in digital and/or analog circuit) and (c) a combination of firmware (and/or software) and circuits, namely:(i) a part of software/processor(s) (including memory(ies) and software that work together to cause a device, such as a server or a mobile phone, to perform several operations) or (ii) a combination of one or more processor(s).

[0024] The definition of ‘circuitry’ may be applicable to all the uses of this term throughout the application, including the claims. The term ‘circuitry’ may also include, for instance and if applicable to a specific claim element, specific integrated circuits such as one for a mobile phone, or a baseband integrated circuit or any similar server based integrated circuit, any network device or a cellular network device. Furthermore, the term ‘circuitry’ as used in this application may also cover an implementation of a part of a microprocessor, a processor (or multiple processors) and its (or their) accompanying firmware and/or software.

[0025] In this application, the term “content” may include files that have executable content, namely: byte code, patches, object code, markup language files and scripts. Additionally, “content” referred to herein, may also cover files that are not executable in nature, like the documents that require data files that need to be accessed or documents that may need to be opened.

[0026] FIG. 1 illustrates a generic block diagram of an opto-electronic engine, according to one embodiment of the invention. The opto-electronic engine comprises three layers.

A first layer (101), a second layer (103) and a third layer (105). The first layer (101) and second layer (103) are connected by solder bumps (107) and the second layer (103) and the third layer (105) are connected by an edge connector (109). FIGs. 2-4 explain elements associated with each of the layers.

[0027] FIG 2 represents a first layer (101) of the optoelectronic engine (100), according to one embodiment of the invention. In some example embodiments, a FPGA 203 may be placed on a LTCC, Silicon interposer or a glass interposer 209. Further, a heat sink 201 may be placed on the FPGA 203. A transmitter 205 and a receiver 207 may be placed on the LTCC 209. In some example embodiements, the FPGA 203 drives the transmitter 205 and the receiver 207. The transmitter 205,the receiver 207 and the FPGA 203 may be placed on the LTCC using a plurality of solder bumps for achiving high accurary alignment. The transmitter 205 and the receiver 207 may be optical in nature. In some example embodiment, LTCC 209 may be replaced by a glass interposer having less layers compared to LTCC 209.

[0028] FIG. 3 illustrate a second layer (103) of the opto-electronic engine. The second layer comprises a silicon, organic or a glass layer connected to a memory 301, a processor 303, a communication interface 305 and a testing interface 307. The silicon, organic or a glass layer that may dissipate the high amount of heat generated by the digital circuits such as the memory 301, the processor 303, the communication interface 305 and the testing interface 307. The processor 303 can be any processor, such as 32-bit processors using a flat address space, such as a Hitachi SH1, an Intel 960, an Intel 80386, a Motorola 68020 (or any other processors carrying similar or bigger addressing space). Processors other than the above mentioned, processors that may be built in the future, are also apt. The processor can include but is not limited to general processor, Application Specific Integrated Circuit (ASIC), Digital Signal Processing (DSP) chip,

AT89S52 microcontroller firmware or a combination, Field Programmable Gate Arrays (FPGAs) thereof.

[0029] Processors which are suitable for carrying out a computer program may include, by example, both special and general purpose microprocessors, or processors of any kind for digital computer. Generally, a processor obtains instructions and data through a read only memory card or a random-access memory (RAM) or both. The vital elements of a computer are its processor for carrying out instructions and multiple memory devices for hoarding data and instructions. Generally, a computer includes, or be operatively associated to transfer data to or receive data from, or both, multiple mass storage devices for hoarding data, e.g., magneto optical disks, magnetic, or optical disks. However, a computer requires no such devices. Moreover, a computer can be lodged into another device without much effort, e.g., a personal digital assistant (PDA),a mobile telephone, a GPS receiver, a mobile audio player, to name a few. Computer readable media which are suitable for hoarding computer programs and data consists of all forms of media, and memory devices, non-volatile memory, including semiconductor memory devices, e.g., EEPROM, EPROM, and magnetic disks, flash memory devices; e.g., removable disks or internal hard disks ; magneto optical disks, DVD-ROM disks and CD ROM . The memory can be of non-transitory form such as a RAM, ROM, flash memory, etc. The processor along with the memory can be supplemented by, or subsumed in, special purpose logic circuits.

[0030] In accordance with an example embodiment, the memory 301 includes both static memory (e.g., ROM, CD-ROM, etc.) and dynamic memory (e.g., RAM, magnetic disk, writable optical disk, etc.) for hoarding the executable instructions which when executed perform evaluation of the data integrity. In some example embodiment the memory may be 16 DDR4. In some example embodiments, the communication interface 305 may be

achieved using PCIe protocol along with a JTAG based testing interface 307.The components of the second layer 103 form the organic digital layer. Each of the component is connected to the digital substrate using solder bumps.

[0031] FIG.4 illustrates a third layer 105 of the opto-electronic engine 100. The third layer 105 is a low cost organic analog substrate or PCB that is connected to a plurality of power sources 401, where each of the plurality of power sources 401 is connected to the analog substrate using a solder bumps. **FIG. 5** illustrates assembly of the opto-electronic engine. The first layer 101 is connected to the second layer 103 using solder bumps 107. The second layer 103 is connected to the third layer 105 using the edge connector 109.

[0032] FIGs. 6A-6B assembly of the opto-electronic engine with a micron memory, according to one embodiment of the invention. **FIG. 6A** illustrates a fourth layer 111 that is connected to first layer using solder bumps 107 and the fourth layer 111 is connected to the second layer using another edge connector 113. **FIG. 6B** illustrates provision for integrating micron-memory units 115 with the opto-electronic engine. The micron-memory units 115 represented by M1 to M7 is connected to first substrate 117. The first substrate 117 is connected to the second substrate 119 via process of chip assay. The second substrate 119 is connected to the third substrate 123 via solder bumps 121.

[0033] The above detailed description includes description of the invention in connection with a number of embodiments and implementations. The invention is not limited by the number of embodiments and implementations but covers various obvious modifications and equivalent arrangements which lie within the purview of the appended claims. Though aspects of the invention are expressed in certain combinations among the claims, it is considered that these features may be arranged in any combination and order. Any element, step, or feature used in the detailed description of the invention should not be construed as crucial to the invention unless explicitly mentioned as such. It is also

presumed by the attached claims to consider all such possible features along with advantages of the present invention which shall fall within the scope of the invention and true spirit. Therefore, the specification and accompanied drawings are to be contemplated in an illustrative and exemplary rather than limiting sense.

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