CLAIMS

1. A wafer level surface acoustic wave filter, comprising: a wafer, an electrode layer, a supporting wall and a cover plate; wherein the wafer comprises a substrate layer and a piezoelectric thin film layer, and the substrate layer and the piezoelectric thin film layer are combined together by wafer bonding therebetween;

the electrode layer is arranged on a surface of the piezoelectric thin film layer, the supporting wall is located between the piezoelectric thin film layer and the cover plate, and the supporting wall surrounds between the piezoelectric thin film layer and the cover plate to form a sealed cavity;

the cover plate comprises a first material layer and a second material layer, the first material layer and the second material layer are combined together by wafer bonding therebetween; the second material layer is located on a side of the cover plate close to the sealed cavity; the first material layer uses the same material as the substrate layer, and the second material layer uses the same material as the piezoelectric thin film layer;

wherein the cover plate comprises at least two material layers, and a thickness of each material layer is related to a temperature expansion coefficient of each material layer, wherein the at least two material layers comprise the first material layer and the second material layer.

2. The wafer level surface acoustic wave filter according to claim 1, wherein a ratio of a thickness of the piezoelectric thin film layer to a thickness of the wafer is less than a preset threshold, wherein the preset threshold is set to enable the thickness of the piezoelectric thin film layer to be less than the thickness of the substrate layer.

3. The wafer level surface acoustic wave filter according to claim 2, wherein a value of the preset threshold is 0.1.

4. The wafer level surface acoustic wave filter according to claim 1, wherein the electrode layer comprises an interdigital electrode and a thickened electrode, and the thickened electrode is distributed in at least one of following positions of the interdigital electrode: an input position, an output position, and an earthing position.

5. The wafer level surface acoustic wave filter according to claim 4, further comprising at least one solder ball, the at least one solder ball penetrates the cover plate and the supporting wall in a through silicon via (TSV) manner and then electrically contacts the

electrode layer;

or, the at least one solder ball is electrically connected with the electrode layer in a redistribution layer (RDL) manner.

6. The wafer level surface acoustic wave filter according to any one of claims 1-5, wherein the piezoelectric thin film layer is made from at least one of following materials: lithium tantalate $LiTaO_3$ and lithium niobate $LiNbO_3$.

7. The wafer level surface acoustic wave filter according to any one of claims 1-5, wherein the substrate layer is made from at least one of following materials: silicon Si and sapphire.

8. A wafer level surface acoustic wave filter, comprising: a wafer, an electrode layer, a supporting wall and a cover plate; wherein the wafer comprises a substrate layer and a piezoelectric thin film layer, and the substrate layer and the piezoelectric thin film layer are combined together by wafer bonding therebetween;

the electrode layer is arranged on a surface of the piezoelectric thin film layer, the supporting wall is located between the piezoelectric thin film layer and the cover plate, and the supporting wall surrounds between the piezoelectric thin film layer and the cover plate to form a sealed cavity;

the cover plate comprises a first material layer, a second material layer and a third material layer; the third material layer is located between the first material layer and the second material layer, and the first material layer and the second material layer are combined together by using the third material layer; the second material layer is located on a side of the cover plate close to the sealed cavity; and the first material layer uses the same material as the substrate layer, the second material layer uses the same material as the piezoelectric thin film layer;

wherein a thickness of each material layer of the first material layer, the second material layer and the third material layer is related to a temperature expansion coefficient of each material layer.

9. The wafer level surface acoustic wave filter according to claim 8, wherein a material used for the third material layer is an organic binder.

10. A package method for a wafer level surface acoustic wave filter, comprising:

obtaining a wafer, the wafer comprising a substrate layer and a piezoelectric thin film layer, and the substrate layer and the piezoelectric thin film layer being combined together by wafer bonding therebetween;

preparing an electrode layer on the piezoelectric thin film layer;

preparing a supporting wall on the piezoelectric thin film layer;

obtaining a cover plate, the cover plate comprising a first material layer and a second material layer, the first material layer and the second material layer being combined together by wafer bonding therebetween; the second material layer being located on a side of the cover plate close to a sealed cavity; the first material layer using the same material as the substrate layer, and the second material layer using the same material as the piezoelectric thin film layer; and

sealing the supporting wall and the cover plate, so that the supporting wall surrounds between the piezoelectric thin film layer and the cover plate to form the sealed cavity;

wherein a thickness of each material layer of the first material layer, the second material layer and the third material layer is related to a temperature expansion coefficient of each material layer.

11. A package method for a wafer level surface acoustic wave filter, comprising:

obtaining a wafer, the wafer comprising a substrate layer and a piezoelectric thin film layer, and the substrate layer and the piezoelectric thin film layer being combined together by wafer bonding therebetween;

preparing an electrode layer on the piezoelectric thin film layer;

preparing a supporting wall on the piezoelectric thin film layer;

obtaining a cover plate, the cover plate comprising a first material layer, a second material layer and a third material layer; the third material layer being located between the first material layer and the second material layer, and the first material layer and the second material layer being combined together by using the third material layer; the second material layer being located on a side of the cover plate close to a sealed cavity; the first material layer using the same material as the substrate layer, and the second material layer using the same material as the piezoelectric thin film layer; and

sealing the supporting wall and the cover plate, so that the supporting wall surrounds

between the piezoelectric thin film layer and the cover plate to form the sealed cavity;

wherein a thickness of each material layer of the first material layer, the second material layer and the third material layer is related to a temperature expansion coefficient of each material layer.

12. The package method according to claim 11, wherein a ratio of a thickness of the piezoelectric thin film layer to a thickness of the wafer is less than a preset threshold, wherein the preset threshold is set to enable the thickness of the piezoelectric thin film layer to be less than the thickness of the substrate layer.

13. The package method according to claim 12, wherein a value of the preset threshold is 0.1.

14. The package method according to claim 11, wherein the electrode layer comprises an interdigital electrode and a thickened electrode, and the thickened electrode is distributed in at least one of following positions of the interdigital electrode: an input position, an output position, and an earthing position.

15. The package method according to claim 14, further comprising:

forming a via hole which penetrates the cover plate and the supporting wall in a through silicon via (TSV) manner at a preset position of the cover plate, and implanting a solder ball in the via hole by electroplating, the solder ball electrically contacting the electrode layer.

16. The package method according to any one of claims 11-15, wherein the piezoelectric thin film layer is made from at least one of following materials: lithium tantalate $LiTaO_3$ and lithium niobate $LiNbO_3$; the substrate layer is made from at least one of following materials: silicon Si and sapphire.