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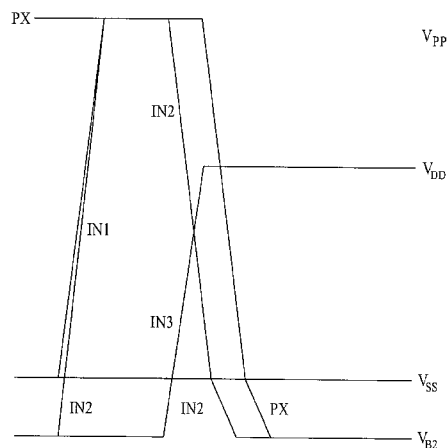
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(54) Title: LOW VOLTAGE OPERATION DRAM CONTROL CIRCUITS



(57) Abstract: Circuits and methods are described for reducing leakage current and speeding access within dynamic random access memory circuit devices. A number of beneficial aspects are described. A circuit is described for an enhanced sense amplifier utilizing complementary drain transistors coupled to the sense or restore signals and driven by gate voltages which extend outside of the voltage range between V_{SS} and V_{DD} . The drain transistors are self reverse-biased in a standby mode. A method is also described for reducing leaking in non-complementary sense amplifiers by modifying the sense and restore gate voltages. Another aspect is a new negative word line method utilizing stacked pull-down transistors and a multistep control circuit. In addition a level shifter scheme is described for preventing unwanted current flow between voltage sources while discharging control signal PX.

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