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1 Semiconductor Device and Method
for Producing the Same

BACKGROUND OF THE INVENTION

5 Field of the Invention

The present invention relates to a semiconductor integrated circuit such as a memory, a photoelectric converting device, a signal processing device or the like adapted for use in various electronic appliances, and more particularly to a semiconductor device featured in the electrode structure of functional elements and a method for producing the same.

Related Background Art

For providing a highly integrated semiconductor circuit device, the development of miniaturized functional elements, such as a MOS transistor with a submicron gate length, is desired in recent years. As a specific example, a MOS transistor with a gate length of $0.8 \mu\text{m}$ occupies an area of ca. $20 \mu\text{m}^2$, suitable for a high level of integration.

25 However the higher level of integration achieved by the miniaturization of functional elements has not necessarily lead to the anticipated satisfactory characteristics. Such discrepancy has been considered attributable to the method for producing such functional elements, and the efforts to solve such drawback has inevitably been directed to the improvement in such

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- 1 producing method. Stated differently, the predominant
perception has been that the preparation of a
satisfactorily functioning element in stable and
reproducible manner is an important factor for the
5 improvement of production yield.

However, the detailed investigation of the
present inventors on the element structure and on the
producing method therefor has revealed that a novel
structure in the electrodes and/or the wirings therefor
10 can achieve a finer geometry and a higher level of
integration, with improved performance. This fact
will be explained in the following, taking a MOSFET
and a planar CMOS transistor as examples.

Fig. 1A is a schematic plan view of an example
15 of the conventional function element, and Fig. 1B is a
schematic cross-sectional view along a line A-A' in
Fig. 1A.

There are illustrated an n-type semiconductor
substrate 1, and a p⁻-type semiconductor area (p⁻ well)
20 2, in which formed are a drain area 3 and a source area
4 both of an n⁺-type semiconductor, and a sub area 5
for ohmic connection of the p⁻ well 2 with an electrode.
Above a channel area in the p⁻ well 2, there is provided
a gate electrode 6 across a gate insulation film, and an
25 n-channel MOSFET is thus formed. A drain electrode 7
and a source electrode 8 respectively contact with the
drain area 3, and with the source and sub areas 4, 5

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1 through contact holes formed in an insulation layer 9.

Multi-terminal elements, such as functional
elements, are often used with a fixed potential at a
terminal. The above-explained MOSFET is used with
5 the source and sub areas thereof maintained at a same
potential. For this purpose, the sub area 5 is
positioned horizontally next to the source area 4
across a field insulation film 10, and said source
area 4 and sub area 5 are short-circuited by the source
10 electrode 8 connected through the contact holes.

Such structure requires a plurality of field
insulation films 10 and contact holes positioned in the
horizontal direction, thus occupying a large area, and
cannot achieve a sufficiently high level of integration
15 even if a fine geometry can be realized.

For resolving the above-mentioned drawback,
there is proposed a semiconductor device as shown in
Figs. 2A and 2B, which are respectively a schematic
plan view and a schematic cross-sectional view along a
20 line B-B' in Fig. 2A. In this structure, the source
area 4 and the sub area 5 are positioned in mutually
contacting manner, thereby dispensing with the field
insulation film therebetween and requiring only one
contact hole for said two areas, instead of one contact
25 hole for each area.

However, even in this structure, the horizontal
positioning of the source area 4 and the sub area 5

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- 1 requires an excessive surface area. Also the contact
hole requires a certain large diameter for achieving
sufficient short-circuiting of the source area 4 and
the sub area 5, so that the design freedom of the
5 production process is difficult to increase.

In the following there will be explained an
example of the planar CMOS transistor.

- The logic circuit in an integrated circuit
requires functional elements with features such as
10 possibility for a high level of integration, a high-
speed operation, a low power consumption etc., and the
planar CMOS transistors are recently used as the
elements meeting such requirements for constituting the
logic circuit. Fig. 3 schematically illustrates the
15 structure of an inversion logic circuit composed of
conventional planar CMOS transistors.

- On a p-type substrate 501, there are formed an
n⁻ layer 502, a p⁻ layer 503, a LOCOS oxide film 504,
and an interlayer insulation film 505. The PMOS
20 transistor includes an n⁺ layer 506 for obtaining the
substrate potential, a p⁺ drain layer 507 and a p⁺
source layer 508, while the NMOS transistor includes
an n⁺ source layer 509, an n⁺ drain layer 510 and a
p⁺ layer 511 for obtaining the substrate potential.
25 There are further provided a gate oxide film 512, a
gate electrode 513 for the PMOS transistor and a gate
electrode 514 for the NMOS transistor.

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1 The drain 507 and the n^+ layer 506 of the PMOS
transistor are given a highest potential, while the
drain 510 and the p^+ layer 511 of the NMOS transistor
are given a lowest potential. The gate electrodes 513,
5 514 of the PMOS and NMOS transistors are mutually
connected by a metal wiring to constitute an input
terminal, while the sources 508, 509 of said transistors
are mutually connected by a metal wiring to constitute
an output terminal, whereby an inversion logic circuit
10 is constructed.

When a voltage equal to or higher than V_{th} of
the NMOS transistor, for example the highest potential,
is applied to the gate electrodes 513, 514, a channel
is formed below the gate of the NMOS transistor, whereby
15 the drain 510 and the source 509 are connected. Thus
an electron current flows through said channel, thus
maintaining the output terminal at the lowest potential.

Then, when a voltage equal to or lower than
(highest potential + V_{th} of PMOS transistor), for
20 example the lowest potential, is applied to the gate
electrodes 513, 514, a channel is formed below the
gate of the PMOS transistor, whereby the drain 507 and
the source 508 thereof are connected. Thus a hole
current flows through said channel, thus maintaining
25 the output terminal at the highest potential.

The inverter function is thus realized, as the
output terminal is maintained at the lowest or highest

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- 1 potential respectively when the highest or lowest
potential is given to the input terminal.

In such conventional CMOS transistors, the
device dimension is reduced by miniaturization of the
5 gate length, contact holes and wiring width. However
such conventional structure requires formation of gate
areas on the surface, and isolation of the NMOS and
PMOS transistors by a LOCOS oxide film, so that the
device dimension has a limitation and a further reduction
10 in size is difficult to achieve.

SUMMARY OF THE INVENTION

In consideration of the foregoing, an object of
the present invention is to provide a semiconductor
15 device suitable for achieving a fine geometry and a
higher level of integration.

Another object of the present invention is to
provide a semiconductor device including very small-
sized functional elements.

20 Still another object of the present invention
is to provide a semiconductor device in which the
number of electrodes is reduced and the element
isolation area can be reduced in size, that the
dimension of the element can be further reduced.

25 Still another object of the present invention
is to provide a method for producing a semiconductor
device suitable for achieving a fine geometry and

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- 1 a higher level of integration.

Still another object of the present invention is to provide a method for producing a semiconductor device capable of filling a fine contact hole or a
5 fine, deep trench, thereby realizing satisfactory electrical connection.

Still another object of the present invention is to provide a method for producing a semiconductor device, capable of significantly improving the
10 electrical characteristics of the above-mentioned semiconductor device and of improving the production yield.

For attaining the above-mentioned objects, the present invention is featured by the following
15 structure. The semiconductor device of the present invention, provided with a first semiconductor area of a first conductive type, and a second semiconductor area, formed on said first semiconductor area, of a second conductive type different from said first
20 conductive, is featured by facts that an electrode electrically connected to said first semiconductor area is formed through said second semiconductor area, and that said first and second semiconductor areas are electrically short-circuited by said electrode.

25 The above-explained structure is additionally featured by facts that said second semiconductor area is a source or drain area of a field effect transistor,

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1 and that said electrode is composed of aluminum or a
conductive material principally composed of aluminum.

Said structure is further featured by facts
that the field effect transistor has a buried drain
5 area and a buried gate area, that a PMOS transistor
and an NMOS transistor are formed on respective sides of
said buried gate, that said second semiconductor area
constitutes said buried drain area, and that said
electrode reaching the drain area is provided in at
10 least either of said PMOS and NMOS transistors.

Said structure is further featured by a fact
that said electrode is composed of aluminum or a
conductive material principally composed of aluminum.

An additional feature is that said semiconductor
15 device is a NOT circuit element, a NOR circuit element
or a NAND circuit element.

Also the semiconductor device producing method
of the present invention is featured by a first step
for forming an aperture in said second semiconductor
20 area thereby exposing a part of said first semiconductor
area, and a second step for depositing a conductive
material in said aperture, wherein said second step is
to deposit aluminum or a conductive material principally
composed of aluminum into said aperture by a CVD method
25 utilizing alkylaluminum hydride gas and hydrogen.

Said method is further featured by a fact that
said alkylaluminum hydride is dimethylaluminum hydride.

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1 The semiconductor device producing method of
the present invention is furthermore featured by:

a step for burying drain areas of PMOS
transistor and an NMOS transistor in a semiconductor
5 substrate;

a step for forming an aperture so as to
penetrate the junction portion between the drain area
of said PMOS transistor and the drain area of said
NMOS transistor;

10 a step for forming an insulation film covering
the internal surface of said aperture;

a step for depositing, in said aperture, a
common gate for said PMOS and NMOS transistors; and

a step for forming a buried electrode reaching
15 at least either of the buried drain area of said PMOS
transistor and the buried drain area of said NMOS
transistor.

Said method is further featured by a fact that
said buried electrode is formed by formation of an
20 aperture reaching at least either of said two buried
drain areas, and by selective deposition of aluminum in
said aperture by a CVD method utilizing dimethylaluminum
hydride and hydrogen.

The present invention can provide a semiconductor
25 device including very small functional elements which
can be formed with necessary minimum components without
unnecessary planar areas, thereby being capable of

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1 significantly reducing the layout area and adapted for
achieving a fine geometry and a high level of integration.

Also the present invention allows to reduce
the number of electrodes and reduce the element
5 isolation area in size, thereby further decreasing
the dimension of the element.

Furthermore, the present invention utilizes
aluminum electrode formation by low-temperature aluminum
deposition by a CVD method utilizing alkylaluminum
10 hydride gas and hydrogen, thereby significantly
improving the electrical characteristics and the
production yield.

BRIEF DESCRIPTION OF THE DRAWINGS

15 Figs. 1A and 1B illustrate an example of the
conventional semiconductor device, wherein Fig. 1A is a
schematic plan view thereof and Fig. 1B is a schematic
cross-sectional view along a line A-A' in Fig. 1A;

Figs. 2A and 2B illustrate another example
20 of the conventional semiconductor device, wherein
Fig. 2A is a schematic plan view thereof and Fig. 2B is
a schematic cross-sectional view along a line B-B' in
Fig. 2A;

Fig. 3 is a schematic cross-sectional view of
25 a conventional CMOS transistor;

Figs. 4A, 4B, 4C and 4D are cross-sectional
views showing features of the semiconductor device of

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1 the present invention and illustrating variations thereof;

Fig. 5A is a cross-sectional view of a preferred embodiment of the present invention;

Fig. 5B is an equivalent circuit diagram
5 thereof;

Figs. 6 to 17 are views showing steps for producing the structure shown in Fig. 5;

Figs. 18 to 20 are schematic views of continuous metal film forming apparatus suitable for forming a
10 CVD-Al film or a metal film principally composed of aluminum;

Fig. 21 is a view showing the function of the apparatus shown in Fig. 20;

Figs. 22A, 22B and 22C are schematic perspective
15 views showing film forming procedure for forming electrodes and wirings by the Al-CVD method;

Fig. 23A is a schematic plan view of a MOSFET constituting a first embodiment of the present invention;

20 Fig. 23B is a schematic cross-sectional view along an X-X' line in Fig. 23A;

Figs. 24A to 24E are schematic cross-sectional views showing the method for producing the MOSFET shown in Figs. 23A and 23B;

25 Fig. 25A is a schematic cross-sectional view of a semiconductor device, constituting a second embodiment of the present invention and applied to a CMOS inverter

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1 circuit;

Fig. 25B is a circuit diagram of said embodiment;

Fig. 25C is a schematic cross-sectional view
of a device by the prior art, as a comparative example
5 to the above-mentioned embodiment;

Fig. 26A is a schematic plan view of a
semiconductor device constituting a third embodiment of
the present invention and applied to a CMOS inverter
circuit;

10 Fig. 26B is a schematic cross-sectional view
along a line Y-Y' in Fig. 26A;

Fig. 26C is a circuit diagram of said
embodiment;

Fig. 27A is a schematic plan view of a
15 semiconductor device constituting a fourth embodiment
of the present invention and applied to a NAND circuit
composed of vertical MOS transistors;

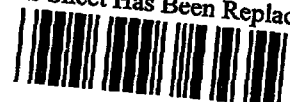
Fig. 27B is a schematic cross-sectional view
along a line Z-Z' in Fig. 27A;

20 Fig. 27C is a circuit diagram of said
embodiment;

Fig. 28 is a schematic cross-sectional view of
a fifth embodiment of the present invention; and

Fig. 29 is a schematic cross-sectional view of
25 a sixth embodiment of the present invention.

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1 DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now the present invention will be clarified in detail by preferred embodiments thereof.

5 A preferred embodiment of the present invention is constructed in the following manner. In functional elements such as field effect transistor, bipolar transistor, diffusion resistor etc., terminals to be used in an electrically short-circuited state are formed by forming, on a first semiconductor area of
10 a first conductive type, a second semiconductor area of a second conductive type, and forming an electrode contacting said first semiconductor area through said second semiconductor area.

15 Figs. 4A to 4D are schematic cross-sectional views showing various modes of the present invention.

In an example shown in Fig. 4A, there is formed an electrode 120 which reaches a first semiconductor area 102, penetrating the center of a second semiconductor area 104.

20 In an example shown in Fig. 4B, the electrode 120 reaches the first semiconductor area 102 through an end portion of the second semiconductor area 104.

In an example shown in Fig. 4C, the electrode 120 does not sink into the first semiconductor area 102, as in the case of Fig. 4A, but merely contacts
25 the upper surface thereof. 121 indicates a source electrode wiring.

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1 Figs. 4A to 4C do not show the sub area. Such
sub area can be dispensed with if the material of the
electrode 120 can make ohmic contact with the first
semiconductor area 102. If necessary, a sub area 105
5 may be formed, as shown in Fig. 4D, at a position
where the electrode contacts the first semiconductor
area 102. The electrode 120 is preferably provided with
an insulation film on a large part of the lateral wall
thereof and contacts the area 104 through a silicon
10 area exposed in said insulation film.

Fig. 5A is a schematic cross-sectional view of
another embodiment of the present invention, and Fig.
5B is an equivalent circuit diagram thereof.

In Fig. 5A there are shown a p-type substrate
15 57, an n^- diffusion layer 56, a buried drain area 51
of a PMOS transistor, a channel area 52 of the PMOS
transistor, a source area 53 thereof, a gate oxide
film 54 common for PMOS and NMOS transistor, a poly-
silicon gate 55, an insulation film 58, a source area
20 201 of an NMOS transistor, a channel area 202 thereof,
a buried drain area 203 thereof, a buried electrode 60
common for the drain and well of the PMOS transistor,
a buried electrode 61 common for the drain and well of
the NMOS transistor, source electrodes 62, 63
25 respectively of the PMOS and NMOS transistors, and a
common gate electrode 64.

As shown in the equivalent circuit in Fig. 5B,

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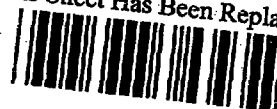
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1 a highest potential is given to the drain 51 and the
well 52 of the PMOS transistor 30, while a lowest
potential is given to the drain 203 and the well 202
of the NMOS transistor 31. The common gate 55 of the
5 PMOS and NMOS transistors constitutes an input terminal,
while the sources 53, 201 of the PMOS and NMOS
transistors are mutually connected to constitute an
output terminal, whereby an inversion logic circuit is
constituted. When the highest potential is applied to
10 the input terminal, the NMOS transistor 31 is rendered
conductive to provide the output terminal with the
lowest potential. When the lowest potential is applied
to the input terminal, the PMOS transistor 30 is
rendered conductive to provide the output terminal
15 with the highest potential. The inversion logic
operation is thus realized.

In the present invention, as shown in Fig. 5A,
fine buried electrodes 60, 61 are buried deep into
the semiconductor substrate. In the prior art, it
20 has been difficult to fill, even a contact hole of a
large aspect ratio, completely with a conductive
material, and it has been impossible to form a deep
buried electrode as shown in Fig. 5A by metal
deposition.

25 The present invention is based on a finding
that a metal of satisfactory quality can be deposited
with extremely good selectivity by a novel CVD method

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1 to be explained later.

In the following there will be explained the process for producing the CMOS transistor shown in Fig. 5, with reference to Figs. 6 to 17.

5 At first, in the p-type substrate 57, the n^- diffusion layer 56 was formed by ion implantation and an annealing step (Fig. 6).

Then the n^+ drain layer 203 in the substrate 57 and the p^+ drain layer 51 in the n^- layer 56 were
10 formed respectively by ion implantation and annealing (Fig. 7).

The n^- layer 52 was subsequently formed over the entire surface by CVD (Fig. 8).

Then an etching process was conducted to form
15 an aperture penetrating the n^- layer 52, p^+ layer 51 and n^+ layer 203 and reaching the n^- layer 56 (Fig. 9).

Ion implantation was conducted in an area for forming the NMOS transistor in the n^- layer, followed by annealing, to form the p^- layer 202 (Fig. 10).

20 Then the p^+ source area 53 and the n^+ layer 59 for electrode connection were formed in the n^- layer 52, and the n^+ source area 201 and the p^+ area 204 for electrode connection were formed in the p^- layer 202, respectively by ion implantation and annealing (Fig.
25 11).

Then the gate oxide film 54 was formed by thermal oxidation (Fig. 12).

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1 Subsequently polysilicon was deposited in the
aperture by CVD, followed by an etch-back process, to
form the buried polysilicon layer (Fig. 13).

The interlayer insulation film 58 was deposited
5 by CVD (Fig. 14), and the contact holes for the drains
51, 203 and the wells 52, 202 were formed by etching
(Fig. 15).

Then Al was deposited in the contact holes by
the above-mentioned CVD utilizing DMAH and H_2 , thereby
10 forming the electrodes 60, 61 common for the drains
and wells (Fig. 16).

Contact holes for the source and the gate
were formed by etching (Fig. 17).

Finally Al was deposited in the contact holes
15 by CVD, and the source electrodes 111, 112 and the
gate electrode 63 were formed to complete the
structure shown in Fig. 5A. The inversion logic
circuit was formed by patterning the Al wirings in
such a manner that the source electrodes of the PMOS
20 and NMOS transistors are mutually connected.

When a voltage equal to or higher than V_{th} of
the NMOS transistor, for example the highest potential,
is applied to the gate electrode 55, a channel is
formed below the gate of the NMOS transistor, whereby
25 the drain 203 and the source 201 thereof are connected.
Thus an electron current flow through said channel to
maintain the output terminal at the lowest potential.

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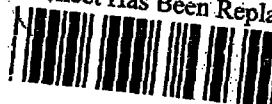
1 Then, when a voltage equal to or lower than
 (highest potential + V_{th} of PMOS transistor), for
 example the lowest potential, is applied to the gate
 electrode 55, a channel is formed below the PMOS
5 transistor, whereby the drain 51 and the source 53
 thereof are connected. Thus a hole current flows through
 said channel to maintain the output terminal at the
 highest potential.

 Thus the inverter operation is realized, as
10 the output terminal is maintained at the lowest or
 highest potential respectively when the input terminal
 is given the highest or lowest potential.

 The present embodiment can be constructed with
 only one gate electrode, and does not require an
15 isolation area, as the gate serves to separate the
 PMOS and NMOS transistors. It is therefore rendered
 possible to reduce the number of electrodes and to
 reduce the isolation area in size, thereby obtaining
 a logic circuit of a reduced dimension.

20 The source electrodes 62, 63 and the gate
 electrode 64 may be composed, like the electrode 120
 in the aforementioned first example or the buried
 electrodes 60, 61 in the second example, of
 polycrystalline silicon, Al, W, Mo, Cu, Al-Cu,
25 Al-Cu, Al-Ti, Al-Si-Ti, Al-Si-Cu, WSi_2 , $MoSi_2$ or
 $TiSi_2$, but, in consideration of the production process,
 they are preferably composed of aluminum or a material

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1 principally composed of aluminum such as Al-Si, Al-Cu,
Al-Ti, Al-Si-Ti or Al-Si-Cu. Besides such material is
preferably deposited by a depositing method to be
explained in the following.

5 (Film forming method)

In the following there will be explained a
film forming method suitable for electrode formation
according to the present invention.

Said method is adapted for filling an aperture
10 with a conductive material, for forming the electrode
of the above-explained structure.

Said film forming method consists of forming a
deposited film by a surface reaction on an electron
donating substrate, utilizing alkylaluminum hydride
15 gas and hydrogen gas (said method being hereinafter
called Al-CVD method).

An aluminum film of satisfactory quality can
be deposited by heating the surface of the substrate
in the presence of a gaseous mixture particularly
20 consisting of monomethylaluminum hydride (MMAH) or
dimethylaluminum hydride (DMAH) as the raw material
gas and hydrogen as the reaction gas. At the selective
Al deposition, the substrate surface is preferably
maintained at a temperature at least equal to the
25 decomposition temperature of alkylaluminum hydride
but lower than 450°C, more preferably between 260°C
and 440°C, by direct or indirect heating.



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1 The heating of the substrate in the above-
mentioned temperature range may be achieved by direct
or indirect heating, but formation of an Al film of
satisfactory quality can be achieved with a high
5 deposition speed, particularly by direct heating. For
example, with the more preferred temperature range of
260° - 440°C, a satisfactory film can be obtained with
a deposition speed of 300 - 5000 Å/min. which is higher
than in the resistance heating. Such direct heating
10 (substrate being heated by direct transmission of
energy from the heating means) can be achieved by
heating with a lamp such as a halogen lamp or a xenon
lamp. Also indirect heating may be achieved for
example by resistance heating, conducted by a heat
15 generating member provided in a substrate support
member, for supporting the substrate to be subjected
to film deposition, provided in a film depositing
space.

 This method, if applied to a substrate having
20 both an electron donating surface area and an electron
non-donating surface area, allows to form single
crystal of aluminum with satisfactory selectively
solely on the electron donating surface area. Such
aluminum is excellent in all the properties required
25 for the electrode/wiring material, including a low
hillock frequency and a low alloy spike frequency.

 This is presumably because the semiconductive

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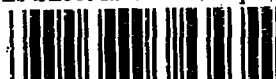
1 or conductive surface constituting an electron donating
surface can selectively develop an aluminum film of
satisfactory quality and excellent crystalline character
of said Al film excludes or significantly reduces the
5 alloy spike formation etc. resulting from an eutectic
reaction with the underlying silicon. Such Al film,
when employed as an electrode of a semiconductor device,
provides the advantages far exceeding the concept of the
conventional Al electrode and not anticipated in the
10 prior technology.

As explained above, the Al deposited in an
aperture with an electron donating surface, for
example an aperture formed in an insulating film and
exposing the surface of a semiconductor substrate
15 therein, has a monocrystalline structure. Besides said
Al-CVD method can achieve selective deposition of
following metal films principally composed of aluminum,
with likewise satisfactory quality.

For example, the electrode may be formed by
20 selective deposition of various conductive materials
such as Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu by
the use of a mixed gaseous atmosphere employing, in
addition to alkylaluminum hydride gas and hydrogen, a
suitable combination of:

25 Si-containing gas such as SiH_4 , Si_2H_6 , Si_3H_8 ,
 $\text{Si}(\text{CH}_3)_4$, SiCl_4 , SiH_2Cl_2 or SiHCl_3 ;

Ti-containing gas such as TiCl_4 , TiBr_4 or



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1 $Ti(CH_3)_4$; and/or

Cu-containing gas such as copper

bisacetylacetonate $Cu(C_5H_7O_2)_2$, copper

bisdipyvaloylmethanite $Cu(C_{11}H_{19}O_2)_2$ or copper

5 bishexafluoroacetylacetonate $Cu(C_5HF_6O_2)_2$.

Also since said Al-CVD method is excellent in selectivity and provides satisfactory surface characteristics on the deposited film, there can be obtained a metal film suitable and widely usable for the wirings of a semiconductor device, by employing a non-selective film forming method in a next deposition step to form a metal film composed solely or principally of aluminum not only on the selectively deposited aluminum film mentioned above but also on the SiO_2 insulation film.

10

15

Examples of such metal films include combinations of selectively deposited Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu and non-selectively deposited Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu.

20 Said non-selective film deposition may be achieved by CVD other than the aforementioned Al-CVD, or by sputtering.

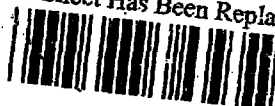
(Film forming apparatus)

In the following there will be explained a film forming apparatus suitable for the electrode formation according to the present invention.

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Figs. 18 to 20 schematically illustrate a

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- 1 continuous metal film forming apparatus suitable for
executing the film forming method explained above.

As shown in Fig. 2, said apparatus is composed
of a loading chamber 311, a CVD reaction chamber (first
5 film forming chamber) 312, an Rf etching chamber 313,
a sputtering chamber (second film forming chamber) 314
and an unloading chamber 315, which are rendered
sealable from the external atmosphere and mutually
communicatable by means of gate valves 310a - 310f and
10 can be respectively made vacuum or reduced in pressure
by vacuum systems 316a - 316e. The loading chamber
311 is used for eliminating the atmosphere of substrate
and replacing it with H_2 prior to the deposition, in
order to improve the throughput. The next CVD reaction
15 chamber 312, for selective deposition onto the substrate
under normal or reduced pressure, is provided therein
with a substrate holder 318 with a resistance heater 317
for heating the substrate surface subjected to film
formation at least within a temperature range of $200^\circ -$
20 $450^\circ C$, and receives the raw material gas such as of
alkylaluminum hydride, which is gasified by bubbling
with hydrogen in a bubbler 319-1, through a raw
material gas supply line 319, and hydrogen as the
reaction gas through a gas line 319'. The Rf etching
25 chamber 313, for cleaning (etching) of the substrate
surface in Ar atmosphere after the selective deposition,
is provided therein with a substrate holder 320 capable

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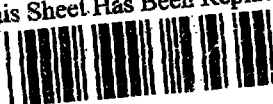
1 of heating the substrate at least within a range of
100° - 250°C and an Rf etching electrode line 321,
and is connected to an Ar gas supply line 322. The
sputtering chamber 314, for non-selective deposition of
5 a metal film by sputtering in Ar atmosphere, is provided
therein with a substrate holder 323 to be heated at
least within a range of 200° - 250°C and a target
electrode 324 for mounting a sputtering target 324a,
and is connected to an Ar gas supply line 325. The
10 final unloading chamber 315, for adjustment of the
substrate after metal film deposition and prior to the
exposure to the external atmosphere, is designed to be
capable of replacing the atmosphere with N₂.

Fig. 19 shows another example of the continuous
15 metal film forming apparatus, wherein same components as
those in Fig. 18 are represented by same numbers. The
apparatus in Fig. 19 is different from that in Fig. 18
in that the substrate surface is directly heated by
halogen lamps 330, and, for this purpose, the substrate
20 holder 312 is provided with projections 331 for supporting
the substrate in a floating state.

Direct heating of the substrate surface with
such structure further increases the deposition speed
as explained before.

25 The continuous metal film forming apparatus of
the above-explained structure is equivalent, in
practice, to a structure shown in Fig. 20, in which

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1 the loading chamber 311, CVD reaction chamber 312, Rf
etching chamber 313, sputtering chamber 314 and unloading
chamber 315 are mutually combined by a transport chamber
326. In this structure, the loading chamber 311 serves
5 also as the chamber 315. In said transport chamber 326,
there is provided an arm 327 constituting transport
means, rotatable in both directions A-A and extendable
and retractable in direction B-B, whereby the substrate
can be transferred in succession from the loading chamber
10 311 to the CVD reaction chamber 312, Rf etching chamber
313, sputtering chamber 314, and finally to the unloading
chamber 315 without exposure to the external atmosphere,
as indicated by arrows in Fig. 21.

(Film forming process)

15 Now there will be explained the film forming
process for forming the electrodes and wirings according
to the present invention.

Fig. 22 illustrates the film forming procedure
for forming the electrodes and wirings according to
20 the present invention, in schematic perspective views.

At first the outline of the procedure will be
described. A semiconductor substrate with an insulating
film having apertures therein is placed in the film
forming chamber, and the surface thereof is maintained
25 for example at 250° - 450°C. Thermal CVD conducted in
a mixed atmosphere of DMAH gas as alkylaluminum hydride
and hydrogen gas causes selective deposition of Al on

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1 the semiconductor exposed in the apertures. There may
naturally be conducted selective deposition of a metal
film principally composed of Al, for example Al-Si,
by introduction for example of Si-containing gas, as
5 explained before. Then a metal film composed solely
or principally of Al is non-selectively formed by
sputtering, on the selectively deposited Al and on the
insulation film. Subsequently the non-selectively
deposited metal film is patterned into the shape of
10 desired wirings, thereby obtaining the electrodes and
the wirings.

This procedure will be explained in greater
detail with reference to Figs. 19 and 22. At first
prepared is a substrate, consisting for example of a
15 monocrystalline silicon wafer bearing thereon grooves
of different sizes, and covered by an insulation film
except for the bottoms of said grooves.

Fig. 22A schematically shows a part of said
substrate, wherein shown are a monocrystalline silicon
20 substrate 401 constituting a conductive substrate; a
thermal silicon oxide film 402 constituting an
insulation film; apertures 403, 404 of different sizes;
and a groove 410.

The formation of Al film, constituting a first
25 wiring layer, on the substrate is conducted in the
following manner, with the apparatus shown in Fig. 19.

At first the above-explained substrate is

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1 placed in the loading chamber 311, in which a hydrogen
atmosphere is established by introduction of hydrogen
as explained before. Then the reaction chamber 312
is evacuated by the vacuum system 316b approximately
5 to 1×10^{-8} Torr, though Al film formation is still
possible with a higher pressure.

Then DMAH gas obtained by bubbling is
supplied from the gas line 319, utilizing H_2 as the
carrier gas.

10 Also hydrogen as the reaction gas is introduced
from the second gas line 319', and the interior of the
reaction chamber 312 is maintained at a predetermined
pressure, by the adjustment of an unrepresented slow leak
valve. A typical pressure is about 1.5 Torr. DMAH is
15 introduced into the reaction chamber from the DMAH
line, with a total pressure of about 1.5 Torr and a
DMAH partial pressure of about 5.0×10^{-3} Torr. Then
the halogen lamps 330 are energized to directly heat
the wafer, thereby causing selective Al deposition.

20 After a predetermined deposition time, the
DMAH supply is interrupted. Said deposition time is so
selected that the Al film on Si (monocrystalline silicon
substrate 1) becomes equally thick as SiO_2 (thermal
silicon oxide film 2), and can be experimentally
25 determined in advance.

In this process, the substrate surface is heated
to ca. 270°C by direct heating, and the procedure

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1 explained above causes selective deposition of an Al
film 405 in the aperture, as shown in Fig. 22B.

The foregoing is called a first film forming
step for forming an electrode in an aperture.

5 After said first film forming step, the CVD
reaction chamber 312 is evacuated, by the vacuum
system 316b, to a pressure not exceeding 5×10^{-3} Torr.
Simultaneously the Rf etching chamber 313 is evacuated
to a pressure not exceeding 5×10^{-6} Torr. After
10 confirmation of said evacuations of the chambers, the
gate valve 310c is opened, then the substrate is moved
from the CVD reaction chamber 312 to the Rf etching
chamber 313 by the transport means, and said gate valve
is closed. The Rf etching chamber 313 is evacuated to
15 a pressure not exceeding 10^{-6} Torr, and is then
maintained in argon atmosphere of $10^{-1} - 10^{-3}$ Torr by
argon supply from the supply line 322. The substrate
holder 320 is maintained at ca. 200°C, and an Rf power
of 100 W is supplied to the Rf etching electrode 321
20 for about 60 seconds to generate an argon discharge in
said chamber 313, whereby the substrate surface is
etched with argon ions and the unnecessary surfacial
layer of the CVD deposition film can be eliminated.
The etch depth in this case is about 100 Å,
25 corresponding to the oxide film. Said surface
etching, of the CVD deposition film, conducted in the
Rf etching chamber, may be dispensed with since said

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- 1 surfacial layer is free from oxygen etc. as the
 substrate is transported in vacuum. In such case, the
 Rf etching chamber 313 may serve for varying the
 temperature within a short time if the temperature
5 is significantly different between the CVD reaction
 chamber 312 and the sputtering chamber 314.

 After said Rf etching, the argon supply is
 terminated, and the Rf etching chamber 313 is
 evacuated to 5×10^{-6} Torr. Then the sputtering
10 chamber is also evacuated to 5×10^{-6} Torr or lower,
 and the gate valve 310d is opened. The substrate
 is transferred from the Rf etching chamber 313 to
 the sputtering chamber 314 by the transport means,
 and said gate valve 310d is closed.

- 15 Subsequently the sputtering chamber is
 maintained at argon atmosphere of $10^{-1} - 10^{-3}$ Torr
 as in the Rf etching chamber 313, and the substrate
 holder 323 is maintained at $200^{\circ} - 250^{\circ}\text{C}$. Argon
 discharge is induced by a DC power of 5 - 10 kW to
20 scrape the target of Al or Al-Si (Si: 0.5%) with argon
 ions, thereby depositing Al or Al-Si onto the substrate
 with a deposition speed of ca. $10000 \text{ \AA}/\text{min}$. This is a
 non-selective deposition step, and is called a second
 film forming step for forming wirings connected to the
25 electrodes.

 After the formation of the metal film of about
 $5000 \text{ \AA}$ on the substrate, the argon supply and the DC

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1 power application are terminated. The loading chamber
311 is evacuated to a pressure of 5×10^{-3} Torr or
lower, then the gate valve 310e is opened and the
substrate is moved. After the gate valve 310e is
5 closed, the loading chamber 311 is supplied with
nitrogen gas to the atmospheric pressure. Subsequently
the gate valve 310f is opened and the substrate is
taken out.

The second Al film deposition step explained
10 above forms an Al film 406 on the SiO_2 film 402, as
shown in Fig. 22C.

Subsequently said Al film 406 is patterned
to obtain the wirings of desired shape.
(Experimental examples)

15 In the following there will be shown experimental
results indicating the superiority of the above-explained
Al-CVD method and the satisfactory quality of the Al
film deposited by said method in the apertures.

There were prepared plural substrates, each
20 consisting of an N-type monocrystalline silicon wafer,
provided thereon with a thermally oxidized SiO_2 film
of a thickness of 8000 Å, in which grooves of different
sizes from $0.25 \times 0.25 \mu\text{m}$ to $100 \times 100 \mu\text{m}$ were formed
by patterning to expose the underlying monocrystalline
25 silicon (samples 1-1).

These samples were subjected to the Al film
formation by the Al-CVD method, employing DMAH as

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1 the raw material gas and hydrogen as the reaction
gas, with a total pressure of 1.5 Torr and a DMAH
partial pressure of 5.0×10^{-3} Torr, and with the
substrate surface temperatures selected in a range of
5 200° - 490°C by direct heating under the regulation
of electric power supplied to the halogen lamps. The
obtained results are summarized in Table 1.

10

15

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25 20 15 10 5 1

Table 1

Substrate surface temp. (°C)	200	230	250	260	270	280	300	350	400	440	450	460	470	480	490
Deposition speed (Å/min.)	← 1000-1500 → ← 3000 - 5000 →														
Si linear defects	← not observed →														
Carbon content	← not detected →														
Resistivity (μΩcm)	← 2.7 - 3.3 → ← 2.8 - 3.4 →														
Reflectance (%)	← 8.5 - 9.5 → ← 90 - 95 → ← ca. 60 →														
Hillock (> 1 μm) density (cm ⁻²)	← 1 - 10 ² → ← 0 - 10 → ← 10 - 10 ⁴ →														
Spike formation (%) destruction frequency of 0.15μm junction)	← 0 → ← 0 - 30 →														

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1 As will be apparent from Table 1, aluminum was
deposited in the apertures with a deposition speed as
high as 3000 - 5000 Å/min. at the substrate surface
temperature of 260°C or higher obtained by direct
5 heating.

The Al film in the apertures, obtained in a
substrate surface temperature range of 260° - 440°C,
showed satisfactory characteristics, with no carbon
content, a resistivity of 2.8 - 3.4 μΩcm, a reflectance
10 of 90 - 95%, a hillock ($\geq 1 \mu\text{m}$) density of 0 - 10 cm⁻²,
and an almost zero spike formation (frequency of
destruction of 0.15 μm junction).

On the other hand, though the film quality
obtained in a surface temperature range of 200° -
15 250°C was somewhat inferior to that obtained in the
temperature range of 260° - 440°C, it is considerably
better than that obtainable with the conventional
technology, but the deposition speed could not exceed
1000 - 1500 Å/min.

20 At the substrate surface temperature equal to
or higher than 450°C, the quality of the Al film in
the apertures were deteriorated, with a reflectance of
60% or lower, a hillock ($\geq 1 \mu\text{m}$) density of 10 - 10⁴
cm⁻² and an alloy spike formation of 0 - 30%.

25 In the following there will be explained how
the above-explained method can be advantageously applied
to the filling of the grooves.

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1 Said method can be advantageously applied to
the grooves composed of the materials explained in the
following.

5 The Al film formation was conducted on the
following substrates (samples) under the same conditions
as in the Al film formation on the above-mentioned
samples 1-1.

10 Samples 1-2 were prepared by forming, on
monocrystalline silicon constituting a first substrate
surface material, a silicon oxide film constituting a
second substrate surface material by means of CVD
method, and forming grooves by a photolithographic
process to locally expose the surface of monocrystalline
silicon in the bottoms of said grooves. The thermal
15 SiO_2 film was 8000 Å thick, and the exposed areas of
monocrystalline silicon were sizes from 0.25 x 0.25 μm
to 100 x 100 μm, with a groove depth of 2 μm. (Such
samples will hereinafter be represented as "CVD SiO_2
(or simply SiO_2)/monocrystalline silicon".)

20 There were also prepared:

a sample 1-3 of boron-doped oxide film formed
by normal pressure CVD (hereinafter written as BSG)/
monocrystalline silicon;

25 a sample 1-4 of phosphor-doped oxide film formed
by normal pressure CVD (PSG)/monocrystalline silicon;

a sample 1-5 of boron- and phosphor-doped oxide
film formed by normal pressure CVD (BSPG)/monocrystalline

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1 silicon;

a sample 1-6 of nitride film formed by plasma
CVD (P-SiN)/monocrystalline silicon;

a sample 1-7 of thermal nitride film (T-SiN)/
5 monocrystalline silicon;

a sample 1-8 of nitride film formed by low
pressure CVD (LP-SiN)/monocrystalline silicon; and

a sample 1-9 of nitride film formed by ECR
(ECR-SiN)/monocrystalline silicon.

10 Further, samples 1-11 to 1-179 were prepared by
taking all the combinations of the first surface
materials of 18 kinds and the second surface materials
of 9 kinds shown in the following. (It is to be noted
that the sample numbers 1-10, 20, 30, 40, 50, 60, 70,
15 80, 90, 100, 110, 120, 130, 140, 150, 160 and 170 are
lacking.) The first surface materials employed were
monocrystalline silicon (mono-Si), polycrystalline
silicon (poly-Si), amorphous silicon (a-Si), tungsten
(W), molybdenum (Mo), tantalum (Ta), tungsten silicide
20 (WSi), titanium silicide (TiSi), aluminum (Al), aluminum
silicon (Al-Si), titanium aluminum (Al-Ti), titanium
nitride (Ti-N), copper (Cu), aluminum silicon copper
(Al-Si-Cu), aluminum palladium (Al-Pd), titanium (Ti),
molybdenum silicide (Mo-Si), and tantalum silicide
25 (Ta-Si). The second substrate surface materials employed
were T-SiO₂, SiO₂, BSG, PSG, BPSG, P-SiN, T-SiN, LP-SiN
and ECR-SiN. In all these samples, there could be

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1 obtained satisfactory Al films comparable to those in
the aforementioned samples 1-1.

Subsequently, the Al was non-selectively
deposited by sputtering on the substrates subjected to
5 the selective Al deposition as explained above, and was
then patterned. Such deposited film is effective for
three-dimensional connections of buried wirings.

The Al film obtained by sputtering and the
selectively deposited Al film in the apertures showed
10 electrically and mechanically satisfactory contact,
because of the improved surface state of the Al film in
the apertures.

Embodiment 1

In the following there will be explained a
15 MOSFET constituting a first embodiment of the present
invention.

Fig. 23A is a schematic plan view of a MOSFET
of said first embodiment, and Fig. 23B is a schematic
cross-sectional view along a line X-X' in Fig. 23A.

20 There are shown a silicon substrate 101 of n-type
semiconductor; a p⁻ well 102; a drain area 103 of n⁺
type formed in the p⁻ well 102; a source area 104 formed
similarly to the drain area 103; a p⁺ sub area 105 for
making ohmic contact between the p⁻ well 102 and the
25 source electrode; a polycrystalline silicon gate
electrode 106; a gate electrode wiring 106' connected
to said gate electrode 106 by a through-hole; an

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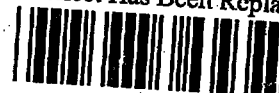
1 insulation film 109 of silicon oxide; and a field
insulation film 110 with bird's beak formed by selective
oxidation.

An electrode 120, constituting the most
5 characteristic structure of the present invention, is
composed of monocrystalline aluminum, and penetrates
the contact hole in the insulation layer 109 and the
source area 104 and reaches the sub area 105 buried in
the p⁻ well 102. A source electrode wiring 121, formed
10 on the insulation layer 109 and the electrode 120, is
composed of aluminum. A drain electrode 122, buried
in the contact hole on the drain area 103, is composed
of monocrystalline aluminum. There is also provided a
drain electrode wiring 123.

15 In the following explained is the method for
producing the MOSFET of the above-explained structure,
with reference to Figs. 24A to 24E.

On the silicon substrate, there were conducted,
by already known manufacturing process, formation of
20 the p⁻ well 102, drain area 103, source area 104 and
field insulation film 110, then formation of the
insulation layer 109 thereon, and formation of the gate
electrode 106 in said insulation layer 109. Then a
photolithographic process utilizing photoresist was
25 applied to form a hole, as a photoresist image, on
the insulation layer 109 above the source area 104.
Then dry etching with CHF₃ - C₂F₆ was conducted to form

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- 1 a hole in the insulation layer 109 down to the source area as shown in Fig. 24A (hole opening step).

Subsequently dry etching with Cl_2 - CBrF_3 was conducted without removal of the photoresist, thereby
5 forming a hole penetrating the source area 104 and entering the p^- well 102 (etching step), and the sub area 105 was formed at the bottom of thus formed hole, as shown in Fig. 24B (p^+ forming step).

Then, as shown in Fig. 24C, aluminum was
10 deposited to the upper surface of the insulation film 109 by the aforementioned Al-CVD method utilizing DMAH and hydrogen, with the substrate surface maintained at 270°C (CVD-Al forming step).

Then the contact hole is formed in the
15 insulation layer 109 on the drain area 103 by a known process as shown in Fig. 24D (hole opening step), and aluminum was deposited by the above-mentioned Al-CVD method. The device was completed then by forming the source electrode wiring 121 and the drain electrode
20 wiring 123 respectively on said electrode 102 and on the drain area 103 by sputtering as shown in Fig. 24E (Al wiring step).

As explained in the foregoing, the present invention allows to constitute a MOSFET, which is to be
25 used with the source area and the sub area thereof in an electrically shortcircuited state, with necessary minimum components and without any unnecessary surface area.

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1 Embodiment 2

Fig. 25A illustrates a second embodiment of the present invention.

5 In said second embodiment, the present invention is applied to a CMOS inverter circuit. The production method will not be explained as it is basically same as that of the first embodiment.

10 Fig. 25B is a circuit diagram of the present embodiment, and Fig. 25C is a similar device obtained by the prior art, for the purpose of comparison. As will be apparent from the comparison of Fig. 25C representing the prior art and Fig. 25A representing the present invention, the layout area of the device can be significantly reduced by the use of the electrode structure of the present invention in the connecting part of the source area and the sub area in the inverter circuit.

15 Embodiment 3

20 A third embodiment of the present invention is illustrated in Figs. 26A and 26B, and in a circuit diagram in Fig. 26C. The producing process of the present embodiment will not be explained as it is basically same as that of the foregoing first embodiment.

25 The present third embodiment also provides a CMOS inverter, but is different from the second embodiment in that the MOS transistors have a vertical

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1 structure. As will be apparent from the illustrations,
the electrode structure of the present invention is
even more effective for reducing the layout area in a
circuit employing vertical MOS transistors.

5 Embodiment 4

A fourth embodiment of the present invention is
illustrated in Figs. 27A and 27B, and shown in a
circuit diagram in Fig. 27C. The producing process
of the present embodiment will not be explained, as it
10 is basically same as that of the foregoing first
embodiment.

In the present fourth embodiment, the present
invention is applied to a NAND circuit composed again
with vertical MOS transistors. As will be apparent
15 from the illustrations, the electrode structure of the
present invention is effective, also in this embodiment,
for reducing the layout area.

Embodiment 5

Fig. 28 is a schematic cross-sectional view of
20 a NOR circuit element constituting a fifth embodiment
of the present invention.

In Fig. 28 there are shown polysilicon gates
205, 207 respectively of PMOS and NMOS transistors;
gate insulation films 206, 208; a p⁺ drain layer 209
25 of the PMOS transistor; an n⁺ source layer 210 of the
NMOS transistor; and electrodes 211, 212, 213, 214
respectively for the drain 209, source 210, and

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1 polysilicon gates 205, 207. Also in this embodiment,
the source 53 of the PMOS transistor and the sources
201, 210 of the NMOS transistor are mutually
connected. At the NMOS side there is formed a buried
5 electrode 61 reaching the n^+ drain layer 203, and, at
the PMOS side, there is formed an electrode 211 for
the p^+ drain layer 59. These two electrodes 61, 211
are formed by selective deposition by the aforementioned
Al-CVD method. The structure shown in Fig. 28 can be
10 formed by steps similar to those shown in Figs. 6 to
17.

A first input terminal 215 of the NOR circuit
is connected to the gate 207 of the NMOS transistor and
the gate 205 of the PMOS transistor. A second input
15 terminal 216 of the NOR circuit is connected to the
common gate 55 of the NMOS and PMOS transistors.

The present device functions in the following
manner. When the first input terminal 215 receives a
voltage equal to or larger than V_{th} of the NMOS
20 transistor, for example a highest potential and the
second input terminal 216 receives a voltage equal to
or lower than [highest potential + V_{th} of PMOS
transistor], for example a lowest potential, a channel
is formed below the NMOS transistor, whereby the drain
25 203 and the source 210 thereof are connected and the
output terminal 217 is maintained at the lowest
potential. In the PMOS transistor in this state, the

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1 p^+ layer 101 and the source area 53 are connected
through the channel, but the source 53 is not connected
to the power supply since a channel is not formed between
the drain 209 and the p^+ layer 51. When the voltages
5 applied to the first and second input terminals 215,
216 are interchanged, the drain 203 and the source
201 of the NMOS transistor are connected through the
channel, whereby the output terminal is maintained at
the lowest potential. In this state the drain 209 and
10 the p^+ layer 51 of the PMOS transistor are connected
through the channel, but the source 53 is not connected
to the power supply, since a channel is not formed
between the source 53 and the p^+ layer 51 of the PMOS
transistor. Then, when the first and second input
15 terminals 215, 216 both receive a voltage equal to or
higher than V_{th} of the NMOS transistor, for example the
highest potential, a channel is formed below the NMOS
transistor, whereby the drain 203 is connected with the
sources 201, 210 through said channel and the output
20 terminal 217 is maintained at the lowest potential.
The source 53 is not connected to the power supply,
since a channel is not formed below the PMOS transistor.
Then, when the first and second input terminals 215, 216
both receive a voltage equal to or lower than [highest
25 potential + V_{th} of PMOS transistor], for example the
lowest potential, a channel is formed below the PMOS
transistor, whereby the source 53 is connected to

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- 1 the drain 209 through the p^+ layer 51 and the output
terminal 217 is maintained at the highest potential.
In this state the sources 201, 210 are not connected
to the power supply, since a channel is not formed
5 below the NMOS transistor.

The NOR function is achieved as explained above,
since the output terminal is maintained at the highest
potential only when the first and second input terminals
are given the lowest potential and at the lowest
10 potential in other combinations of the input potentials.

Also the present embodiment can reduce the
number of electrode and the dimension of the element,
as in the example shown in Fig. 5.

Embodiment 6

- 15 Fig. 29 is a schematic cross-sectional view of
a NAND circuit device constituting a sixth embodiment
of the present invention.

In Fig. 29, there are shown a p^+ source
layer 218 of the PMOS transistor, and an n^+ drain
20 layer 219 of the NMOS transistor. In the present
device, a buried electrode 60 reaching a p^+ drain
layer 51 is formed at the PMOS side, and an electrode
220 for the n^+ drain 219 is formed at the NMOS side.
Said electrode 220 is also formed by selective
25 aluminum deposition utilizing DMAH and hydrogen. The
structure shown in Fig. 29 can be prepared by steps
similar to those in Figs. 6 to 17.

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1 A first input terminal 221 of the NAND circuit
is connected to the gate 207 of the NMOS transistor
and the gate 205 of the PMOS transistor. A second
input terminal 222 of the NAND circuit is connected
5 to the common gate 55 of the NMOS and PMOS transistors.

The device of the present embodiment functions
in the following manner. When the first input terminal
221 receives a voltage equal to or higher than V_{th} of
the NMOS transistor, for example a highest potential,
10 and the second input terminal 222 receives a voltage
equal to or lower than [highest potential + V_{th} of
PMOS transistor], for example a lowest potential, a
channel is formed below the PMOS transistor whereby the
drain 51 and the source 53 thereof are connected and an
15 output terminal 223 is maintained at the highest
potential. In the NMOS transistor in this state, the
 n^+ layer 203 is connected with the drain 219 through
the channel, but the source 201 is not connected to
the power source since a channel is not formed between
20 the source 201 and the n^+ layer 203. When the voltages
applied to the first and second input terminals 221,
222 are interchanged, the drain 51 and the source 218
of the PMOS transistor are connected through the channel
whereby the output terminal 223 is maintained at the
25 highest potential. In this state the source 201 is not
connected to the power source since a channel is not
formed between the drain 219 and the n^+ layer 203 of

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1 the NMOS transistor. Then, when the first and second
input terminals both receive a voltage equal to or
lower than [highest potential + V_{th} of PMOS transistor],
for example the lowest potential, a channel is formed
5 below the PMOS transistor, whereby the drain 51 is
connected with the source 53, 218 through said channel
and the output terminal 223 is maintained at the highest
potential. In this state the source 201 is not
connected to the power source, since a channel is not
10 formed below the NMOS transistor. Then, when the first
and second input terminals both receive a voltage equal
to or higher than V_{th} of the NMOS transistor, for
example the highest potential, a channel is formed
below the NMOS transistor, whereby the drain 219 is
15 connected with the source 200 through the n^+ layer 203
and the output terminal is maintained at the lowest
potential. In this state the sources 53, 218 are not
connected to the power source, since a channel is not
formed below the PMOS transistor.

20 The NAND function is thus achieved, as the
output terminal is maintained at the lowest potential
only when the first and second input terminals are
given the highest potential, but is maintained at the
highest potential at other combinations of the input
25 potentials.

Also this NAND circuit device is provided with
a reduced number of electrodes and can therefore

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1 reduce the dimension of the device.

In the foregoing embodiments 5 and 6, similar advantages can be obtained even if the semiconductors of n- and p-type are interchanged.

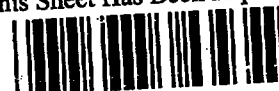
5 Similar advantages can be obtained also when the polysilicon electrode is replaced by a metal or silicide electrode.

As explained in the foregoing, the present invention allows to obtain a semiconductor device
10 provided with very small functional elements, which can be constructed by necessary minimum components without any unnecessary surface area, thereby being capable of significantly reducing the layout area and adapted for achieving a fine geometry and a high level
15 of integration.

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1 CLAIMS:

1. A semiconductor device provided with a first semiconductor area of a first conductive type and a second semiconductor area, formed on or under said first semiconductor area, of a second conductive type different from said first conductive type, wherein:

an electrode electrically connected to said first semiconductor area is formed through said second semiconductor area; and

10 said first and second semiconductor areas are electrically shortcircuited by said electrode.

2. A semiconductor device according to claim 1, wherein said second semiconductor area is a source or drain area of a field effect transistor.

3. A semiconductor device according to claim 2, wherein:

20 said field effect transistor includes a buried drain area and a buried gate area;

a PMOS transistor and an NMOS transistor are formed on respective sides of said buried gate;

said second semiconductor area constitutes said buried drain area; and

25 an electrode reaching said drain area is provided in at least either of said PMOS and NMOS transistors.

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1 4. A semiconductor device according to any of
claims 1 to 3, wherein said electrode is composed of
aluminum or a conductive material principally composed
of aluminum.

5

5. A semiconductor device according to claim
3, constituting a NOT circuit element.

10 6. A semiconductor device according to claim
3, constituting a NOR circuit element.

7. A semiconductor device according to claim
3, constituting a NAND circuit element.

15

8. A method for producing a semiconductor
device provided with a first semiconductor area of a
first conductive type, a second semiconductor area
formed on said first semiconductor area and having a
second conductive type different from said first
20 conductive type, and an electrode for short-circuiting
said first and second semiconductor areas, comprising:

a first step for forming an aperture in said
second semiconductor area thereby exposing a part of
said first semiconductor area; and

25

a second step for depositing a conductive
material in said aperture;

wherein said second step includes a step for

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- 1 depositing aluminum or a conductive material principally
composed of aluminum in said aperture by a CVD method
utilizing alkylaluminum hydride gas and hydrogen.
- 5 9. A method for producing a semiconductor device
according to claim 8, wherein said alkylaluminum hydride
is dimethylaluminum hydride.
- 10 10. A method for producing a semiconductor
device, comprising steps of:
forming buried drain areas of a PMOS transistor
and of a NMOS transistor on a semiconductor substrate;
forming an aperture so as to penetrate a junction
part of the drain area of said PMOS transistor and that
15 of said NMOS transistor;
forming an insulation film covering the internal
surface of said aperture;
depositing, in said aperture, a common gate for
said PMOS and NMOS transistors; and
20 forming a buried electrode reaching at least
either of the buried drain area of said PMOS transistor
and that of said NMOS transistor.
- 25 11. A method for producing a semiconductor
device according to claim 10, wherein said buried
electrode is formed by forming an aperture reaching
at least either of said two buried drain areas, and

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1 selectively depositing aluminum in said aperture by
a CVD method utilizing dimethylaluminum hydride and
hydrogen.

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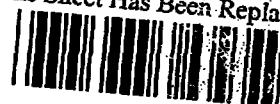
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ABSTRACT1 SEMICONDUCTOR DEVICE AND METHOD FOR PRODUCING THE SAME

There is provided a semiconductor device with very small functional elements, which can be constructed by necessary minimum components without any unnecessary surface area, thus being capable of significantly reducing the layout area and adapted for achieving a fine geometry and a high level of integration. The semiconductor device is provided with a first semiconductor area of a first conductive type (for example a p⁻ well) and a second semiconductor area formed on or under the first semiconductor area and having a second conductive type different from the first conductive type (for example a source or drain area), in which an electrode electrically connected to the first semiconductor area is formed through the second semiconductor area, and the first and second semiconductor areas are shortcircuited by the above-mentioned electrode.

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FIG. 1A

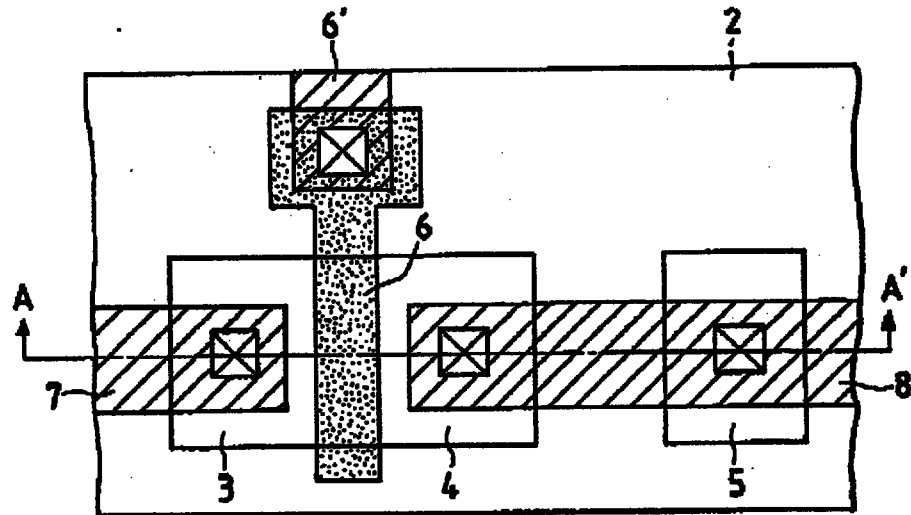
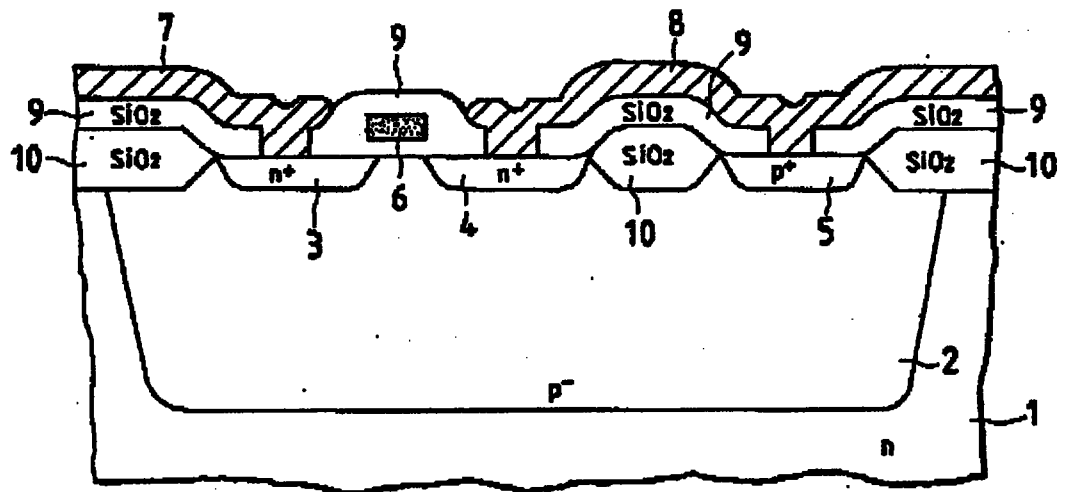


FIG. 1B



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FIG. 2A

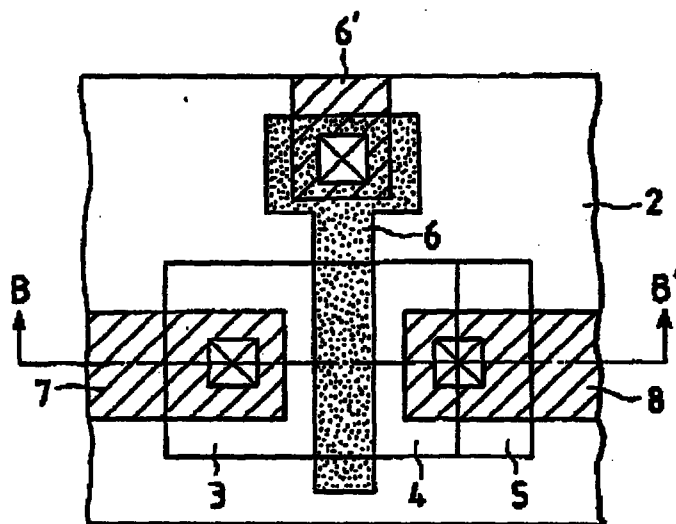
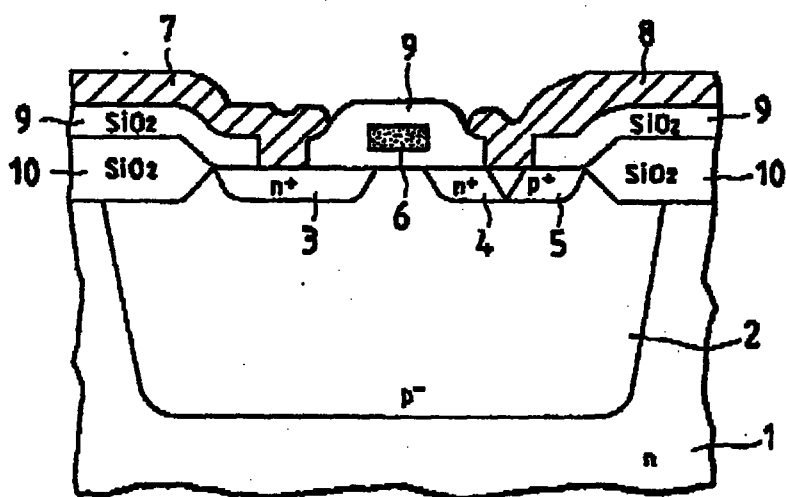


FIG. 2B



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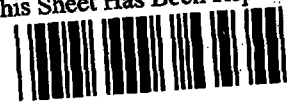
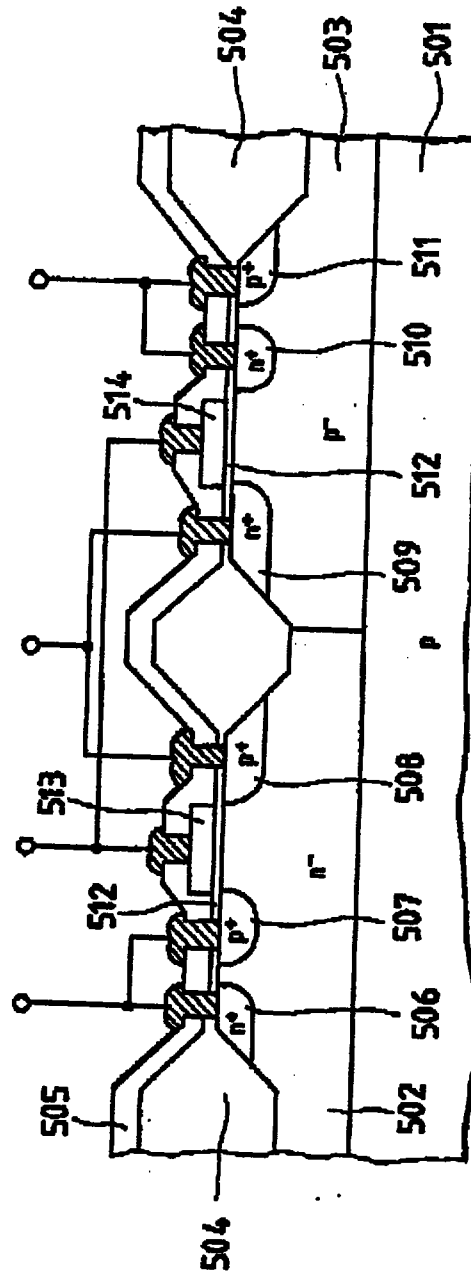


FIG. 3



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FIG. 4A

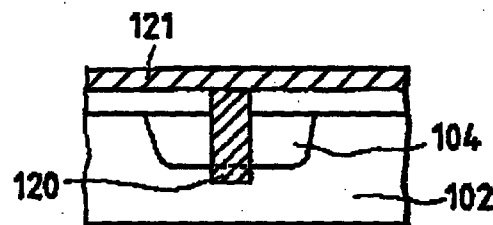


FIG. 4B

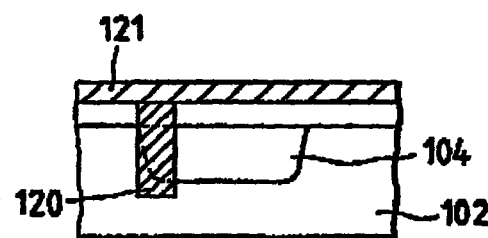


FIG. 4C

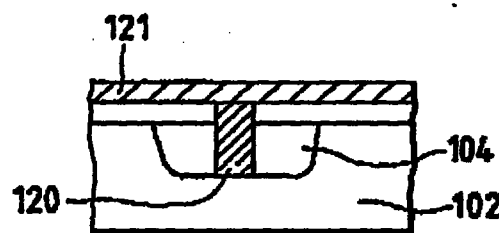


FIG. 4D

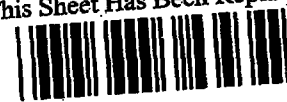
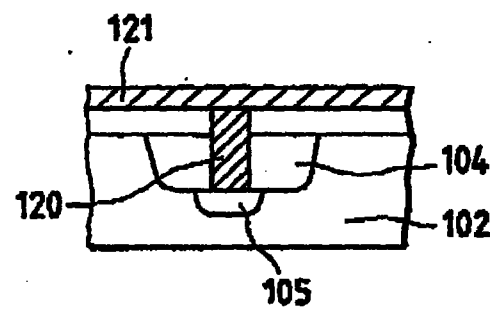


FIG. 5A

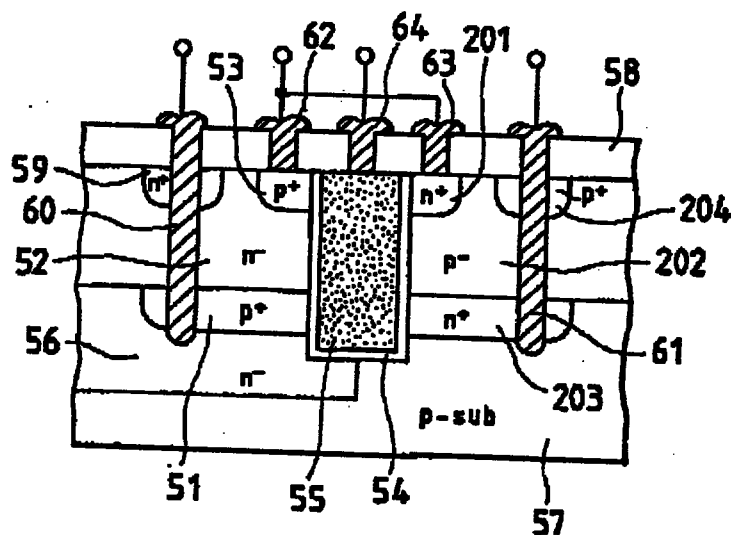


FIG. 5B

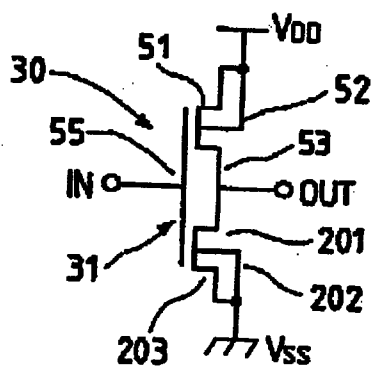


FIG. 6

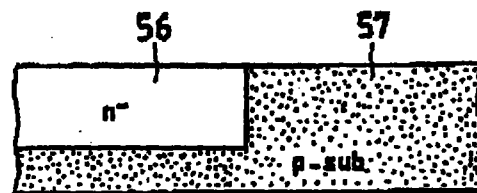


FIG. 7

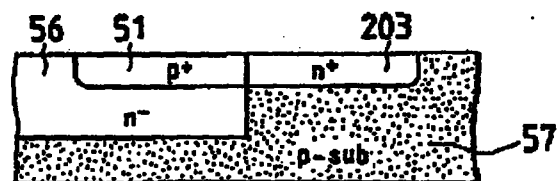


FIG. 8

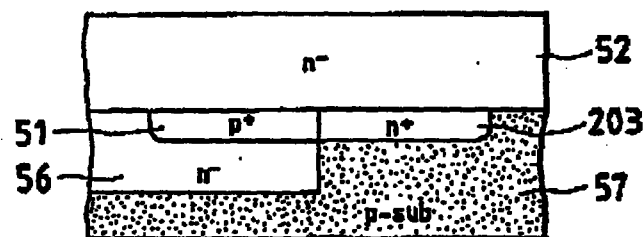


FIG. 9

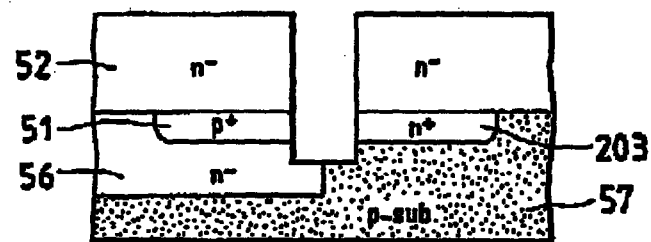


FIG. 10

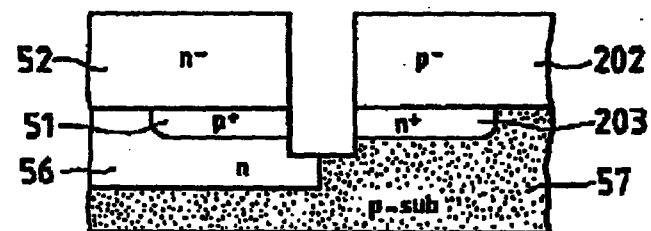
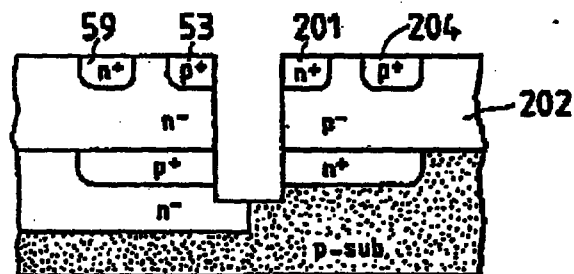


FIG. 11



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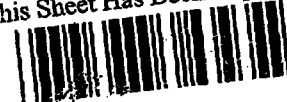


FIG. 12

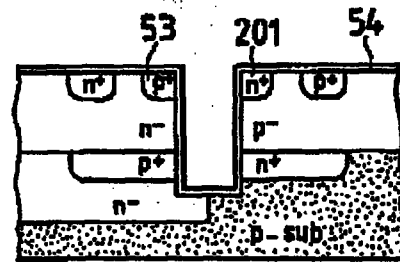


FIG. 13

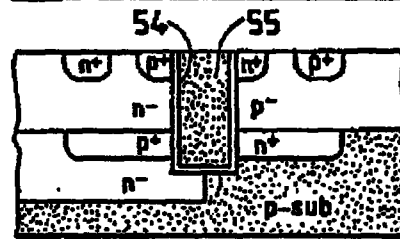


FIG. 14

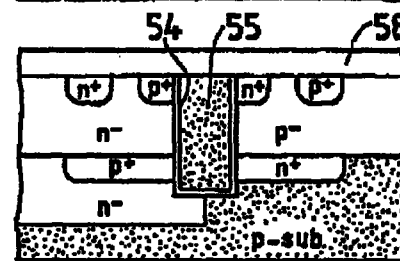


FIG. 15

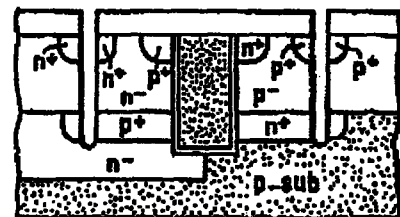


FIG. 16

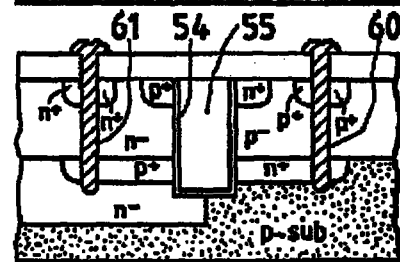


FIG. 17

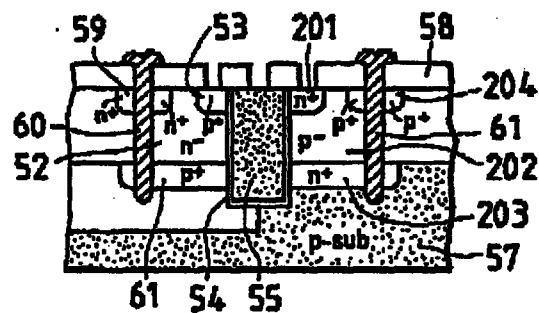


FIG. 18

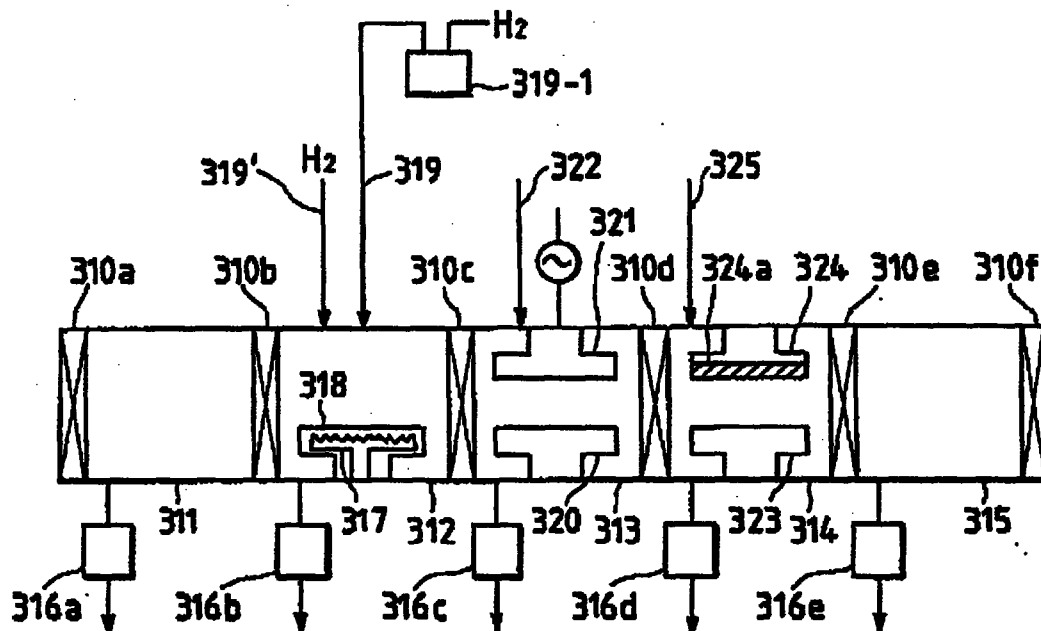
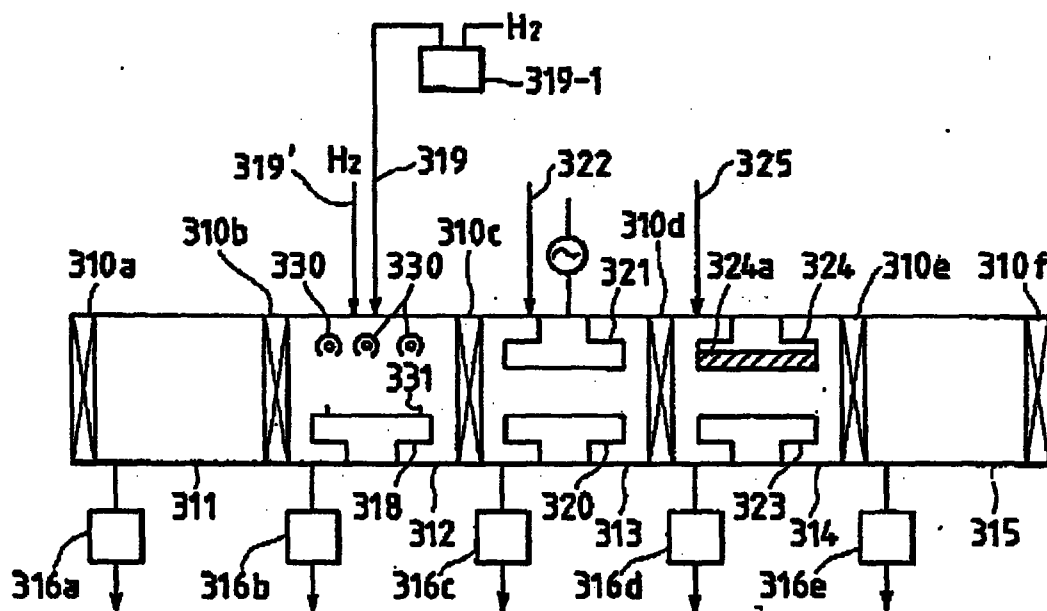


FIG. 19



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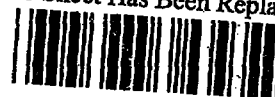


FIG. 20

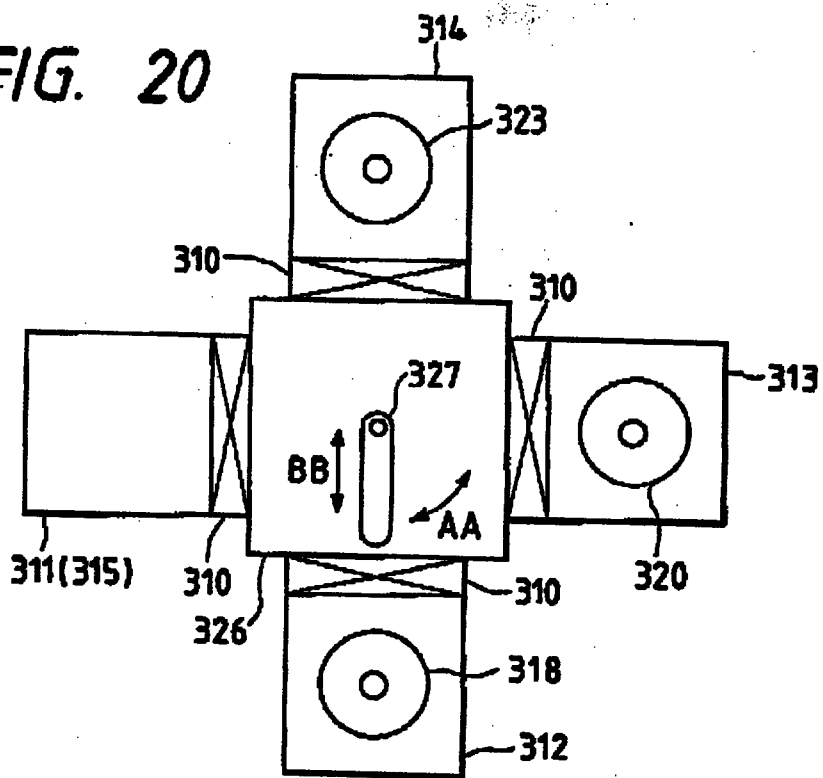


FIG. 21

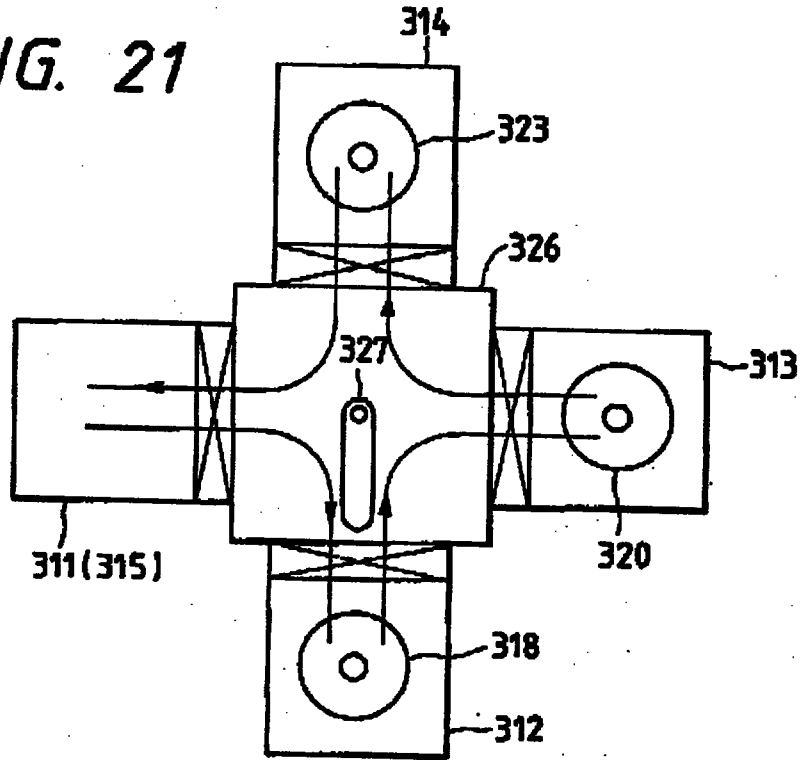


FIG. 22A

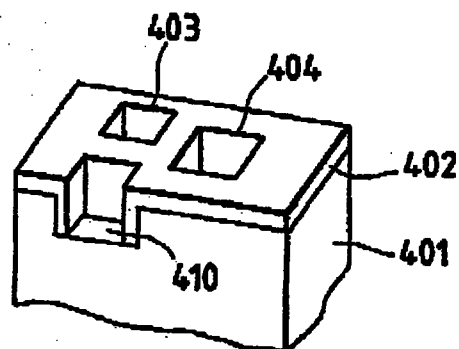


FIG. 22B

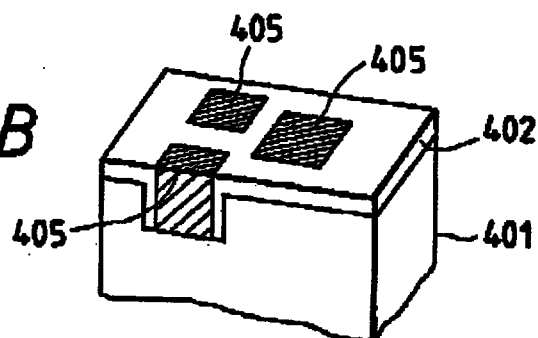
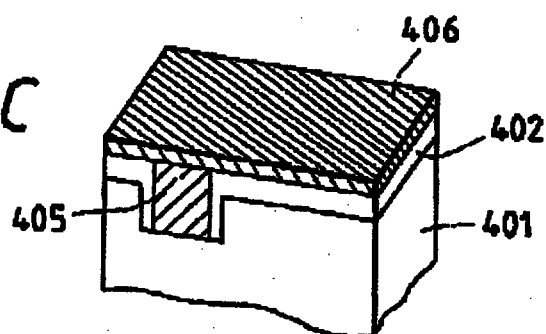


FIG. 22C



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FIG. 23A

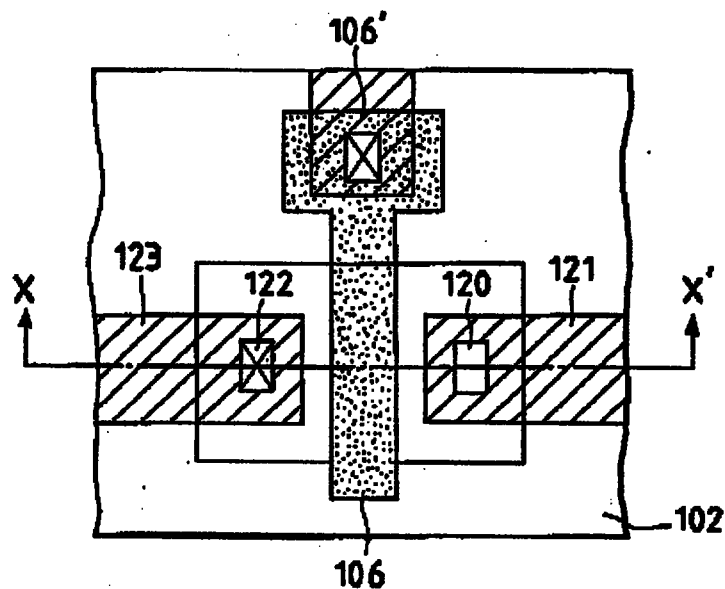
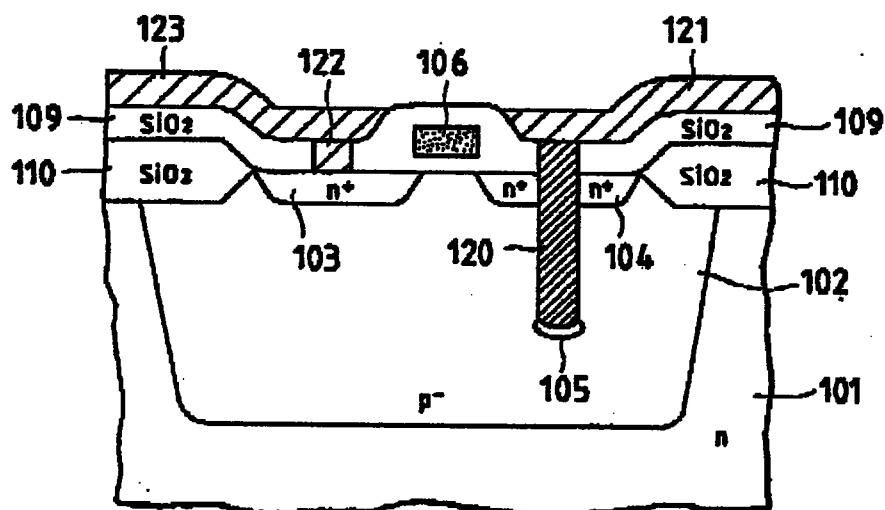


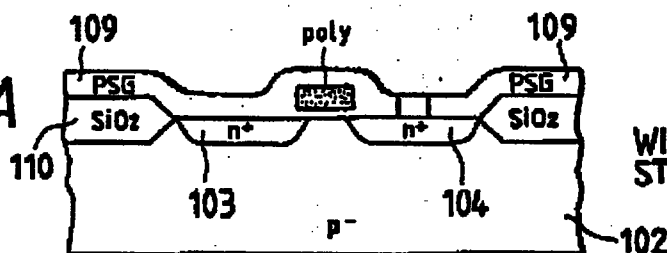
FIG. 23B



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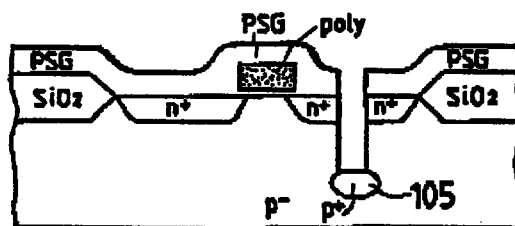


FIG. 24A



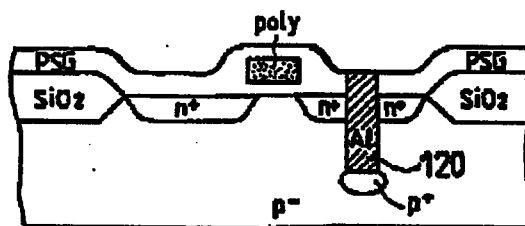
WINDOW FORMING STEP

FIG. 24B



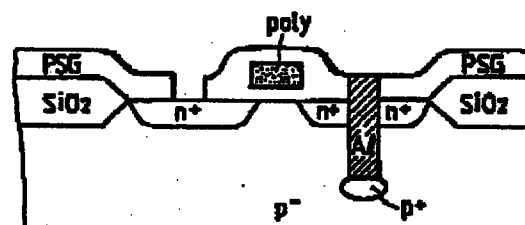
ETCHING PROCESS SHAPING STEP

FIG. 24C



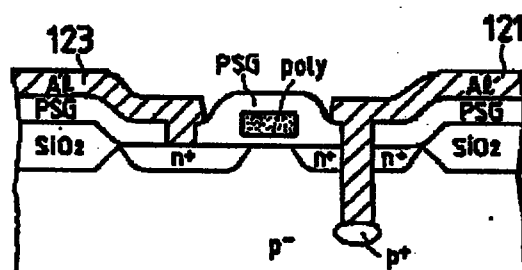
SHAPING STEP

FIG. 24D



WINDOW FORMING STEP

FIG. 24E



WIRING STEP

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FIG. 25A

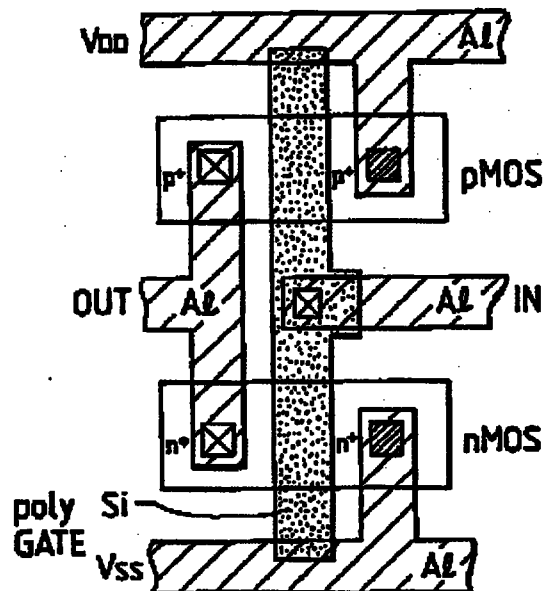


FIG. 25B

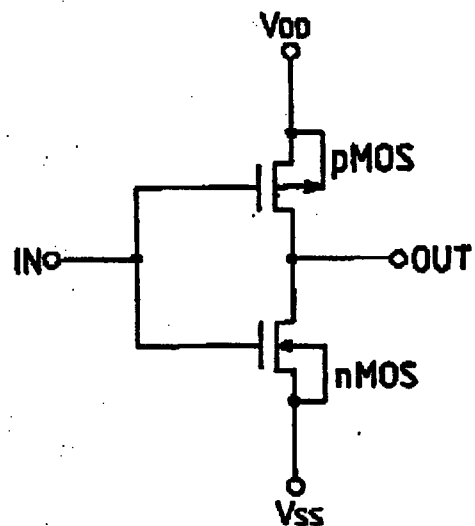
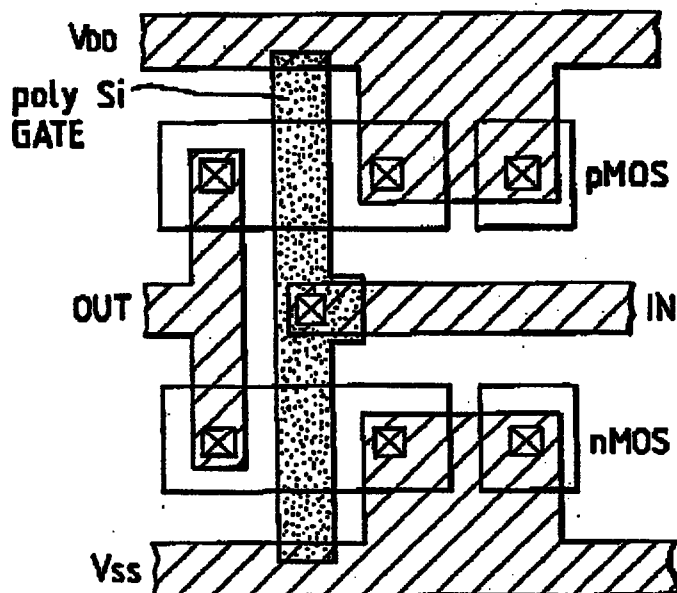


FIG. 25C



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FIG. 26A

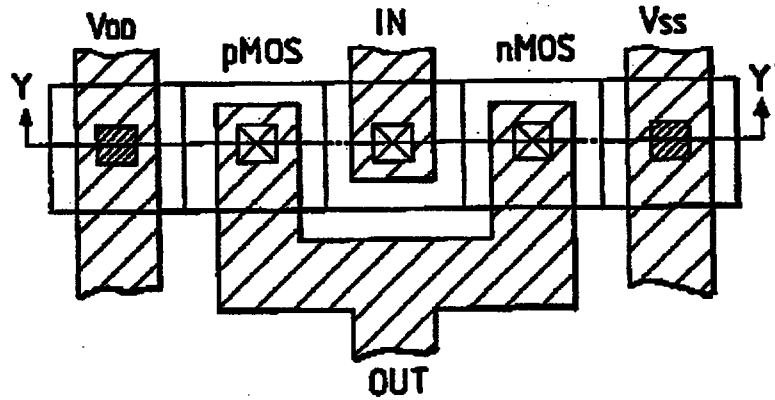


FIG. 26B

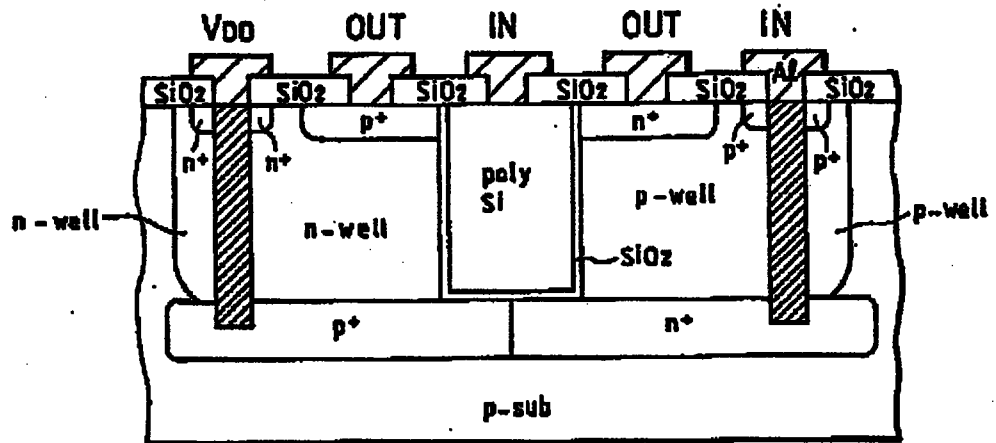
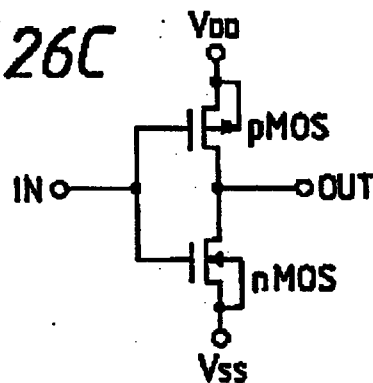


FIG. 26C



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FIG. 27A

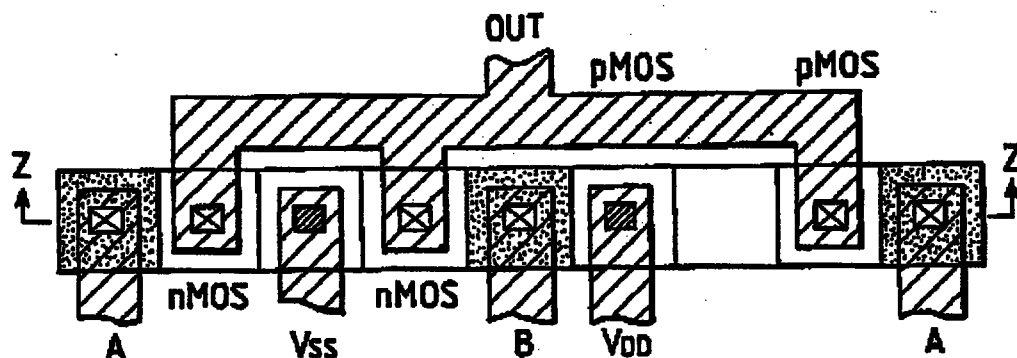


FIG. 27B

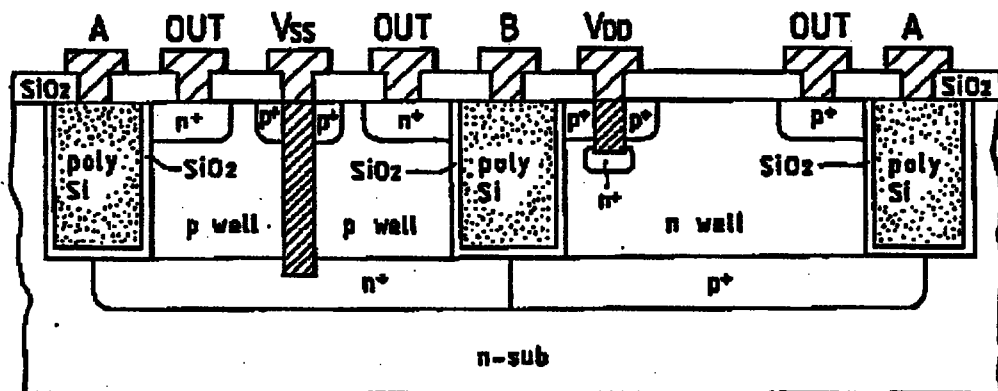
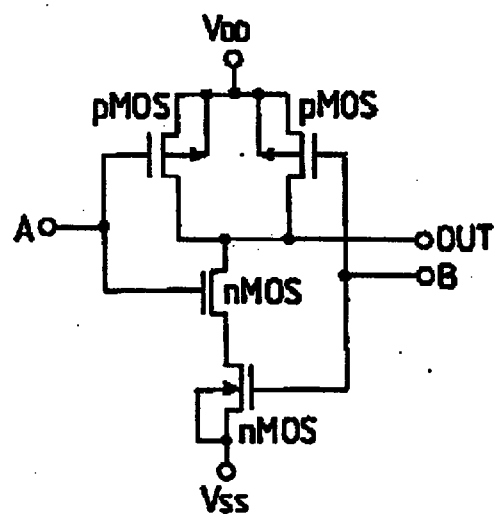


FIG. 27C



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FIG. 28

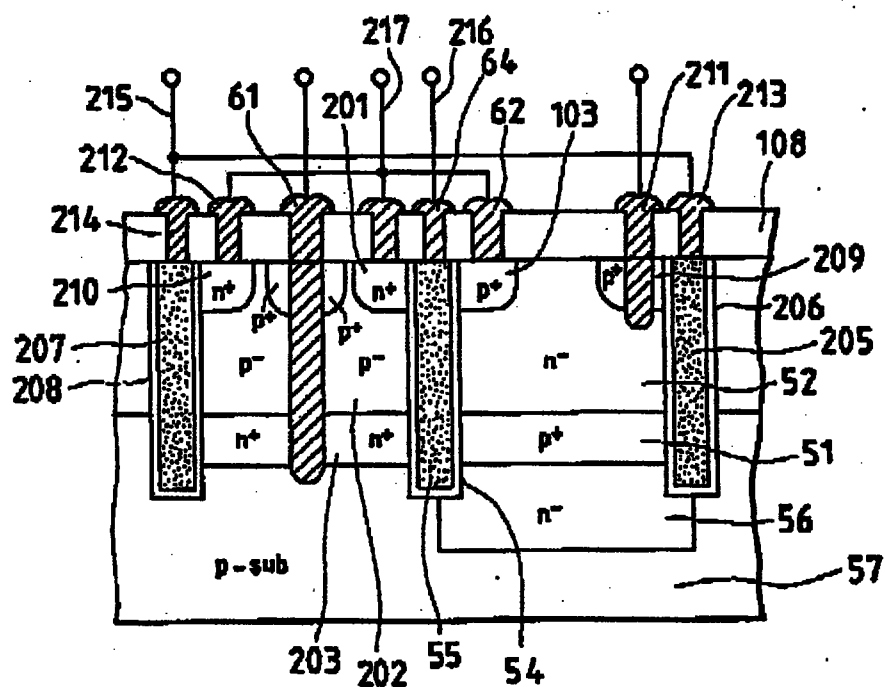
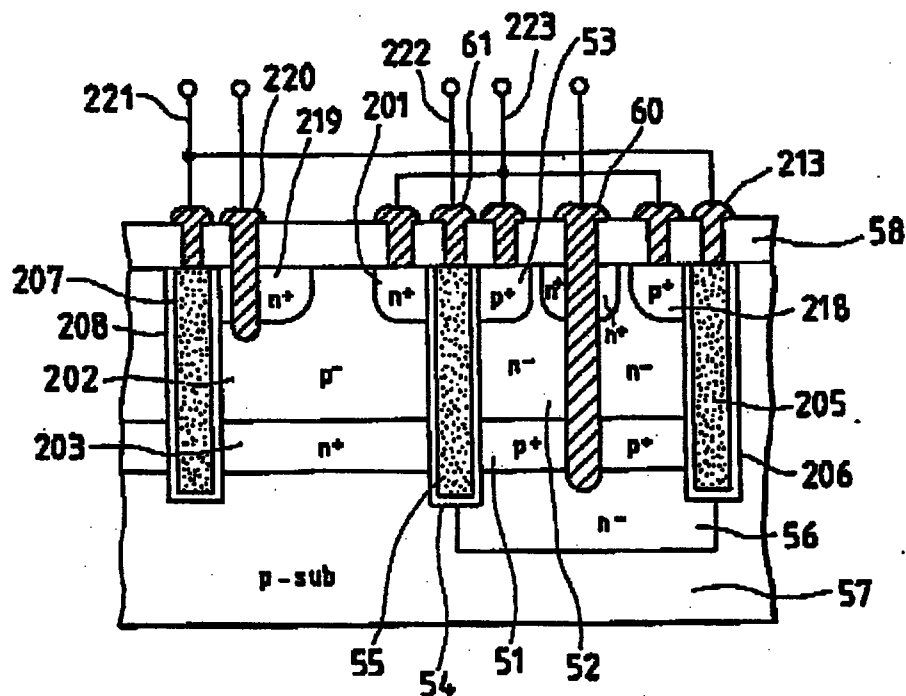


FIG. 29



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Semiconductor Device and Method
for Producing the Same

BACKGROUND OF THE INVENTION

Field of the Invention

The present invention relates to a semiconductor integrated circuit such as a memory, a photoelectric converting device, a signal processing device or the like adapted for use in various electronic appliances, and more particularly to a semiconductor device featured in the electrode structure of functional elements and a method for producing the same.

Related Background Art

For providing a highly integrated semiconductor circuit device, the development of miniaturized functional elements, such as a MOS transistor with a submicron gate length, is desired in recent years. As a specific example, a MOS transistor with a gate length of $0.8\text{ }\mu\text{m}$ occupies an area of ca. $20\text{ }\mu\text{m}^2$, suitable for a high level of integration.

However the higher level of integration achieved by the miniaturization of functional elements has not necessarily lead to the anticipated satisfactory characteristics. Such discrepancy has been considered attributable to the method for producing such functional elements, and the efforts to solve such drawback has inevitably been directed to the improvement in such

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producing method. Stated differently, the predominant perception has been that the preparation of a satisfactorily functioning element in stable and reproducible manner is an important factor for the improvement of production yield.

However, the detailed investigation of the present inventors on the element structure and on the producing method therefor has revealed that a novel structure in the electrodes and/or the wirings therefor can achieve a finer geometry and a higher level of integration, with improved performance. This fact will be explained in the following, taking a MOSFET and a planar CMOS transistor as examples.

Fig. 1A is a schematic plan view of an example of the conventional function element, and Fig. 1B is a schematic cross-sectional view along a line A-A' in Fig. 1A.

There are illustrated an n-type semiconductor substrate 1, and a p⁻-type semiconductor area (p⁻ well) 2, in which formed are a drain area 3 and a source area 4 both of an n⁺-type semiconductor, and a sub area 5 for ohmic connection of the p⁻ well 2 with an electrode. Above a channel area in the p⁻ well 2, there is provided a gate electrode 6 across a gate insulation film, and an n-channel MOSFET is thus formed. A drain electrode 7 and a source electrode 8 respectively contact with the drain area 3, and with the source and sub areas 4, 5

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through contact holes formed in an insulation layer 9.

Multi-terminal elements, such as functional elements, are often used with a fixed potential at a terminal. The above-explained MOSFET is used with the source and sub areas thereof maintained at a same potential. For this purpose, the sub area 5 is positioned horizontally next to the source area 4 across a field insulation film 10, and said source area 4 and sub area 5 are short-circuited by the source electrode 8 connected through the contact holes.

Such structure requires a plurality of field insulation films 10 and contact holes positioned in the horizontal direction, thus occupying a large area, and cannot achieve a sufficiently high level of integration even if a fine geometry can be realized.

For resolving the above-mentioned drawback, there is proposed a semiconductor device as shown in Figs. 2A and 2B, which are respectively a schematic plan view and a schematic cross-sectional view along a line B-B' in Fig. 2A. In this structure, the source area 4 and the sub area 5 are positioned in mutually contacting manner, thereby dispensing with the field insulation film therebetween and requiring only one contact hole for said two areas, instead of one contact hole for each area.

However, even in this structure, the horizontal positioning of the source area 4 and the sub area 5

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requires an excessive surface area. Also the contact hole requires a certain large diameter for achieving sufficient short-circuiting of the source area 4 and the sub area 5, so that the design freedom of the production process is difficult to increase.

In the following there will be explained an example of the planar CMOS transistor.

The logic circuit in an integrated circuit requires functional elements with features such as possibility for a high level of integration, a high-speed operation, a low power consumption etc., and the planar CMOS transistors are recently used as the elements meeting such requirements for constituting the logic circuit. Fig. 3 schematically illustrates the structure of an inversion logic circuit composed of conventional planar CMOS transistors.

On a p-type substrate 501, there are formed an n^- layer 502, a p^- layer 503, a LOCOS oxide film 504, and an interlayer insulation film 505. The PMOS transistor includes an n^+ layer 506 for obtaining the substrate potential, a p^+ drain layer 507 and a p^+ source layer 508, while the NMOS transistor includes an n^+ source layer 509, an n^+ drain layer 510 and a p^+ layer 511 for obtaining the substrate potential. There are further provided a gate oxide film 512, a gate electrode 513 for the PMOS transistor and a gate electrode 514 for the NMOS transistor.

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The drain 507 and the n^+ layer 506 of the PMOS transistor are given a highest potential, while the drain 510 and the p^+ layer 511 of the NMOS transistor are given a lowest potential. The gate electrodes 513, 514 of the PMOS and NMOS transistors are mutually connected by a metal wiring to constitute an input terminal, while the sources 508, 509 of said transistors are mutually connected by a metal wiring to constitute an output terminal, whereby an inversion logic circuit is constructed.

When a voltage equal to or higher than V_{th} of the NMOS transistor, for example the highest potential, is applied to the gate electrodes 513, 514, a channel is formed below the gate of the NMOS transistor, whereby the drain 510 and the source 509 are connected. Thus an electron current flows through said channel, thus maintaining the output terminal at the lowest potential.

Then, when a voltage equal to or lower than (highest potential + V_{th} of PMOS transistor), for example the lowest potential, is applied to the gate electrodes 513, 514, a channel is formed below the gate of the PMOS transistor, whereby the drain 507 and the source 508 thereof are connected. Thus a hole current flows through said channel, thus maintaining the output terminal at the highest potential.

The inverter function is thus realized, as the output terminal is maintained at the lowest or highest

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potential respectively when the highest or lowest potential is given to the input terminal.

In such conventional CMOS transistors, the device dimension is reduced by miniaturization of the gate length, contact holes and wiring width. However such conventional structure requires formation of gate areas on the surface, and isolation of the NMOS and PMOS transistors by a LOCOS oxide film, so that the device dimension has a limitation and a further reduction in size is difficult to achieve.

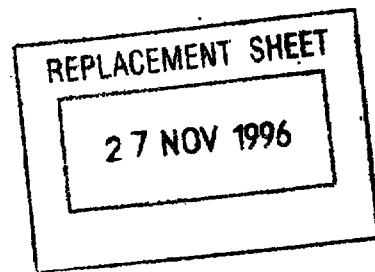
SUMMARY OF THE INVENTION

In consideration of the foregoing, an object of the present invention is to provide a semiconductor device suitable for achieving a fine geometry and a higher level of integration.

Another object of the present invention is to provide a semiconductor device including very small-sized functional elements.

Still another object of the present invention is to provide a semiconductor device in which the number of electrodes is reduced and the element isolation area can be reduced in size, that the dimension of the element can be further reduced.

Still another object of the present invention is to provide a method for producing a semiconductor device suitable for achieving a fine geometry and



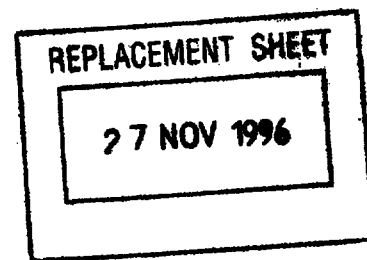
a higher level of integration.

Still another object of the present invention is to provide a method for producing a semiconductor device capable of filling a fine contact hole or a fine, deep trench, thereby realizing satisfactory electrical connection.

Still another object of the present invention is to provide a method for producing a semiconductor device, capable of significantly improving the electrical characteristics of the above-mentioned semiconductor device and of improving the production yield.

For attaining the above-mentioned objects, the present invention is featured by the following structure. The semiconductor device of the present invention, provided with a first semiconductor area of a first conductive type, and a second semiconductor area, formed on said first semiconductor area, of a second conductive type different from said first conductive, is featured by facts that an electrode electrically connected to said first semiconductor area is formed through said second semiconductor area, and that said first and second semiconductor areas are electrically short-circuited by said electrode.

The above-explained structure is additionally featured by facts that said second semiconductor area is a source or drain area of a field effect transistor,



and that said electrode is composed of aluminum or a conductive material principally composed of aluminum.

Said structure is further featured by facts that the field effect transistor has a buried drain area and a buried gate area, that a PMOS transistor and an NMOS transistor are formed on respective sides of said buried gate, that said second semiconductor area constitutes said buried drain area, and that said electrode reaching the drain area is provided in at least either of said PMOS and NMOS transistors.

Said structure is further featured by a fact that said electrode is composed of aluminum or a conductive material principally composed of aluminum.

An additional feature is that said semiconductor device is a NOT circuit element, a NOR circuit element or a NAND circuit element.

Also the semiconductor device producing method of the present invention is featured by a first step for forming an aperture in said second semiconductor area thereby exposing a part of said first semiconductor area, and a second step for depositing a conductive material in said aperture, wherein said second step is to deposit aluminum or a conductive material principally composed of aluminum into said aperture by a CVD method utilizing alkylaluminum hydride gas and hydrogen.

Said method is further featured by a fact that said alkylaluminum hydride is dimethylaluminum hydride.

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The semiconductor device producing method of the present invention is furthermore featured by:

a step for burying drain areas of PMOS transistor and an NMOS transistor in a semiconductor substrate;

a step for forming an aperture so as to penetrate the junction portion between the drain area of said PMOS transistor and the drain area of said NMOS transistor;

a step for forming an insulation film covering the internal surface of said aperture;

a step for depositing, in said aperture, a common gate for said PMOS and NMOS transistors; and

a step for forming a buried electrode reaching at least either of the buried drain area of said PMOS transistor and the buried drain area of said NMOS transistor.

Said method is further featured by a fact that said buried electrode is formed by formation of an aperture reaching at least either of said two buried drain areas, and by selective deposition of aluminum in said aperture by a CVD method utilizing dimethylaluminum hydride and hydrogen.

The present invention can provide a semiconductor device including very small functional elements which can be formed with necessary minimum components without unnecessary planar areas, thereby being capable of

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significantly reducing the layout area and adapted for achieving a fine geometry and a high level of integration.

Also the present invention allows to reduce the number of electrodes and reduce the element isolation area in size, thereby further decreasing the dimension of the element.

Furthermore, the present invention utilizes aluminum electrode formation by low-temperature aluminum deposition by a CVD method utilizing alkylaluminum hydride gas and hydrogen, thereby significantly improving the electrical characteristics and the production yield.

BRIEF DESCRIPTION OF THE DRAWINGS

Figs. 1A and 1B illustrate an example of the conventional semiconductor device, wherein Fig. 1A is a schematic plan view thereof and Fig. 1B is a schematic cross-sectional view along a line A-A' in Fig. 1A;

Figs. 2A and 2B illustrate another example of the conventional semiconductor device, wherein Fig. 2A is a schematic plan view thereof and Fig. 2B is a schematic cross-sectional view along a line B-B' in Fig. 2A;

Fig. 3 is a schematic cross-sectional view of a conventional CMOS transistor;

Figs. 4A, 4B, 4C and 4D are cross-sectional views showing features of the semiconductor device of

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the present invention and illustrating variations thereof;

Fig. 5A is a cross-sectional view of a preferred embodiment of the present invention;

Fig. 5B is an equivalent circuit diagram thereof;

Figs. 6 to 17 are views showing steps for producing the structure shown in Fig. 5;

Figs. 18 to 20 are schematic views of continuous metal film forming apparatus suitable for forming a CVD-Al film or a metal film principally composed of aluminum;

Fig. 21 is a view showing the function of the apparatus shown in Fig. 20;

Figs. 22A, 22B and 22C are schematic perspective views showing film forming procedure for forming electrodes and wirings by the Al-CVD method;

Fig. 23A is a schematic plan view of a MOSFET constituting a first embodiment of the present invention;

Fig. 23B is a schematic cross-sectional view along an X-X' line in Fig. 23A;

Figs. 24A to 24E are schematic cross-sectional views showing the method for producing the MOSFET shown in Figs. 23A and 23B;

Fig. 25A is a schematic cross-sectional view of a semiconductor device, constituting a second embodiment of the present invention and applied to a CMOS inverter

circuit;

Fig. 25B is a circuit diagram of said embodiment;

Fig. 25C is a schematic cross-sectional view of a device by the prior art, as a comparative example to the above-mentioned embodiment;

Fig. 26A is a schematic plan view of a semiconductor device constituting a third embodiment of the present invention and applied to a CMOS inverter circuit;

Fig. 26B is a schematic cross-sectional view along a line Y-Y' in Fig. 26A;

Fig. 26C is a circuit diagram of said embodiment;

Fig. 27A is a schematic plan view of a semiconductor device constituting a fourth embodiment of the present invention and applied to a NAND circuit composed of vertical MOS transistors;

Fig. 27B is a schematic cross-sectional view along a line Z-Z' in Fig. 27A;

Fig. 27C is a circuit diagram of said embodiment;

Fig. 28 is a schematic cross-sectional view of a fifth embodiment of the present invention; and

Fig. 29 is a schematic cross-sectional view of a sixth embodiment of the present invention.

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DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

Now the present invention will be clarified in detail by preferred embodiments thereof.

A preferred embodiment of the present invention is constructed in the following manner. In functional elements such as field effect transistor, bipolar transistor, diffusion resistor etc., terminals to be used in an electrically short-circuited state are formed by forming, on a first semiconductor area of a first conductive type, a second semiconductor area of a second conductive type, and forming an electrode contacting said first semiconductor area through said second semiconductor area.

Figs. 4A to 4D are schematic cross-sectional views showing various modes of the present invention.

In an example shown in Fig. 4A, there is formed an electrode 120 which reaches a first semiconductor area 102, penetrating the center of a second semiconductor area 104.

In an example shown in Fig. 4B, the electrode 120 reaches the first semiconductor area 102 through an end portion of the second semiconductor area 104.

In an example shown in Fig. 4C, the electrode 120 does not sink into the first semiconductor area 102, as in the case of Fig. 4A, but merely contacts the upper surface thereof. 121 indicates a source electrode wiring.

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Figs. 4A to 4C do not show the sub area. Such sub area can be dispensed with if the material of the electrode 120 can make ohmic contact with the first semiconductor area 102. If necessary, a sub area 105 may be formed, as shown in Fig. 4D, at a position where the electrode contacts the first semiconductor area 102. The electrode 120 is preferably provided with an insulation film on a large part of the lateral wall thereof and contacts the area 104 through a silicon area exposed in said insulation film.

Fig. 5A is a schematic cross-section view of another embodiment of the present invention, and Fig. 5B is an equivalent circuit diagram thereof.

In Fig. 5A there are shown a p-type substrate 57, an n^- diffusion layer 56, a buried drain area 51 of a PMOS transistor, a channel area 52 of the PMOS transistor, a source area 53 thereof, a gate oxide film 54 common for PMOS and NMOS transistor, a polysilicon gate 55, an insulation film 58, a source area 201 of an NMOS transistor, a channel area 202 thereof, a buried drain area 203 thereof, a buried electrode 60 common for the drain and well of the PMOS transistor, a buried electrode 61 common for the drain and well of the NMOS transistor, source electrodes 62, 63 respectively of the PMOS and NMOS transistors, and a common gate electrode 64.

As shown in the equivalent circuit in Fig. 5B,

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a highest potential is given to the drain 51 and the well 52 of the PMOS transistor 30, while a lowest potential is given to the drain 203 and the well 202 of the NMOS transistor 31. The common gate 55 of the PMOS and NMOS transistors constitutes an input terminal, while the sources 53, 201 of the PMOS and NMOS transistors are mutually connected to constitute an output terminal, whereby an inversion logic circuit is constituted. When the highest potential is applied to the input terminal, the NMOS transistor 31 is rendered conductive to provide the output terminal with the lowest potential. When the lowest potential is applied to the input terminal, the PMOS transistor 30 is rendered conductive to provide the output terminal with the highest potential. The inversion logic operation is thus realized.

In the present invention, as shown in Fig. 5A, fine buried electrodes 60, 61 are buried deep into the semiconductor substrate. In the prior art, it has been difficult to fill, even a contact hole of a large aspect ratio, completely with a conductive material, and it has been impossible to form a deep buried electrode as shown in Fig. 5A by metal deposition.

The present invention is based on a finding that a metal of satisfactory quality can be deposited with extremely good selectivity by a novel CVD method

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to be explained later.

In the following there will be explained the process for producing the CMOS transistor shown in Fig. 5, with reference to Figs. 6 to 17.

At first, in the p-type substrate 57, the n^- diffusion layer 56 was formed by ion implantation and an annealing step (Fig. 6).

Then the n^+ drain layer 203 in the substrate 57 and the p^+ drain layer 51 in the n^- layer 56 were formed respectively by ion implantation and annealing (Fig. 7).

The n^- layer 52 was subsequently formed over the entire surface by CVD (Fig. 8).

Then an etching process was conducted to form an aperture penetrating the n^- layer 52, p^+ layer 51 and n^+ layer 203 and reaching the n^- layer 56 (Fig. 9).

Ion implantation was conducted in an area for forming the NMOS transistor in the n^- layer, followed by annealing, to form the p^- layer 202 (Fig. 10).

Then the p^+ source area 53 and the n^+ layer 59 for electrode connection were formed in the n^- layer 52, and the n^+ source area 201 and the p^+ area 204 for electrode connection were formed in the p^- layer 202, respectively by ion implantation and annealing (Fig. 11).

Then the gate oxide film 54 was formed by thermal oxidation (Fig. 12).

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Subsequently polysilicon was deposited in the aperture by CVD, followed by an etch-back process, to form the buried polysilicon layer (Fig. 13).

The interlayer insulation film 58 was deposited by CVD (Fig. 14), and the contact holes for the drains 51, 203 and the wells 52, 202 were formed by etching (Fig. 15).

Then Al was deposited in the contact holes by the above-mentioned CVD utilizing DMAH and H_2 , thereby forming the electrodes 60, 61 common for the drains and wells (Fig. 16).

Contact holes for the source and the gate were formed by etching (Fig. 17).

Finally Al was deposited in the contact holes by CVD, and the source electrodes 111, 112 and the gate electrode 63 were formed to complete the structure shown in Fig. 5A. The inversion logic circuit was formed by patterning the Al wirings in such a manner that the source electrodes of the PMOS and NMOS transistors are mutually connected.

When a voltage equal to or higher than V_{th} of the NMOS transistor, for example the highest potential, is applied to the gate electrode 55, a channel is formed below the gate of the NMOS transistor, whereby the drain 203 and the source 201 thereof are connected. Thus an electron current flow through said channel to maintain the output terminal at the lowest potential.

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Then, when a voltage equal to or lower than (highest potential + V_{th} of PMOS transistor), for example the lowest potential, is applied to the gate electrode 55, a channel is formed below the PMOS transistor, whereby the drain 51 and the source 53 thereof are connected. Thus a hole current flows through said channel to maintain the output terminal at the highest potential.

Thus the inverter operation is realized, as the output terminal is maintained at the lowest or highest potential respectively when the input terminal is given the highest or lowest potential.

The present embodiment can be constructed with only one gate electrode, and does not require an isolation area, as the gate serves to separate the PMOS and NMOS transistors. It is therefore rendered possible to reduce the number of electrodes and to reduce the isolation area in size, thereby obtaining a logic circuit of a reduced dimension.

The source electrodes 62, 63 and the gate electrode 64 may be composed, like the electrode 120 in the aforementioned first example or the buried electrodes 60, 61 in the second example, of polycrystalline silicon, Al, W, Mo, Cu, Al-Cu, Al-Cu, Al-Ti, Al-Si-Ti, Al-Si-Cu, WSi_2 , $MoSi_2$ or $TiSi_2$, but, in consideration of the production process, they are preferably composed of aluminum or a material

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principally composed of aluminum such as Al-Si, Al-Cu, Al-Ti, Al-Si-Ti or Al-Si-Cu. Besides such material is preferably deposited by a depositing method to be explained in the following.

(Film forming method)

In the following there will be explained a film forming method suitable for electrode formation according to the present invention.

Said method is adapted for filling an aperture with a conductive material, for forming the electrode of the above-explained structure.

Said film forming method consists of forming a deposited film by a surface reaction on an electron donating substrate, utilizing alkylaluminum hydride gas and hydrogen gas (said method being hereinafter called Al-CVD method).

An aluminum film of satisfactory quality can be deposited by heating the surface of the substrate in the presence of a gaseous mixture particularly consisting of monomethylaluminum hydride (MMAH) or dimethylaluminum hydride (DMAH) as the raw material gas and hydrogen as the reaction gas. At the selective Al deposition, the substrate surface is preferably maintained at a temperature at least equal to the decomposition temperature of alkylaluminum hydride but lower than 450°C, more preferably between 260°C and 440°C, by direct or indirect heating.

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The heating of the substrate in the above-mentioned temperature range may be achieved by direct or indirect heating, but formation of an Al film of satisfactory quality can be achieved with a high deposition speed, particularly by direct heating. For example, with the more preferred temperature range of $260^{\circ} - 440^{\circ}\text{C}$, a satisfactory film can be obtained with a deposition speed of $300 - 5000 \text{ \AA}/\text{min}$. which is higher than in the resistance heating. Such direct heating (substrate being heated by direct transmission of energy from the heating means) can be achieved by heating with a lamp such as a halogen lamp or a xenon lamp. Also indirect heating may be achieved for example by resistance heating, conducted by a heat generating member provided in a substrate support member, for supporting the substrate to be subjected to film deposition, provided in a film depositing space.

This method, if applied to a substrate having both an electron donating surface area and an electron non-donating surface area, allows to form single crystal of aluminum with satisfactory selectively solely on the electron donating surface area. Such aluminum is excellent in all the properties required for the electrode/wiring material, including a low hillock frequency and a low alloy spike frequency.

This is presumably because the semiconductive

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or conductive surface constituting an electron donating surface can selectively develop an aluminum film of satisfactory quality and excellent crystalline character of said Al film excludes or significantly reduces the alloy spike formation etc. resulting from an eutectic reaction with the underlying silicon. Such Al film, when employed as an electrode of a semiconductor device, provides the advantages far exceeding the concept of the conventional Al electrode and not anticipated in the prior technology.

As explained above, the Al deposited in an aperture with an electron donating surface, for example an aperture formed in an insulating film and exposing the surface of a semiconductor substrate therein, has a monocrystalline structure. Besides said Al-CVD method can achieve selective deposition of following metal films principally composed of aluminum, with likewise satisfactory quality.

For example, the electrode may be formed by selective deposition of various conductive materials such as Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu by the use of a mixed gaseous atmosphere employing, in addition to alkylaluminum hydride gas and hydrogen, a suitable combination of:

Si-containing gas such as SiH_4 , Si_2H_6 , Si_3H_8 , $\text{Si}(\text{CH}_3)_4$, SiCl_4 , SiH_2Cl_2 or SiHCl_3 ;

Ti-containing gas such as TiCl_4 , TiBr_4 or

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$\text{Ti}(\text{CH}_3)_4$; and/or

Cu-containing gas such as copper bisacetylacetonate $\text{Cu}(\text{C}_5\text{H}_7\text{O}_2)_2$, copper bisdipyvaloylmethanite $\text{Cu}(\text{C}_{11}\text{H}_{19}\text{O}_2)_2$ or copper bishexafluoroacetylacetonate $\text{Cu}(\text{C}_5\text{HF}_6\text{O}_2)_2$.

Also since said Al-CVD method is excellent in selectivity and provides satisfactory surface characteristics on the deposited film, there can be obtained a metal film suitable and widely usable for the wirings of a semiconductor device, by employing a non-selective film forming method in a next deposition step to form a metal film composed solely or principally of aluminum not only on the selectively deposited aluminum film mentioned above but also on the SiO_2 insulation film.

Examples of such metal films include combinations of selectively deposited Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu and non-selectively deposited Al, Al-Si, Al-Ti, Al-Cu, Al-Si-Ti or Al-Si-Cu.

Said non-selective film deposition may be achieved by CVD other than the aforementioned Al-CVD, or by sputtering.

(Film forming apparatus)

In the following there will be explained a film forming apparatus suitable for the electrode formation according to the present invention.

Figs. 18 to 20 schematically illustrate a

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continuous metal film forming apparatus suitable for executing the film forming method explained above.

As shown in Fig. 2, said apparatus is composed of a loading chamber 311, a CVD reaction chamber (first film forming chamber) 312, an Rf etching chamber 313, a sputtering chamber (second film forming chamber) 314 and an unloading chamber 315, which are rendered sealable from the external atmosphere and mutually communicatable by means of gate valves 310a - 310f and can be respectively made vacuum or reduced in pressure by vacuum systems 316a - 316e. The loading chamber 311 is used for eliminating the atmosphere of substrate and replacing it with H_2 prior to the deposition, in order to improve the throughput. The next CVD reaction chamber 312, for selective deposition onto the substrate under normal or reduced pressure, is provided therein with a substrate holder 318 with a resistance heater 317 for heating the substrate surface subjected to film formation at least within a temperature range of $200^\circ - 450^\circ C$, and receives the raw material gas such as of alkylaluminum hydride, which is gasified by bubbling with hydrogen in a bubbler 319-1, through a raw material gas supply line 319, and hydrogen as the reaction gas through a gas line 319'. The Rf etching chamber 313, for cleaning (etching) of the substrate surface in Ar atmosphere after the selective deposition, is provided therein with a substrate holder 320 capable

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of heating the substrate at least within a range of 100° - 250°C and an Rf etching electrode line 321, and is connected to an Ar gas supply line 322. The sputtering chamber 314, for non-selective deposition of a metal film by sputtering in Ar atmosphere, is provided therein with a substrate holder 323 to be heated at least within a range of 200° - 250°C and a target electrode 324 for mounting a sputtering target 324a, and is connected to an Ar gas supply line 325. The final unloading chamber 315, for adjustment of the substrate after metal film deposition and prior to the exposure to the external atmosphere, is designed to be capable of replacing the atmosphere with N₂.

Fig. 19 shows another example of the continuous metal film forming apparatus, wherein same components as those in Fig. 18 are represented by same numbers. The apparatus in Fig. 19 is different from that in Fig. 18 in that the substrate surface is directly heated by halogen lamps 330, and, for this purpose, the substrate holder 312 is provided with projections 331 for supporting the substrate in a floating state.

Direct heating of the substrate surface with such structure further increases the deposition speed as explained before.

The continuous metal film forming apparatus of the above-explained structure is equivalent, in practice, to a structure shown in Fig. 20, in which

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the loading chamber 311, CVD reaction chamber 312, Rf etching chamber 313, sputtering chamber 314 and unloading chamber 315 are mutually combined by a transport chamber 326. In this structure, the loading chamber 311 serves also as the chamber 315. In said transport chamber 326, there is provided an arm 327 constituting transport means, rotatable in both directions A-A and extendable and retractable in direction B-B, whereby the substrate can be transferred in succession from the loading chamber 311 to the CVD reaction chamber 312, Rf etching chamber 313, sputtering chamber 314, and finally to the unloading chamber 315 without exposure to the external atmosphere, as indicated by arrows in Fig. 21.

(Film forming process)

Now there will be explained the film forming process for forming the electrodes and wirings according to the present invention.

Fig. 22 illustrates the film forming procedure for forming the electrodes and wirings according to the present invention, in schematic perspective views.

At first the outline of the procedure will be described. A semiconductor substrate with an insulating film having apertures therein is placed in the film forming chamber, and the surface thereof is maintained for example at 250° - 450°C. Thermal CVD conducted in a mixed atmosphere of DMAH gas as alkylaluminum hydride and hydrogen gas causes selective deposition of Al on

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the semiconductor exposed in the apertures. There may naturally be conducted selective deposition of a metal film principally composed of Al, for example Al-Si, by introduction for example of Si-containing gas, as explained before. Then a metal film composed solely or principally of Al is non-selectively formed by sputtering, on the selectively deposited Al and on the insulation film. Subsequently the non-selectively deposited metal film is patterned into the shape of desired wirings, thereby obtaining the electrodes and the wirings.

This procedure will be explained in greater detail with reference to Figs. 19 and 22. At first prepared is a substrate, consisting for example of a monocrystalline silicon wafer bearing thereon grooves of different sizes, and covered by an insulation film except for the bottoms of said grooves.

Fig. 22A schematically shows a part of said substrate, wherein shown are a monocrystalline silicon substrate 401 constituting a conductive substrate; a thermal silicon oxide film 402 constituting an insulation film; apertures 403, 404 of different sizes; and a groove 410.

The formation of Al film, constituting a first wiring layer, on the substrate is conducted in the following manner, with the apparatus shown in Fig. 19.

At first the above-explained substrate is

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placed in the loading chamber 311, in which a hydrogen atmosphere is established by introduction of hydrogen as explained before. Then the reaction chamber 312 is evacuated by the vacuum system 316b approximately to 1×10^{-8} Torr, though Al film formation is still possible with a higher pressure.

Then DMAH gas obtained by bubbling is supplied from the gas line 319, utilizing H_2 as the carrier gas.

Also hydrogen as the reaction gas is introduced from the second gas line 319', and the interior of the reaction chamber 312 is maintained at a predetermined pressure, by the adjustment of an unrepresented slow leak valve. A typical pressure is about 1.5 Torr. DMAH is introduced into the reaction chamber from the DMAH line, with a total pressure of about 1.5 Torr and a DMAH partial pressure of about 5.0×10^{-3} Torr. Then the halogen lamps 330 are energized to directly heat the wafer, thereby causing selective Al deposition.

After a predetermined deposition time, the DMAH supply is interrupted. Said deposition time is so selected that the Al film on Si (monocrystalline silicon substrate 1) becomes equally thick as SiO_2 (thermal silicon oxide film 2), and can be experimentally determined in advance.

In this process, the substrate surface is heated to ca. $270^\circ C$ by direct heating, and the procedure

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explained above causes selective deposition of an Al film 405 in the aperture, as shown in Fig. 22B.

The foregoing is called a first film forming step for forming an electrode in an aperture.

After said first film forming step, the CVD reaction chamber 312 is evacuated, by the vacuum system 316b, to a pressure not exceeding 5×10^{-3} Torr. Simultaneously the Rf etching chamber 313 is evacuated to a pressure not exceeding 5×10^{-6} Torr. After confirmation of said evacuations of the chambers, the gate valve 310c is opened, then the substrate is moved from the CVD reaction chamber 312 to the Rf etching chamber 313 by the transport means, and said gate valve is closed. The Rf etching chamber 313 is evacuated to a pressure not exceeding 10^{-6} Torr, and is then maintained in argon atmosphere of $10^{-1} - 10^{-3}$ Torr by argon supply from the supply line 322. The substrate holder 320 is maintained at ca. 200°C, and an Rf power of 100 W is supplied to the Rf etching electrode 321 for about 60 seconds to generate an argon discharge in said chamber 313, whereby the substrate surface is etched with argon ions and the unnecessary surfacial layer of the CVD deposition film can be eliminated. The etch depth in this case is about 100 Å, corresponding to the oxide film. Said surface etching, of the CVD deposition film, conducted in the Rf etching chamber, may be dispensed with since said

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surfacial layer is free from oxygen etc. as the substrate is transported in vacuum. In such case, the Rf etching chamber 313 may serve for varying the temperature within a short time if the temperature is significantly different between the CVD reaction chamber 312 and the sputtering chamber 314.

After said Rf etching, the argon supply is terminated, and the Rf etching chamber 313 is evacuated to 5×10^{-6} Torr. Then the sputtering chamber is also evacuated to 5×10^{-6} Torr or lower, and the gate valve 310d is opened. The substrate is transferred from the Rf etching chamber 313 to the sputtering chamber 314 by the transport means, and said gate valve 310d is closed.

Subsequently the sputtering chamber is maintained at argon atmosphere of $10^{-1} - 10^{-3}$ Torr as in the Rf etching chamber 313, and the substrate holder 323 is maintained at $200^{\circ} - 250^{\circ}\text{C}$. Argon discharge is induced by a DC power of 5 - 10 kW to scrape the target of Al or Al-Si (Si: 0.5%) with argon ions, thereby depositing Al or Al-Si onto the substrate with a deposition speed of ca. $10000 \text{ \AA}/\text{min}$. This is a non-selective deposition step, and is called a second film forming step for forming wirings connected to the electrodes.

After the formation of the metal film of about $5000 \text{ \AA}$ on the substrate, the argon supply and the DC

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power application are terminated. The loading chamber 311 is evacuated to a pressure of 5×10^{-3} Torr or lower, then the gate valve 310e is opened and the substrate is moved. After the gate valve 310e is closed, the loading chamber 311 is supplied with nitrogen gas to the atmospheric pressure. Subsequently the gate valve 310f is opened and the substrate is taken out.

The second Al film deposition step explained above forms an Al film 406 on the SiO_2 film 402, as shown in Fig. 22C.

Subsequently said Al film 406 is patterned to obtain the wirings of desired shape.

(Experimental examples)

In the following there will be shown experimental results indicating the superiority of the above-explained Al-CVD method and the satisfactory quality of the Al film deposited by said method in the apertures.

There were prepared plural substrates, each consisting of an N-type monocrystalline silicon wafer, provided thereon with a thermally oxidized SiO_2 film of a thickness of 8000 Å, in which grooves of different sizes from $0.25 \times 0.25 \mu\text{m}$ to $100 \times 100 \mu\text{m}$ were formed by patterning to expose the underlying monocrystalline silicon (samples 1-1).

These samples were subjected to the Al film formation by the Al-CVD method, employing DMAH as

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the raw material gas and hydrogen as the reaction gas, with a total pressure of 1.5 Torr and a DMAH partial pressure of 5.0×10^{-3} Torr, and with the substrate surface temperatures selected in a range of 200° - 490°C by direct heating under the regulation of electric power supplied to the halogen lamps. The obtained results are summarized in Table 1.

Table 1

Substrate surface temp. (°C)	Deposition speed (A/min.)	Si linear defects	Carbon content	Resistivity (μΩcm)	Reflectance (%)	Hillock (> 1 μm) density (cm ⁻²)	Spike formation (%) destruction frequency of 0.15μm junction)
200	1000-1500	not observed	not detected	2.7 - 3.3	8.5 - 9.5	1 - 10 ²	0
230							
250							
260							
270							
280							
300	3000 - 5000			2.8 - 3.4	90 - 95	0 - 10	0 - 30
350							
400							
440							
450							
460					ca. 60	10 - 10 ⁴	
470							
480							
490							

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As will be apparent from Table 1, aluminum was deposited in the apertures with a deposition speed as high as 3000 - 5000 $\text{\AA}/\text{min}$. at the substrate surface temperature of 260°C or higher obtained by direct heating.

The Al film in the apertures, obtained in a substrate surface temperature range of 260° - 440°C, showed satisfactory characteristics, with no carbon content, a resistivity of 2.8 - 3.4 $\mu\Omega\text{cm}$, a reflectance of 90 - 95%, a hillock ($\geq 1 \mu\text{m}$) density of 0 - 10 cm^{-2} , and an almost zero spike formation (frequency of destruction of 0.15 μm junction).

On the other hand, though the film quality obtained in a surface temperature range of 200° - 250°C was somewhat inferior to that obtained in the temperature range of 260° - 440°C, it is considerably better than that obtainable with the conventional technology, but the deposition speed could not exceed 1000 - 1500 $\text{\AA}/\text{min}$.

At the substrate surface temperature equal to or higher than 450°C, the quality of the Al film in the apertures were deteriorated, with a reflectance of 60% or lower, a hillock ($\geq 1 \mu\text{m}$) density of 10 - 10⁴ cm^{-2} and an alloy spike formation of 0 - 30%.

In the following there will be explained how the above-explained method can be advantageously applied to the filling of the grooves.

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Said method can be advantageously applied to the grooves composed of the materials explained in the following.

The Al film formation was conducted on the following substrates (samples) under the same conditions as in the Al film formation on the above-mentioned samples 1-1.

Samples 1-2 were prepared by forming, on monocrystalline silicon constituting a first substrate surface material, a silicon oxide film constituting a second substrate surface material by means of CVD method, and forming grooves by a photolithographic process to locally expose the surface of monocrystalline silicon in the bottoms of said grooves. The thermal SiO_2 film was 8000 Å thick, and the exposed areas of monocrystalline silicon were sizes from $0.25 \times 0.25 \mu\text{m}$ to $100 \times 100 \mu\text{m}$, with a groove depth of $2 \mu\text{m}$. (Such samples will hereinafter be represented as "CVD SiO_2 (or simply SiO_2)/monocrystalline silicon".)

There were also prepared:

a sample 1-3 of boron-doped oxide film formed by normal pressure CVD (hereinafter written as BSG)/monocrystalline silicon;

a sample 1-4 of phosphor-doped oxide film formed by normal pressure CVD (PSG)/monocrystalline silicon;

a sample 1-5 of boron- and phosphor-doped oxide film formed by normal pressure CVD (BSPG)/monocrystalline

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silicon;

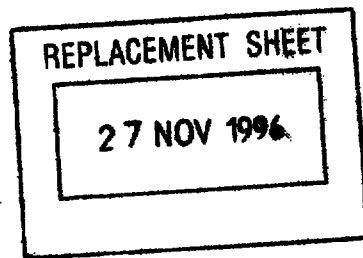
a sample 1-6 of nitride film formed by plasma CVD (P-SiN)/monocrystalline silicon;

a sample 1-7 of thermal nitride film (T-SiN)/monocrystalline silicon;

a sample 1-8 of nitride film formed by low pressure CVD (LP-SiN)/monocrystalline silicon; and

a sample 1-9 of nitride film formed by ECR (ECR-SiN)/monocrystalline silicon.

Further, samples 1-11 to 1-179 were prepared by taking all the combinations of the first surface materials of 18 kinds and the second surface materials of 9 kinds shown in the following. (It is to be noted that the sample numbers 1-10, 20, 30, 40, 50, 60, 70, 80, 90, 100, 110, 120, 130, 140, 150, 160 and 170 are lacking.) The first surface materials employed were monocrystalline silicon (mono-Si), polycrystalline silicon (poly-Si), amorphous silicon (a-Si), tungsten (W), molybdenum (Mo), tantalum (Ta), tungsten silicide (WSi), titanium silicide (TiSi), aluminum (Al), aluminum silicon (Al-Si), titanium aluminum (Al-Ti), titanium nitride (Ti-N), copper (Cu), aluminum silicon copper (Al-Si-Cu), aluminum palladium (Al-Pd), titanium (Ti), molybdenum silicide (Mo-Si), and tantalum silicide (Ta-Si). The second substrate surface materials employed were T-SiO₂, SiO₂, BSG, PSG, BPSG, P-SiN, T-SiN, LP-SiN and ECR-SiN. In all these samples, there could be



obtained satisfactory Al films comparable to those in the aforementioned samples 1-1.

Subsequently, the Al was non-selectively deposited by sputtering on the substrates subjected to the selective Al deposition as explained above, and was then patterned. Such deposited film is effective for three-dimensional connections of buried wirings.

The Al film obtained by sputtering and the selectively deposited Al film in the apertures showed electrically and mechanically satisfactory contact, because of the improved surface state of the Al film in the apertures.

Embodiment 1

In the following there will be explained a MOSFET constituting a first embodiment of the present invention.

Fig. 23A is a schematic plan view of a MOSFET of said first embodiment, and Fig. 23B is a schematic cross-sectional view along a line X-X' in Fig. 23A. There are shown a silicon substrate 101 of n-type semiconductor; a p^- well 102; a drain area 103 of n^+ type formed in the p^- well 102; a source area 104 formed similarly to the drain area 103; a p^+ sub area 105 for making ohmic contact between the p^- well 102 and the source electrode; a polycrystalline silicon gate electrode 106; a gate electrode wiring 106' connected to said gate electrode 106 by a through-hole; an

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insulation film 109 of silicon oxide; and a field insulation film 110 with bird's beak formed by selective oxidation.

An electrode 120, constituting the most characteristic structure of the present invention, is composed of monocrystalline aluminum, and penetrates the contact hole in the insulation layer 109 and the source area 104 and reaches the sub area 105 buried in the p^- well 102. A source electrode wiring 121, formed on the insulation layer 109 and the electrode 120, is composed of aluminum. A drain electrode 122, buried in the contact hole on the drain area 103, is composed of monocrystalline aluminum. There is also provided a drain electrode wiring 123.

In the following explained is the method for producing the MOSFET of the above-explained structure, with reference to Figs. 24A to 24E.

On the silicon substrate, there were conducted, by already known manufacturing process, formation of the p^- well 102, drain area 103, source area 104 and field insulation film 110, then formation of the insulation layer 109 thereon, and formation of the gate electrode 106 in said insulation layer 109. Then a photolithographic process utilizing photoresist was applied to form a hole, as a photoresist image, on the insulation layer 109 above the source area 104. Then dry etching with $CHF_3 - C_2F_6$ was conducted to form

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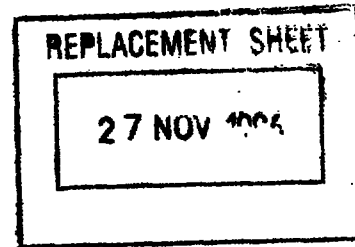
a hole in the insulation layer 109 down to the source area as shown in Fig. 24A (hole opening step).

Subsequently dry etching with Cl_2 - CBrF_3 was conducted without removal of the photoresist, thereby forming a hole penetrating the source area 104 and entering the p^- well 102 (etching step), and the sub area 105 was formed at the bottom of thus formed hole, as shown in Fig. 24B (p^+ forming step).

Then, as shown in Fig. 24C, aluminum was deposited to the upper surface of the insulation film 109 by the aforementioned Al-CVD method utilizing DMAH and hydrogen, with the substrate surface maintained at 270°C (CVD-Al forming step).

Then the contact hole is formed in the insulation layer 109 on the drain area 103 by a known process as shown in Fig. 24D (hole opening step), and aluminum was deposited by the above-mentioned Al-CVD method. The device was completed then by forming the source electrode wiring 121 and the drain electrode wiring 123 respectively on said electrode 102 and on the drain area 103 by sputtering as shown in Fig. 24E (Al wiring step).

As explained in the foregoing, the present invention allows to constitute a MOSFET, which is to be used with the source area and the sub area thereof in an electrically shortcircuited state, with necessary minimum components and without any unnecessary surface area.



Embodiment 2

Fig. 25A illustrates a second embodiment of the present invention.

In said second embodiment, the present invention is applied to a CMOS inverter circuit. The production method will not be explained as it is basically same as that of the first embodiment.

Fig. 25B is a circuit diagram of the present embodiment, and Fig. 25C is a similar device obtained by the prior art, for the purpose of comparison. As will be apparent from the comparison of Fig. 25C representing the prior art and Fig. 25A representing the present invention, the layout area of the device can be significantly reduced by the use of the electrode structure of the present invention in the connecting part of the source area and the sub area in the inverter circuit.

Embodiment 3

A third embodiment of the present invention is illustrated in Figs. 26A and 26B, and in a circuit diagram in Fig. 26C. The producing process of the present embodiment will not be explained as it is basically same as that of the foregoing first embodiment.

The present third embodiment also provides a CMOS inverter, but is different from the second embodiment in that the MOS transistors have a vertical

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structure. As will be apparent from the illustrations, the electrode structure of the present invention is even more effective for reducing the layout area in a circuit employing vertical MOS transistors.

Embodiment 4

A fourth embodiment of the present invention is illustrated in Figs. 27A and 27B, and shown in a circuit diagram in Fig. 27C. The producing process of the present embodiment will not be explained, as it is basically same as that of the foregoing first embodiment.

In the present fourth embodiment, the present invention is applied to a NAND circuit composed again with vertical MOS transistors. As will be apparent from the illustrations, the electrode structure of the present invention is effective, also in this embodiment, for reducing the layout area.

Embodiment 5

Fig. 28 is a schematic cross-sectional view of a NOR circuit element constituting a fifth embodiment of the present invention.

In Fig. 28 there are shown polysilicon gates 205, 207 respectively of PMOS and NMOS transistors; gate insulation films 206, 208; a p^+ drain layer 209 of the PMOS transistor; an n^+ source layer 210 of the NMOS transistor; and electrodes 211, 212, 213, 214 respectively for the drain 209, source 210, and

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polysilicon gates 205, 207. Also in this embodiment, the source 53 of the PMOS transistor and the sources 201, 210 of the NMOS transistor are mutually connected. At the NMOS side there is formed a buried electrode 61 reaching the n^+ drain layer 203, and, at the PMOS side, there is formed an electrode 211 for the p^+ drain layer 59. These two electrodes 61, 211 are formed by selective deposition by the aforementioned Al-CVD method. The structure shown in Fig. 28 can be formed by steps similar to those shown in Figs. 6 to 17.

A first input terminal 215 of the NOR circuit is connected to the gate 207 of the NMOS transistor and the gate 205 of the PMOS transistor. A second input terminal 216 of the NOR circuit is connected to the common gate 55 of the NMOS and PMOS transistors.

The present device functions in the following manner. When the first input terminal 215 receives a voltage equal to or larger than V_{th} of the NMOS transistor, for example a highest potential and the second input terminal 216 receives a voltage equal to or lower than [highest potential + V_{th} of PMOS transistor], for example a lowest potential, a channel is formed below the NMOS transistor, whereby the drain 203 and the source 210 thereof are connected and the output terminal 217 is maintained at the lowest potential. In the PMOS transistor in this state, the

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p^+ layer 101 and the source area 53 are connected through the channel, but the source 53 is not connected to the power supply since a channel is not formed between the drain 209 and the p^+ layer 51. When the voltages applied to the first and second input terminals 215, 216 are interchanged, the drain 203 and the source 201 of the NMOS transistor are connected through the channel, whereby the output terminal is maintained at the lowest potential. In this state the drain 209 and the p^+ layer 51 of the PMOS transistor are connected through the channel, but the source 53 is not connected to the power supply, since a channel is not formed between the source 53 and the p^+ layer 51 of the PMOS transistor. Then, when the first and second input terminals 215, 216 both receive a voltage equal to or higher than V_{th} of the NMOS transistor, for example the highest potential, a channel is formed below the NMOS transistor, whereby the drain 203 is connected with the sources 201, 210 through said channel and the output terminal 217 is maintained at the lowest potential. The source 53 is not connected to the power supply, since a channel is not formed below the PMOS transistor. Then, when the first and second input terminals 215, 216 both receive a voltage equal to or lower than [highest potential + V_{th} of PMOS transistor], for example the lowest potential, a channel is formed below the PMOS transistor, whereby the source 53 is connected to

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the drain 209 through the p^+ layer 51 and the output terminal 217 is maintained at the highest potential. In this state the sources 201, 210 are not connected to the power supply, since a channel is not formed below the NMOS transistor.

The NOR function is achieved as explained above, since the output terminal is maintained at the highest potential only when the first and second input terminals are given the lowest potential and at the lowest potential in other combinations of the input potentials.

Also the present embodiment can reduce the number of electrode and the dimension of the element, as in the example shown in Fig. 5.

Embodiment 6

Fig. 29 is a schematic cross-sectional view of a NAND circuit device constituting a sixth embodiment of the present invention.

In Fig. 29, there are shown a p^+ source layer 218 of the PMOS transistor, and an n^+ drain layer 219 of the NMOS transistor. In the present device, a buried electrode 60 reaching a p^+ drain layer 51 is formed at the PMOS side, and an electrode 220 for the n^+ drain 219 is formed at the NMOS side. Said electrode 220 is also formed by selective aluminum deposition utilizing DMAH and hydrogen. The structure shown in Fig. 29 can be prepared by steps similar to those in Figs. 6 to 17.

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A first input terminal 221 of the NAND circuit is connected to the gate 207 of the NMOS transistor and the gate 205 of the PMOS transistor. A second input terminal 222 of the NAND circuit is connected to the common gate 55 of the NMOS and PMOS transistors.

The device of the present embodiment functions in the following manner. When the first input terminal 221 receives a voltage equal to or higher than V_{th} of the NMOS transistor, for example a highest potential, and the second input terminal 222 receives a voltage equal to or lower than [highest potential + V_{th} of PMOS transistor], for example a lowest potential, a channel is formed below the PMOS transistor whereby the drain 51 and the source 53 thereof are connected and an output terminal 223 is maintained at the highest potential. In the NMOS transistor in this state, the n^+ layer 203 is connected with the drain 219 through the channel, but the source 201 is not connected to the power source since a channel is not formed between the source 201 and the n^+ layer 203. When the voltages applied to the first and second input terminals 221, 222 are interchanged, the drain 51 and the source 218 of the PMOS transistor are connected through the channel whereby the output terminal 223 is maintained at the highest potential. In this state the source 201 is not connected to the power source since a channel is not formed between the drain 219 and the n^+ layer 203 of

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the NMOS transistor. Then, when the first and second input terminals both receive a voltage equal to or lower than [highest potential + V_{th} of PMOS transistor], for example the lowest potential, a channel is formed below the PMOS transistor, whereby the drain 51 is connected with the source 53, 218 through said channel and the output terminal 223 is maintained at the highest potential. In this state the source 201 is not connected to the power source, since a channel is not formed below the NMOS transistor. Then, when the first and second input terminals both receive a voltage equal to or higher than V_{th} of the NMOS transistor, for example the highest potential, a channel is formed below the NMOS transistor, whereby the drain 219 is connected with the source 200 through the n^+ layer 203 and the output terminal is maintained at the lowest potential. In this state the sources 53, 218 are not connected to the power source, since a channel is not formed below the PMOS transistor.

The NAND function is thus achieved, as the output terminal is maintained at the lowest potential only when the first and second input terminals are given the highest potential, but is maintained at the highest potential at other combinations of the input potentials.

Also this NAND circuit device is provided with a reduced number of electrodes and can therefore

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reduce the dimension of the device.

In the foregoing embodiments 5 and 6, similar advantages can be obtained even if the semiconductors of n- and p-type are interchanged.

Similar advantages can be obtained also when the polysilicon electrode is replaced by a metal or silicide electrode.

As explained in the foregoing, the present invention allows to obtain a semiconductor device provided with very small functional elements, which can be constructed by necessary minimum components without any unnecessary surface area, thereby being capable of significantly reducing the layout area and adapted for achieving a fine geometry and a high level of integration.



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CLAIMS:

1. A semiconductor device provided with a first semiconductor area of a first conductive type and a second semiconductor area, formed on or under said first semiconductor area, of a second conductive type different from said first conductive type, wherein:

an electrode electrically connected to said first semiconductor area is formed through said second semiconductor area; and

said first and second semiconductor areas are electrically shortcircuited by said electrode.

2. A semiconductor device according to claim 1, wherein said second semiconductor area is a source or drain area of a field effect transistor.

3. A semiconductor device according to claim 2, wherein:

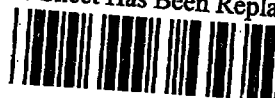
said field effect transistor includes a buried drain area and a buried gate area;

a PMOS transistor and an NMOS transistor are formed on respective sides of said buried gate;

said second semiconductor area constitutes said buried drain area; and

an electrode reaching said drain area is provided in at least either of said PMOS and NMOS transistors.

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4. A semiconductor device according to any of claims 1 to 3, wherein said electrode is composed of aluminum or a conductive material principally composed of aluminum.

5. A semiconductor device according to claim 3, constituting a .NOT circuit element.

6. A semiconductor device according to claim 3, constituting a NOR circuit element.

7. A semiconductor device according to claim 3, constituting a NAND circuit element.

8. A method for producing a semiconductor device provided with a first semiconductor area of a first conductive type, a second semiconductor area formed on said first semiconductor area and having a second conductive type different from said first conductive type, and an electrode for short-circuiting said first and second semiconductor areas, comprising:

a first step for forming an aperture in said second semiconductor area thereby exposing a part of said first semiconductor area; and

a second step for depositing a conductive material in said aperture;

wherein said second step includes a step for

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depositing aluminum or a conductive material principally composed of aluminum in said aperture by a CVD method utilizing alkylaluminum hydride gas and hydrogen.

9. A method for producing a semiconductor device according to claim 8, wherein said alkylaluminum hydride is dimethylaluminum hydride.

10. A method for producing a semiconductor device, comprising steps of:

forming buried drain areas of a PMOS transistor and of a NMOS transistor on a semiconductor substrate;

forming an aperture so as to penetrate a junction part of the drain area of said PMOS transistor and that of said NMOS transistor;

forming an insulation film covering the internal surface of said aperture;

depositing, in said aperture, a common gate for said PMOS and NMOS transistors; and

forming a buried electrode reaching at least either of the buried drain area of said PMOS transistor and that of said NMOS transistor.

11. A method for producing a semiconductor device according to claim 10, wherein said buried electrode is formed by forming an aperture reaching at least either of said two buried drain areas, and

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selectively depositing aluminum in said aperture by
a CVD method utilizing dimethylaluminum hydride and
hydrogen.



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SEMICONDUCTOR DEVICE AND METHOD FOR PRODUCING THE SAMEABSTRACT OF THE DISCLOSURE

There is provided a semiconductor device with very small functional elements, which can be constructed by necessary minimum components without any unnecessary surface area, thus being capable of significantly reducing the layout area and adapted for achieving a fine geometry and a high level of integration. The semiconductor device is provided with a first semiconductor area of a first conductive type (for example a p^- well) and a second semiconductor area formed on or under the first semiconductor area and having a second conductive type different from the first conductive type (for example a source or drain area), in which an electrode electrically connected to the first semiconductor area is formed through the second semiconductor area, and the first and second semiconductor areas are shortcircuited by the above-mentioned electrode.

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(Fig. 4A)

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FIG. 1A

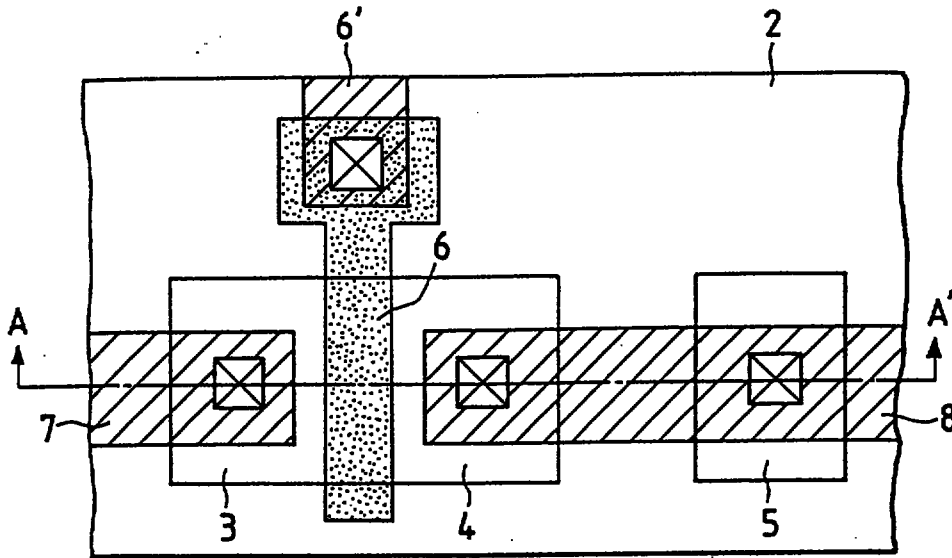
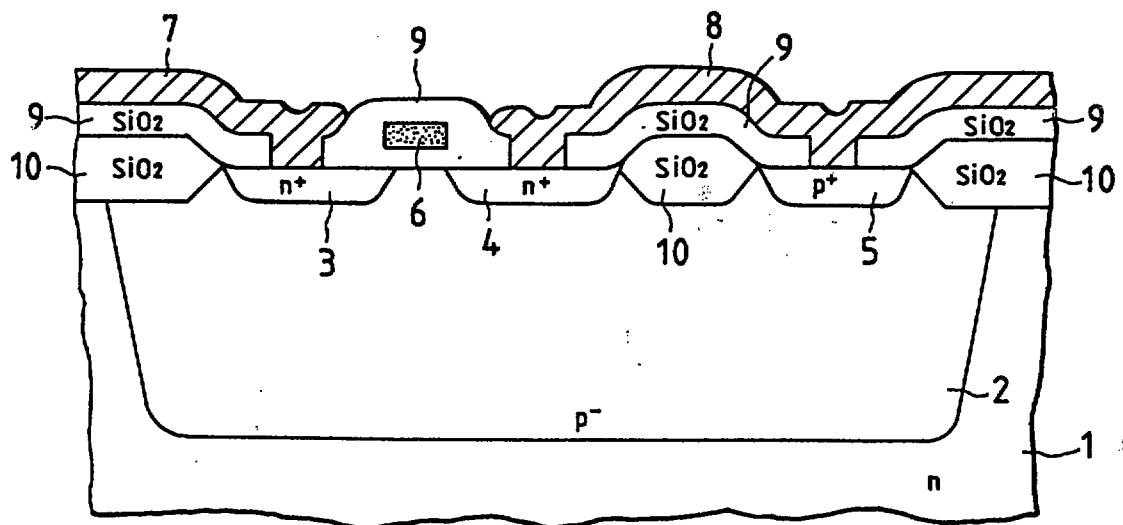


FIG. 1B



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FIG. 2A

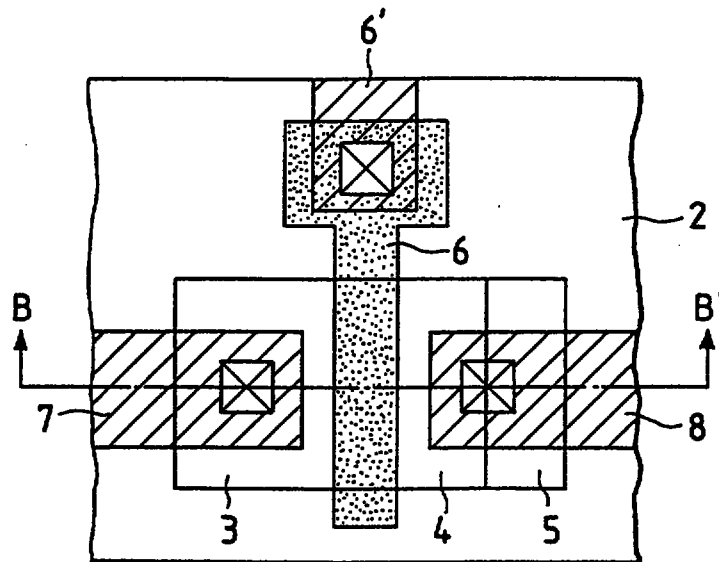
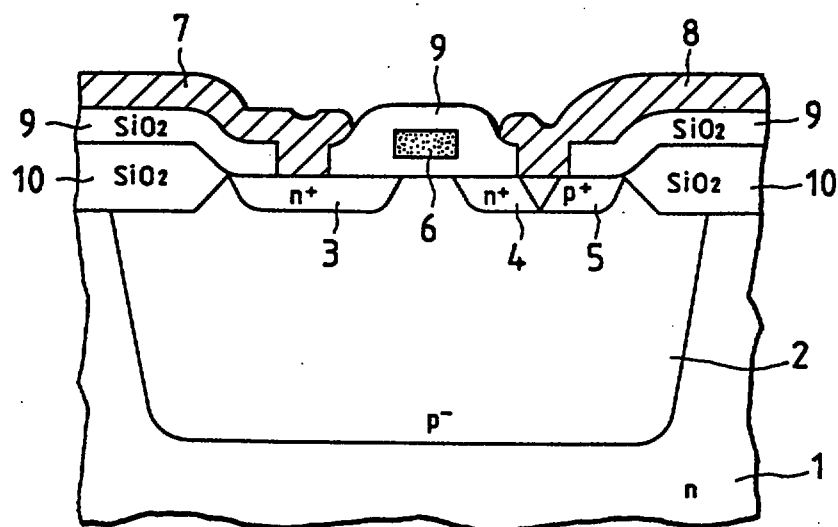
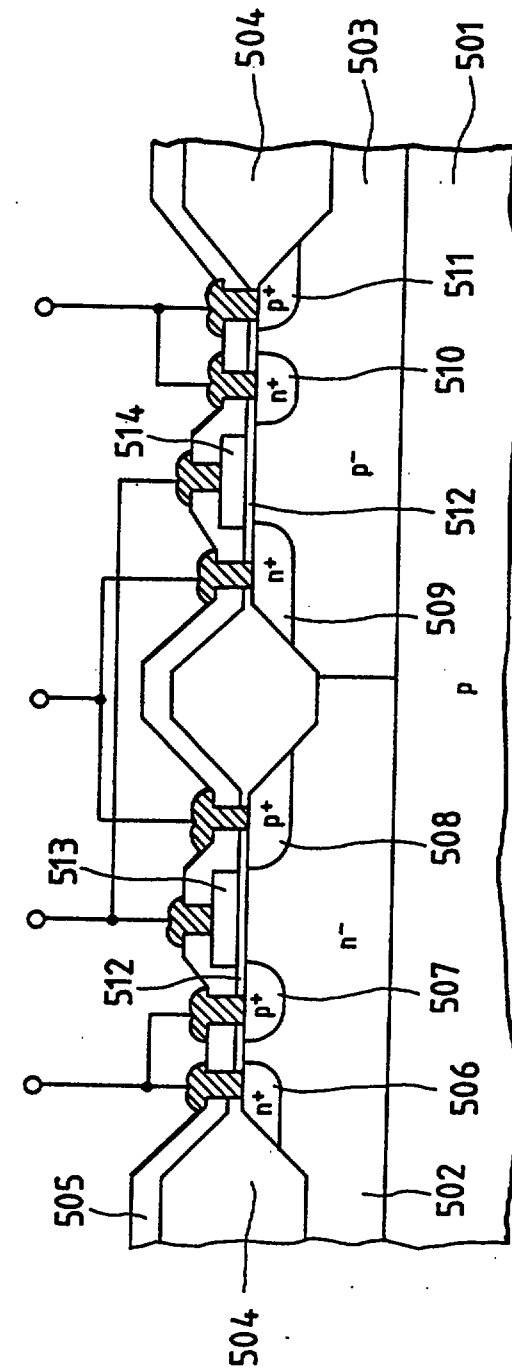


FIG. 2B





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FIG. 4A

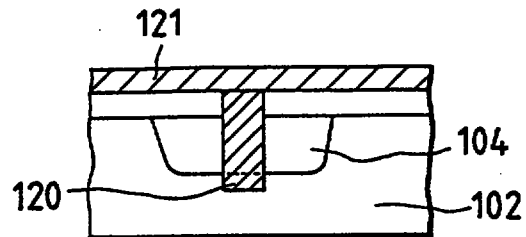


FIG. 4B

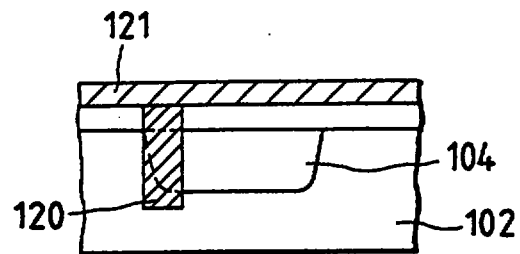


FIG. 4C

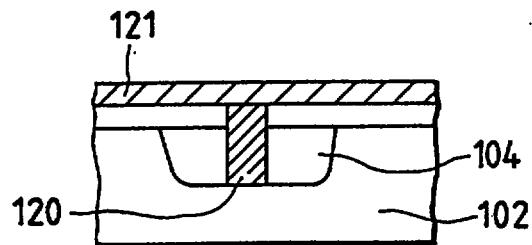
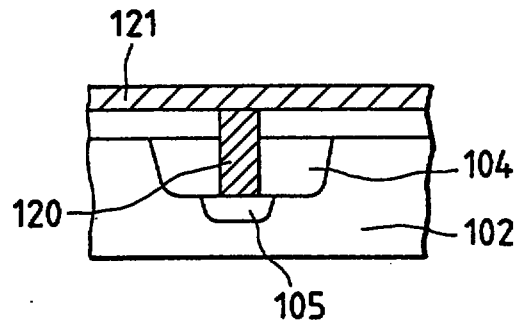


FIG. 4D



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FIG. 5A

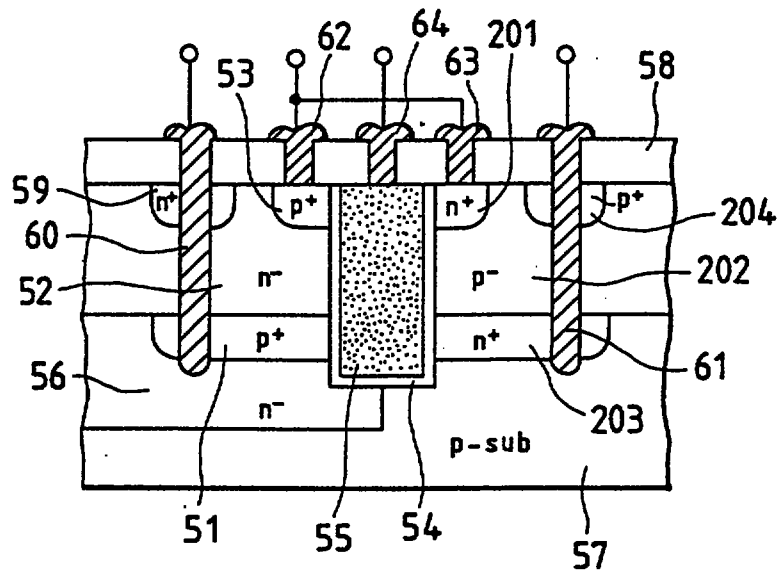
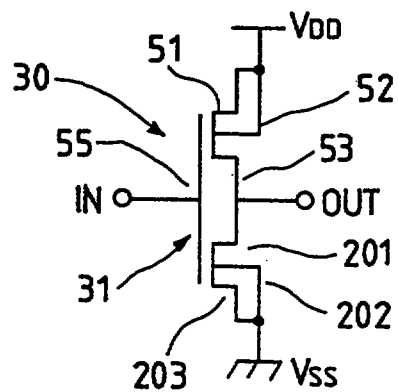


FIG. 5B



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FIG. 6

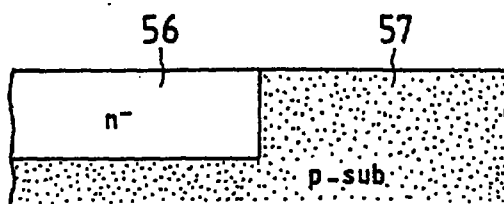


FIG. 7

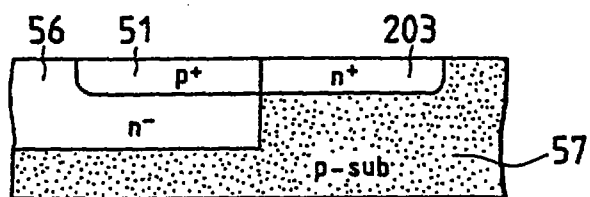


FIG. 8

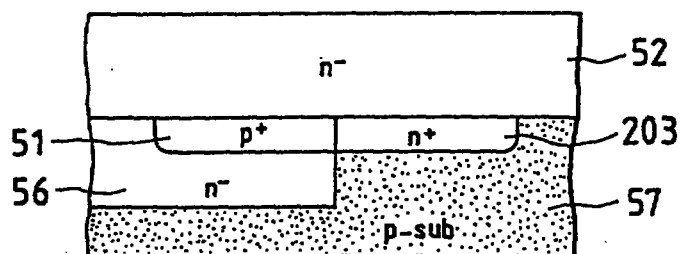


FIG. 9

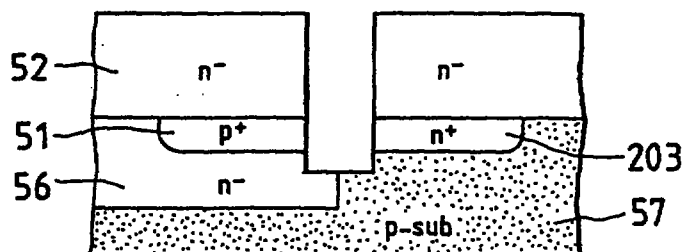


FIG. 10

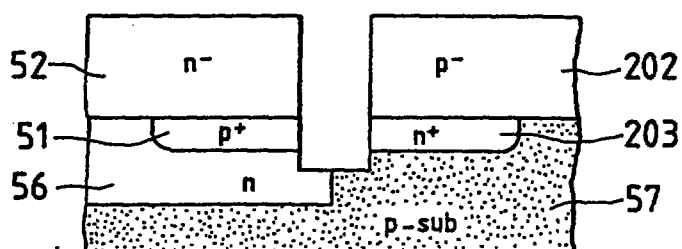
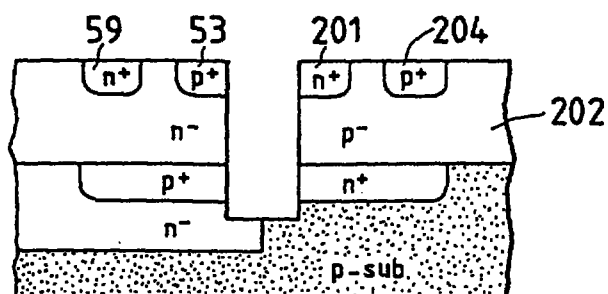


FIG. 11



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FIG. 12

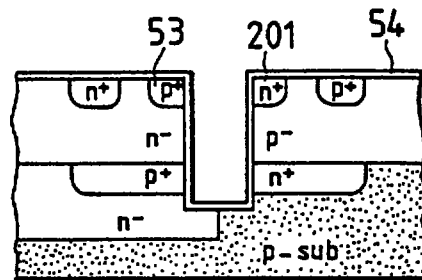


FIG. 13

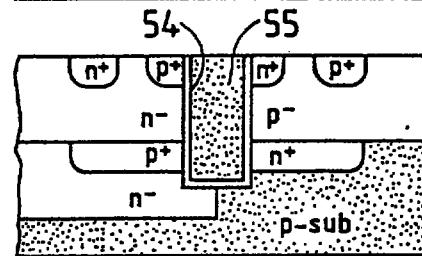


FIG. 14

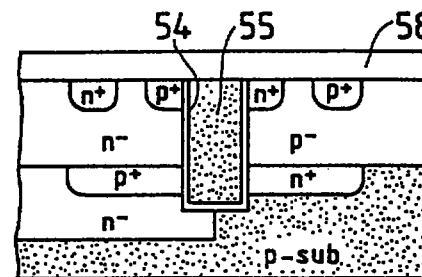


FIG. 15

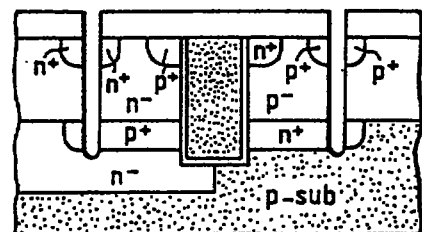


FIG. 16

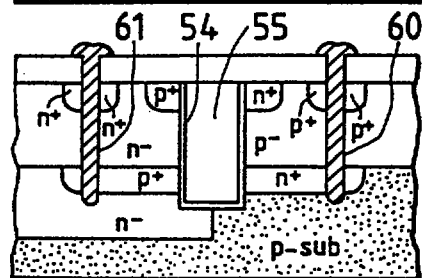
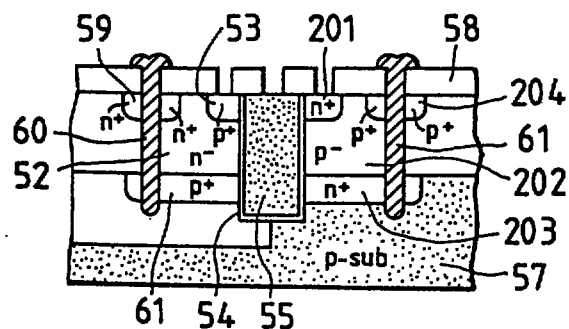


FIG. 17



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FIG. 18

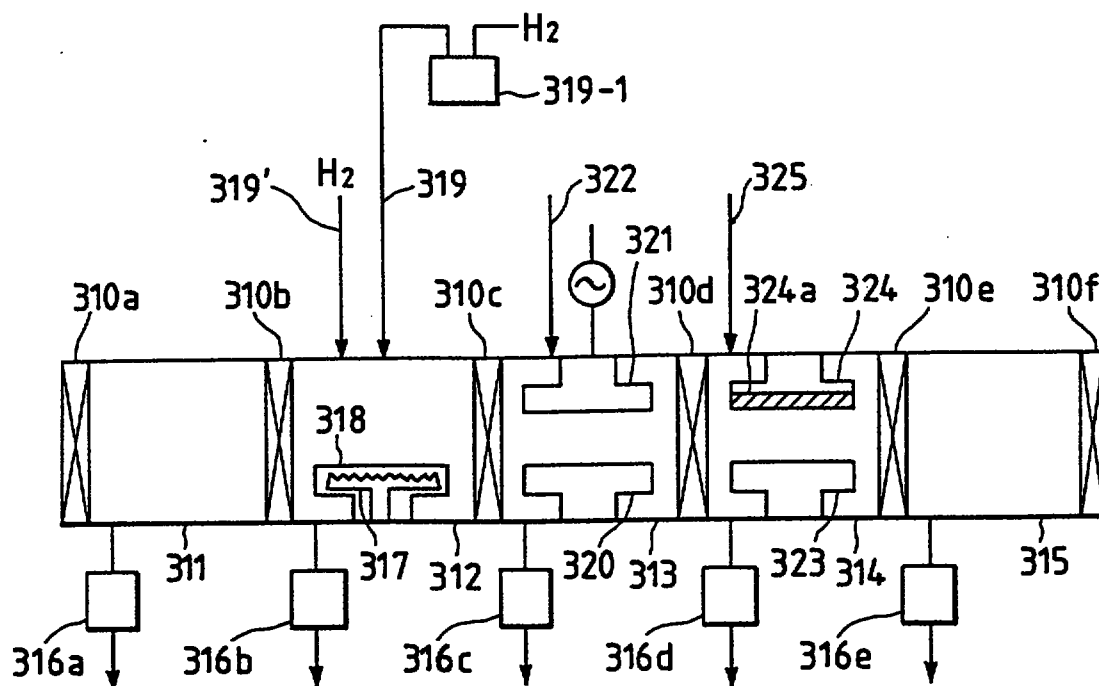
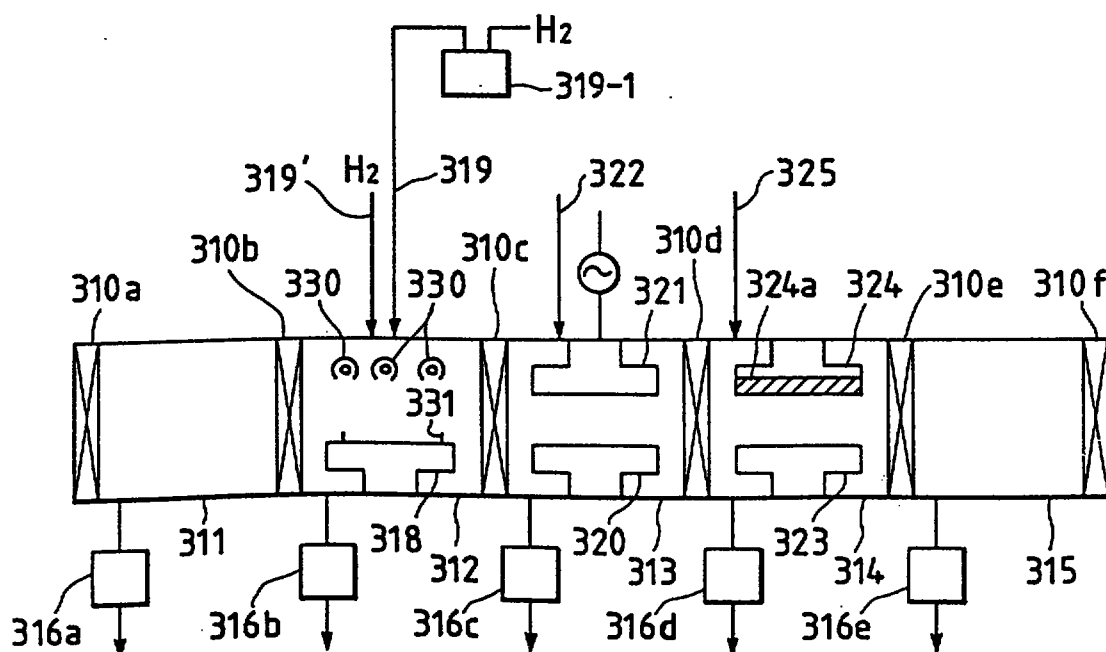


FIG. 19



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FIG. 20

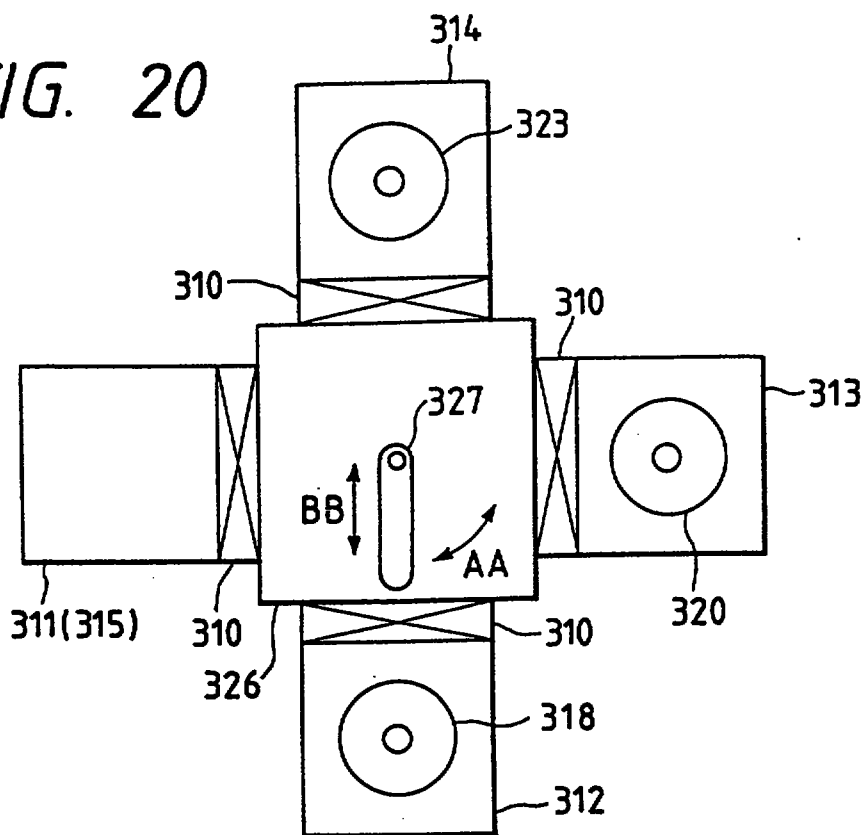
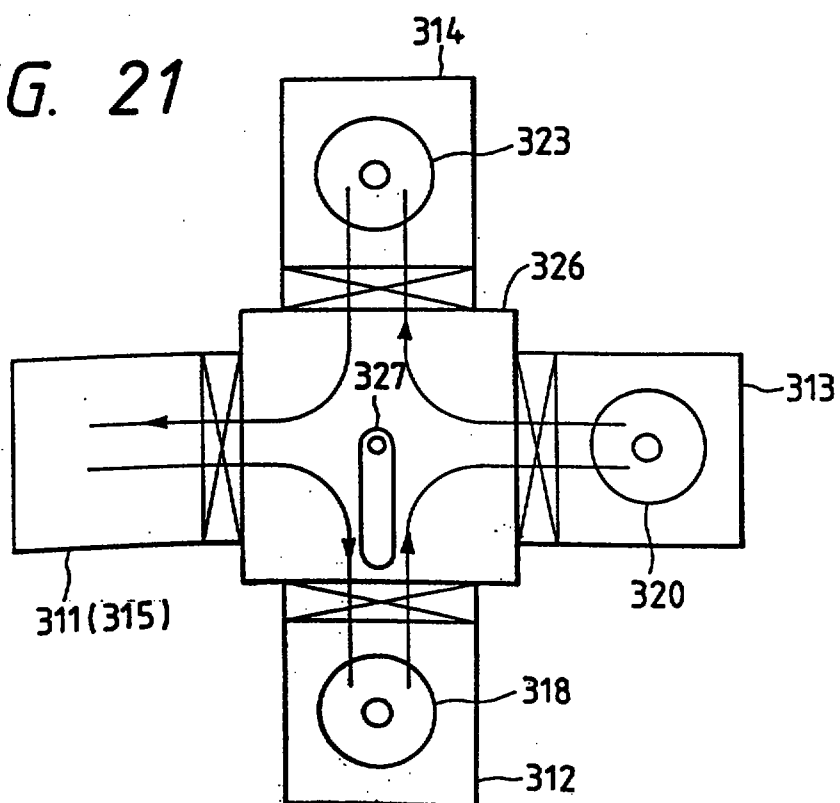


FIG. 21



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FIG. 22A

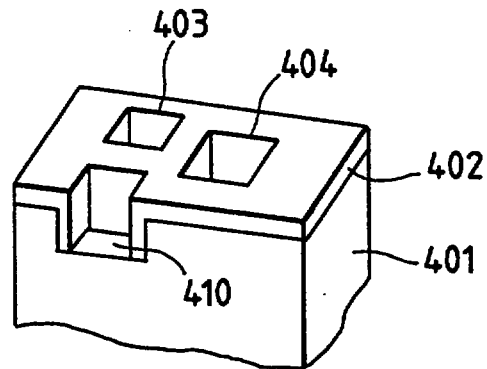


FIG. 22B

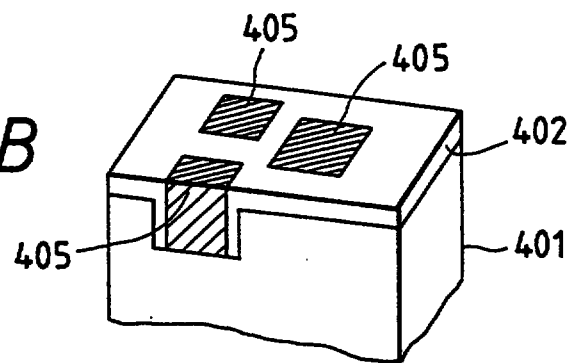
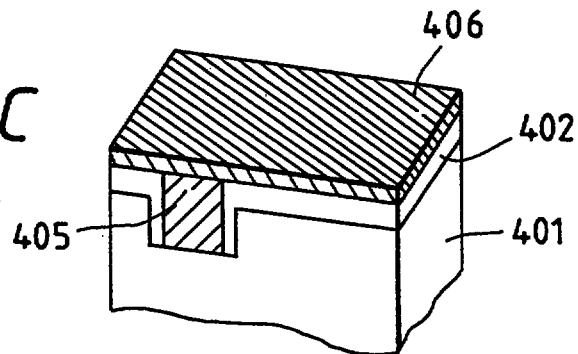


FIG. 22C



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FIG. 23A

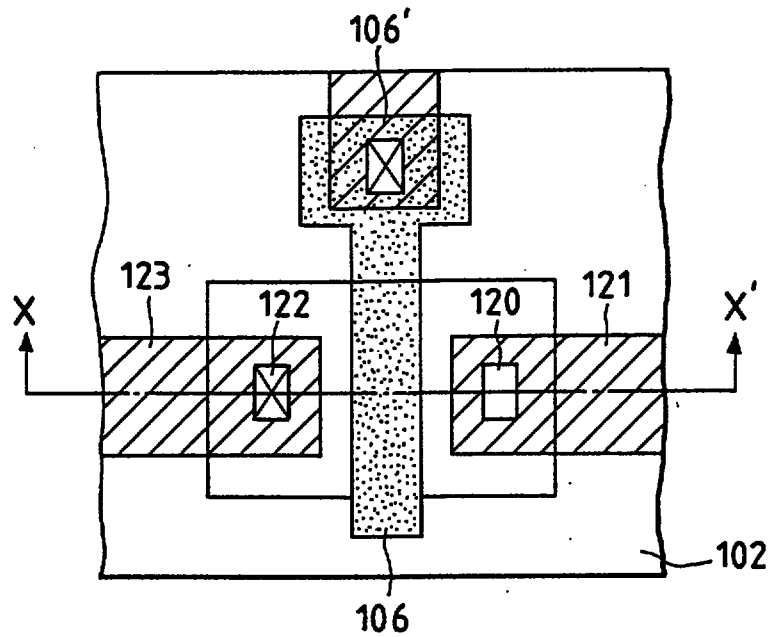
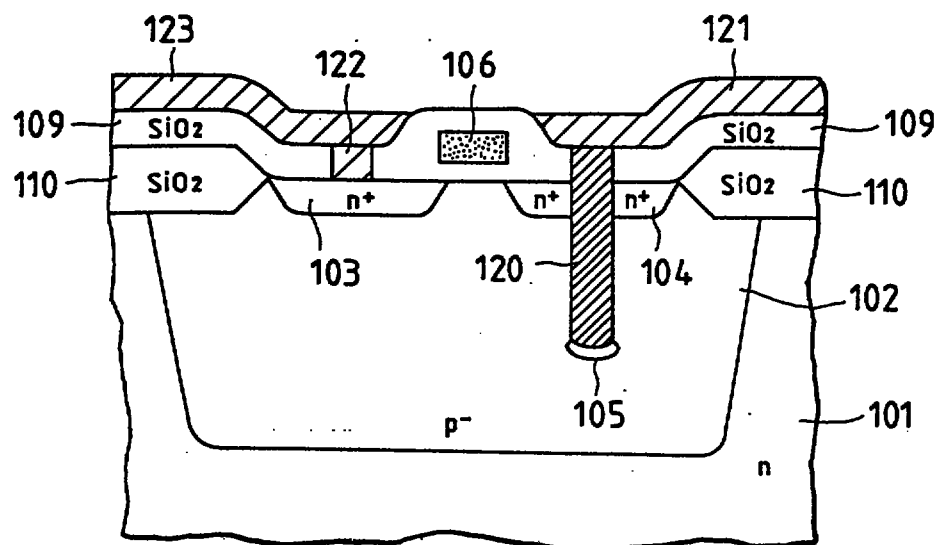


FIG. 23B



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FIG. 24A

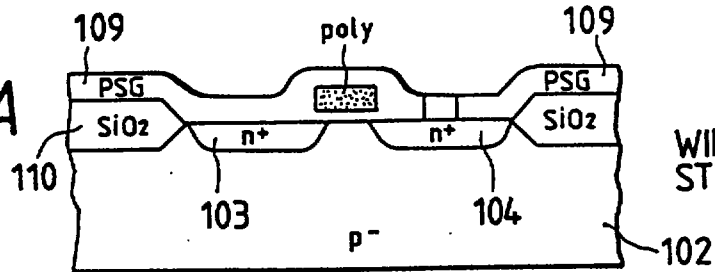
WINDOW FORMING
STEP

FIG. 24B

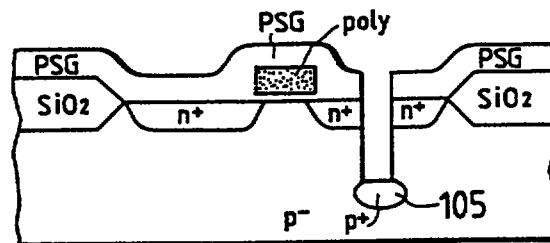
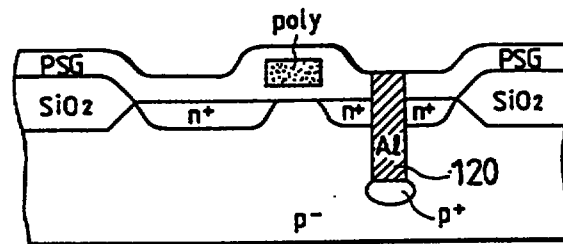
ETCHING PROCESS
SHAPING STEP

FIG. 24C



SHAPING STEP

FIG. 24D

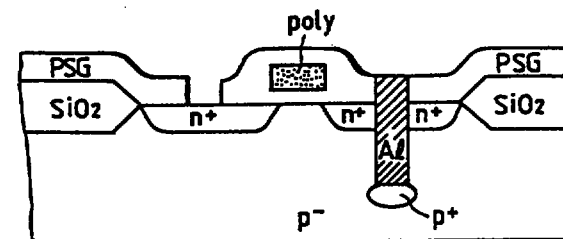
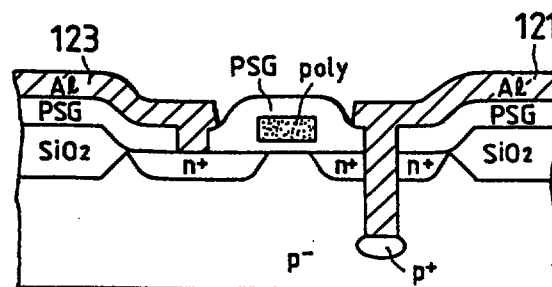
WINDOW FORMING
STEP

FIG. 24E



WIRING STEP

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FIG. 25A

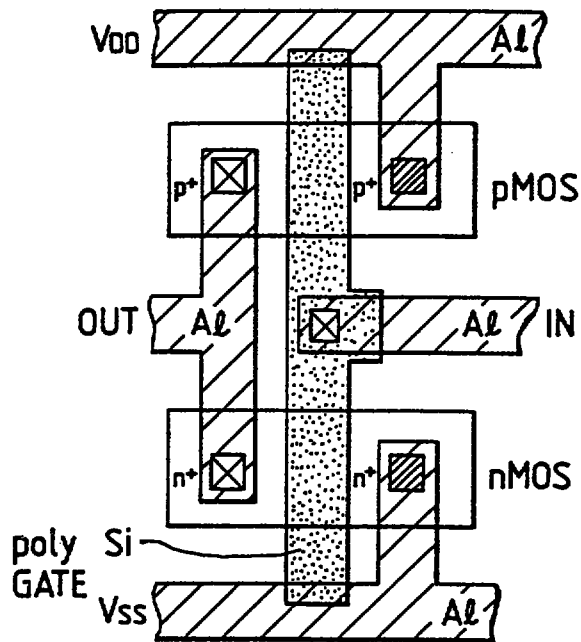


FIG. 25B

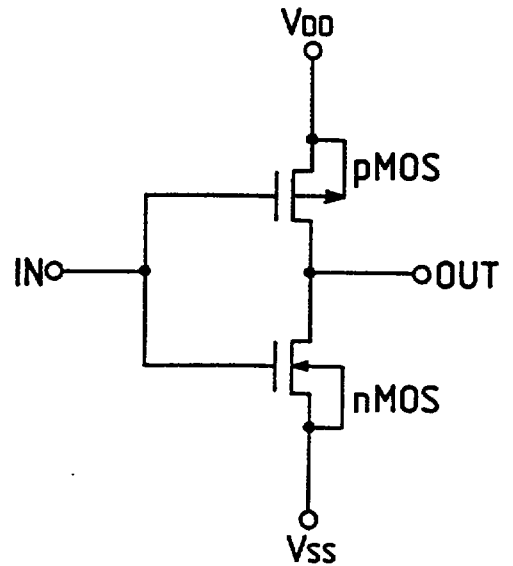
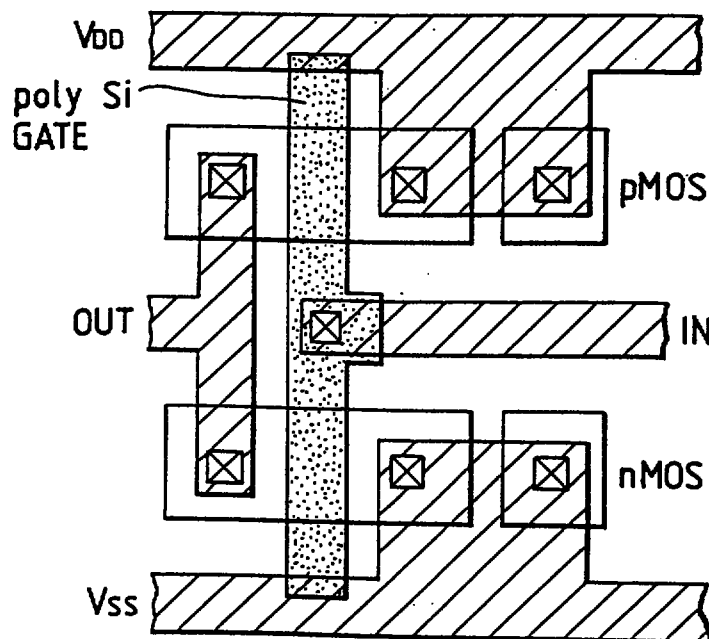


FIG. 25C



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FIG. 26A

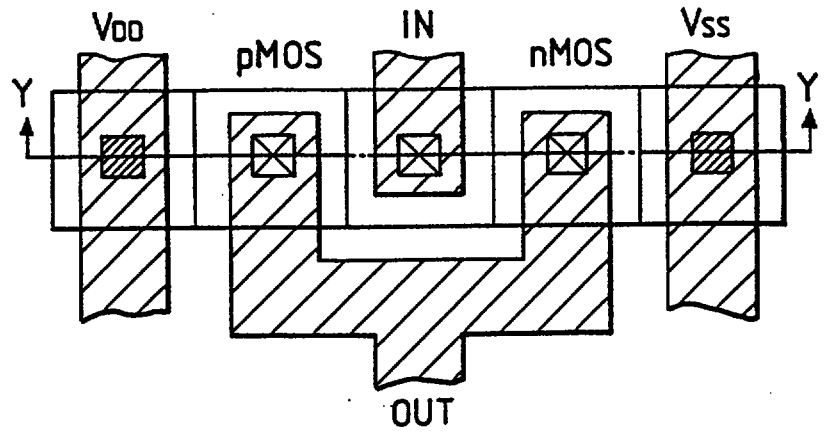


FIG. 26B

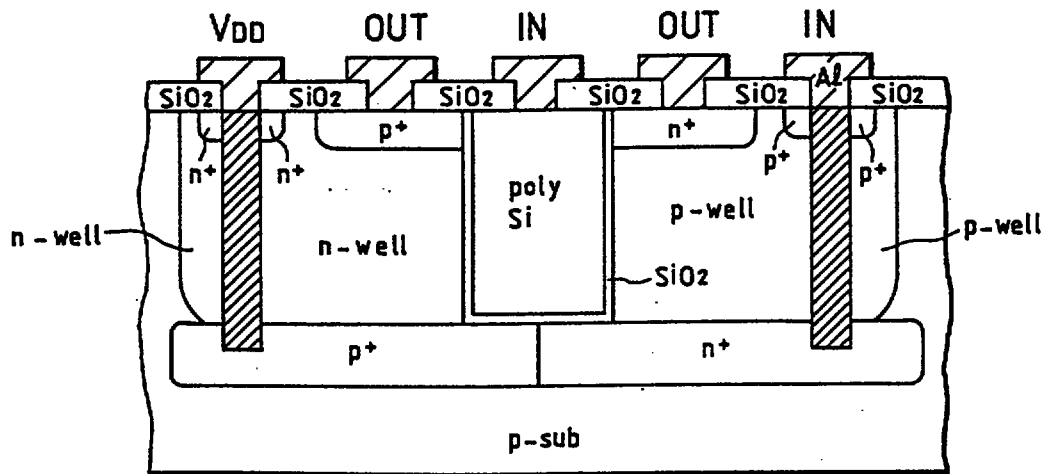
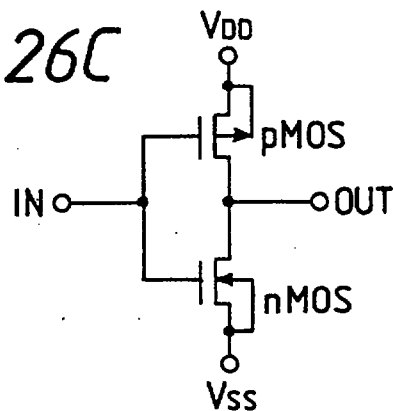


FIG. 26C



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FIG. 27A

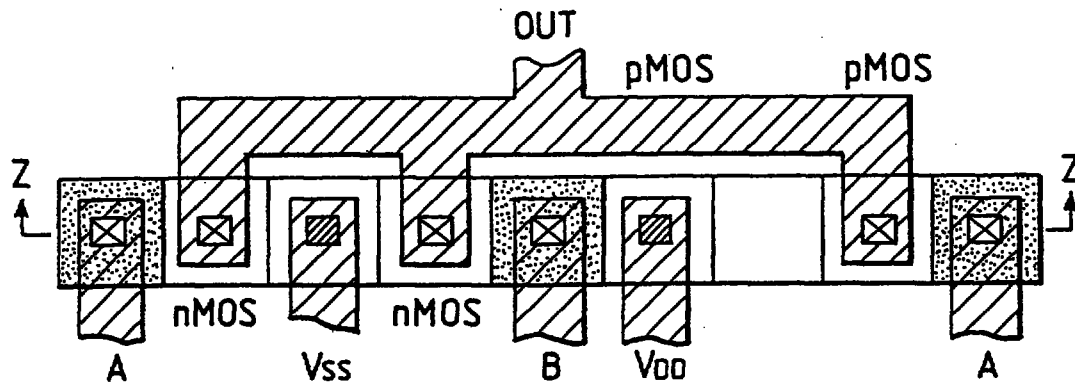


FIG. 27B

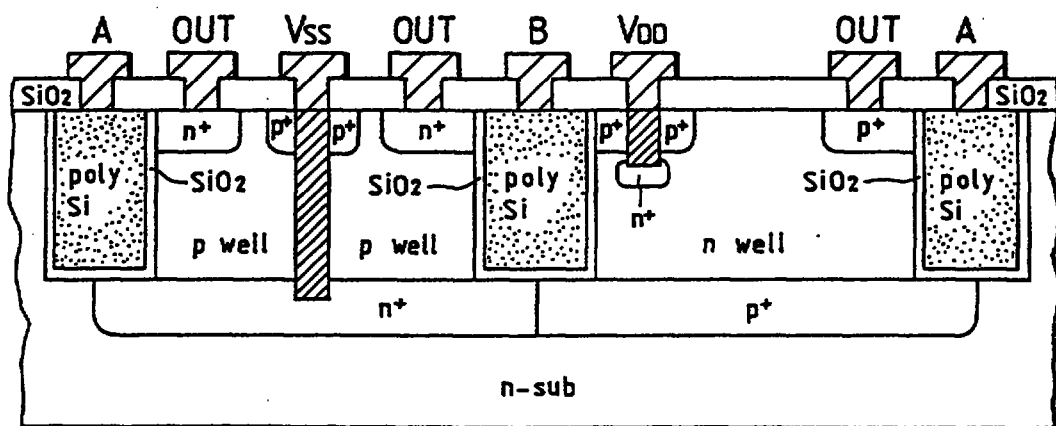
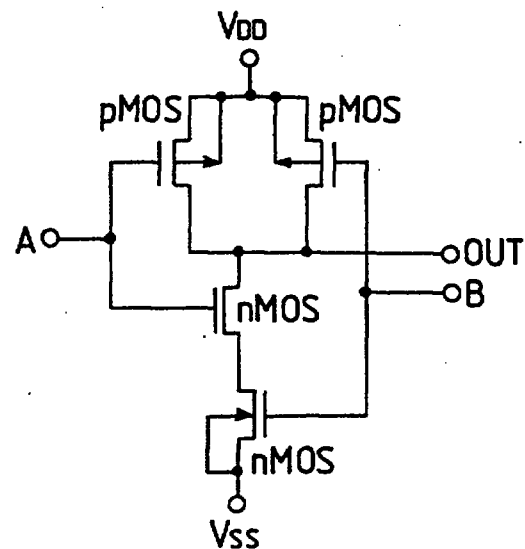


FIG. 27C



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FIG. 28

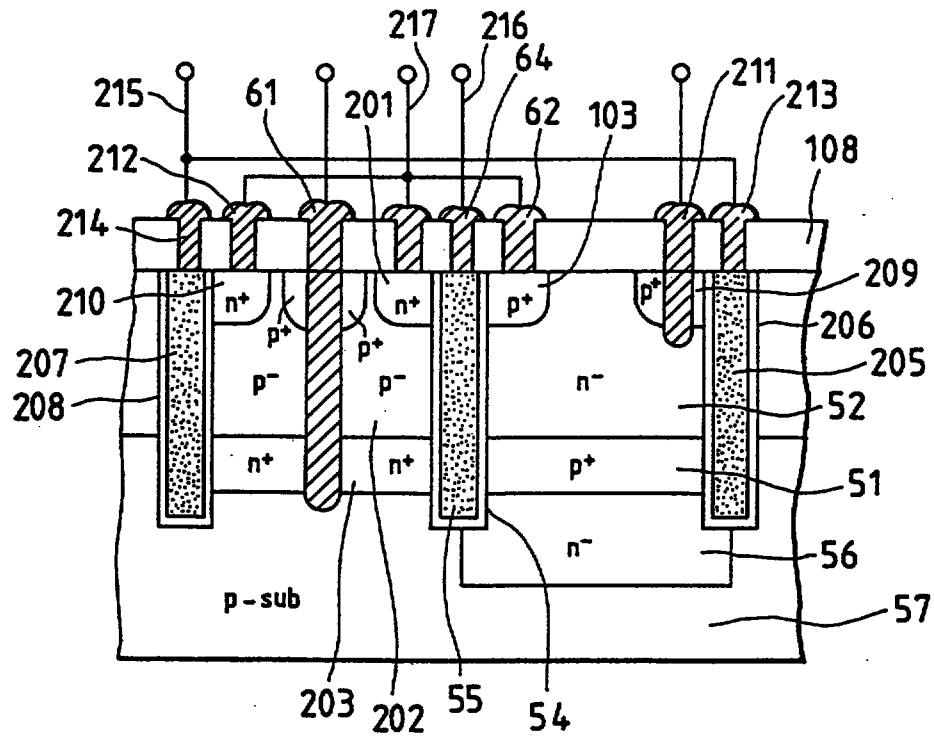
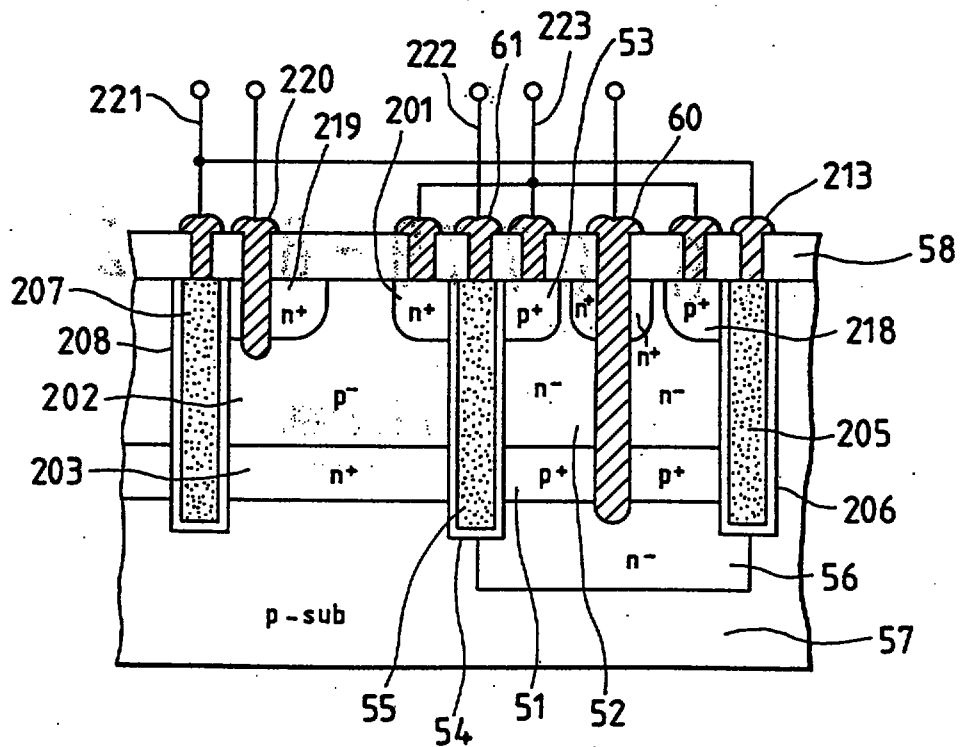


FIG. 29





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REPLACEMENT SHEET

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We claim:

1. A semiconductor device having a semiconductor body provided with a vertical field-effect transistor, which body comprises:
 - a first semiconductor region and a second semiconductor region of a first conductivity type to provide source and drain regions;
 - a third semiconductor region of a second conductivity type different from said first conductivity type having an intermediate portion to provide a channel portion and a surface portion;
 - said first semiconductor region disposed on said intermediate portion;
 - said third semiconductor region disposed on said second semiconductor region;
 - a gate electrode separated from said intermediate portion by an insulating material, wherein said source and drain regions and said channel portion are arranged only vertically along a side surface of said gate electrode; and
 - a buried electrode electrically connected with said second semiconductor region and said third semiconductor region via a through hole penetrating said third semiconductor region, wherein said second region and said third region are thereby short circuited; and wherein said buried electrode is formed in said body.
2. A semiconductor device according to claim 1, constituting a NOT circuit element.
3. A semiconductor device according to claim 1, constituting a NOR circuit element.
4. A semiconductor device according to claim 1, constituting a NAND circuit element.
5. A semiconductor device according to claim 1, wherein said second semiconductor region is a drain.
6. A semiconductor device according to claim 1, wherein said second semiconductor region is buried within said semiconductor body, and is provided on a substrate of the second conductivity type.
7. A semiconductor device according to claim 6, wherein said buried electrode is contacted with said substrate.



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8. A semiconductor device according to claim 1, wherein said second semiconductor region is buried within said semiconductor body, and is provided on a fourth semiconductor region of the second conductivity type.

9. A semiconductor device according to claim 8, wherein said fourth semiconductor region is provided on a substrate of the first conductivity type.

10. A semiconductor device according to claim 1, wherein said buried electrode is made of aluminum.

11. A semiconductor device having a semiconductor body provided with a vertical complementary MOS inverter, said body comprises:

- a first semiconductor region and a second semiconductor region of an N conductivity type to provide source and drain regions;

- a third semiconductor region of a P conductivity type having an intermediate portion to provide a channel portion and a surface portion;

- said first semiconductor region disposed on said intermediate portion;

- said third semiconductor region disposed on said second semiconductor region;

- a fourth semiconductor region and a fifth semiconductor region of a P conductivity type to provide source and drain regions;

- a sixth semiconductor region of an N conductivity type having an intermediate portion to provide a channel portion and a surface portion;

- said fourth semiconductor region disposed on said intermediate portion;

- said sixth semiconductor region disposed on said fifth semiconductor region;

- a common gate electrode separated from said intermediate portions of said third semiconductor region and said sixth semiconductor region by a gate insulator to provide an input-terminal, wherein each of said source and drain regions and said channel portions are arranged only vertically along opposite sides of said common gate electrodes;

- a first buried electrode electrically connected with said second semiconductor region and said third semiconductor region which are thereby short circuited; and

- a second buried electrode electrically connected with said fifth semiconductor region and said sixth semiconductor region which are thereby short circuited;

wherein said first buried electrode and said second buried electrode are formed in said body.

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12. A semiconductor device having a semiconductor body provided with at least two vertical field-effect transistors said body comprising:

at least two first semiconductor regions and a second semiconductor region of a first conductivity type to provide source and drain regions;

a third semiconductor region of a second conductivity type different from said first conductivity type having an intermediate portion to provide at least two channel portions and a surface portion;

said first semiconductor regions disposed on said intermediate portion;

said third semiconductor region disposed on said second semiconductor region;

at least two gate electrodes separated from said intermediate portions by an insulating material, wherein each of said source and drain regions and channel portions are arranged only vertically along a side surface of each said at least two gate electrodes; and

a buried electrode electrically connected with one of said first semiconductor regions and said third semiconductor region via a through hole penetrating the one of said first semiconductor regions, wherein the one of said first region and said third region are thereby short circuited, and wherein said buried electrode is formed in said body.

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ABSTRACT

SEMICONDUCTOR DEVICE AND METHOD FOR PRODUCING THE SAME

There is provided a semiconductor device with very small functional elements, which can be constructed by necessary minimum components without any unnecessary surface area, thus being capable of significantly reducing the layout area and adapted for achieving a fine geometry and a high level of integration. The semiconductor device is provided with a first semiconductor area of a first conductive type (for example a p^- well) and a second semiconductor area formed on or under the first semiconductor area and having a second conductive type different from the first conductive type (for example a source or drain area), in which an electrode electrically connected to the first semiconductor area is formed through the second semiconductor area, and the first and second semiconductor areas are shortcircuited by the above-mentioned electrode.

(Fig. 4A)