FIG. 1

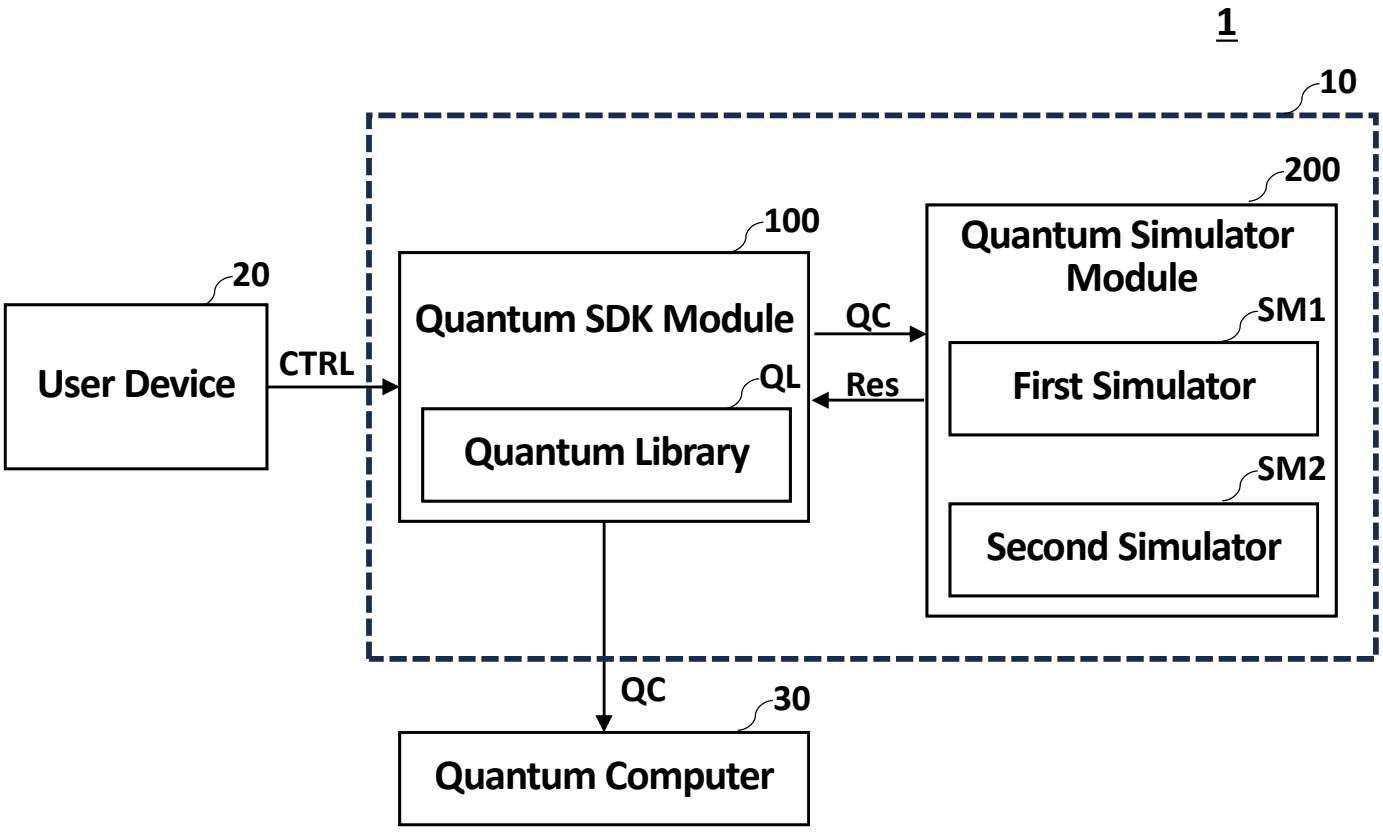

1
10
200
100
Quantum Simulator Module
20
Quantum SDK Module
QC
SM1
User Device
CTRL
QL
Res
First Simulator
Quantum Library
SM2
Second Simulator
QC
30
Quantum Computer

FIG. 2

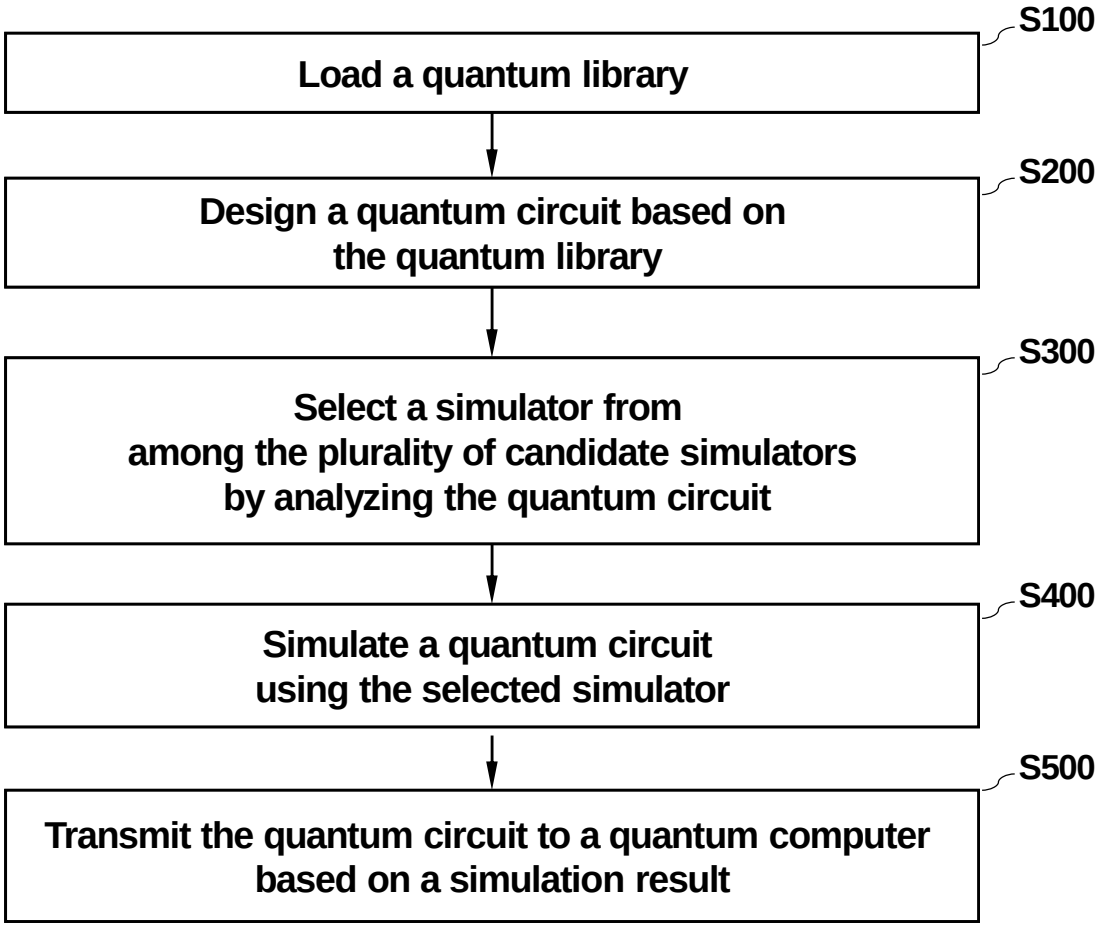

S100
Load a quantum library
S200
Design a quantum circuit based on the quantum library
S300
Select a simulator from among the plurality of candidate simulators by analyzing the quantum circuit
S400
Simulate a quantum circuit using the selected simulator
S500
Transmit the quantum circuit to a quantum computer based on a simulation result

FIG. 3

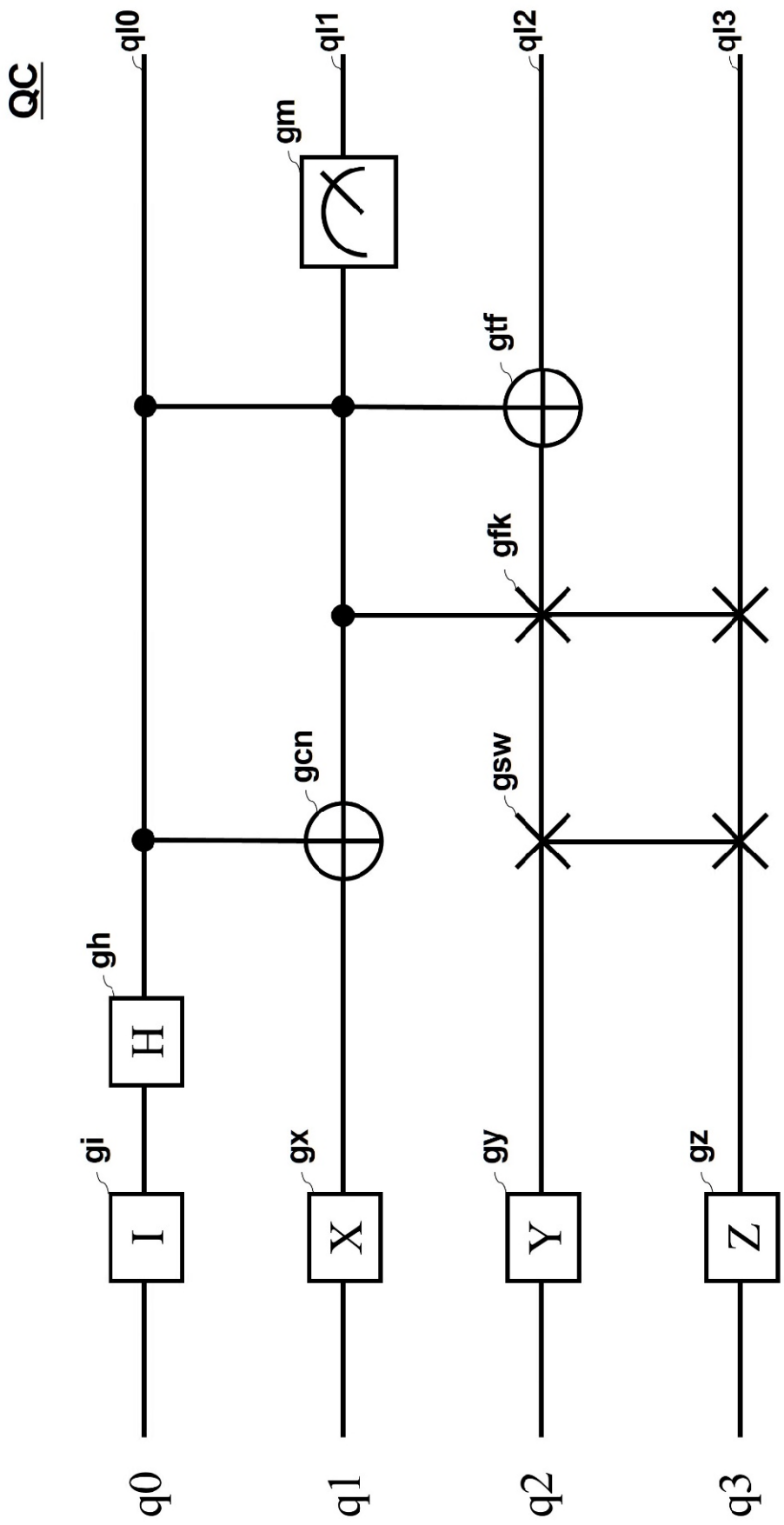

QC
ql0
ql1
ql2
ql3
gm
gtf
gfk
gcn
gsw
gh
gi
gx
gy
gz
H
I
X
Y
Z
q0
q1
q2
q3

FIG. 4

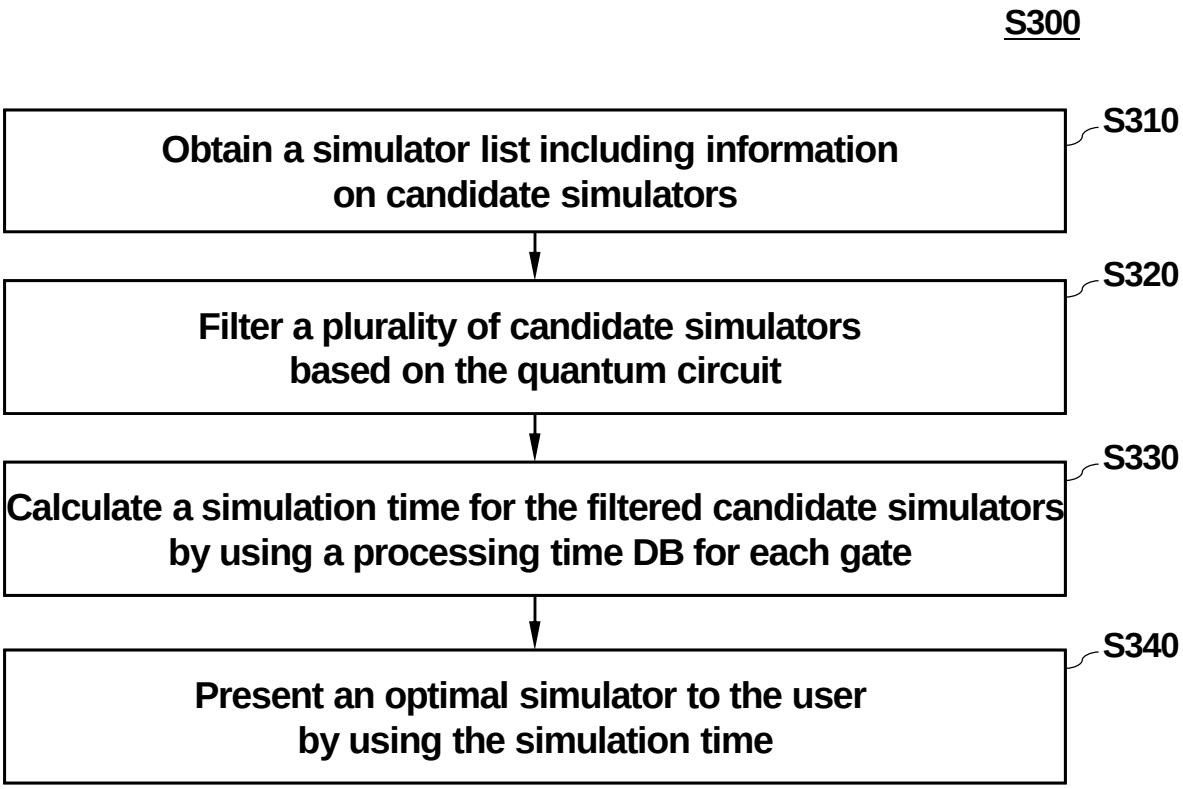

S300
Obtain a simulator list including information on candidate simulators
S310
Filter a plurality of candidate simulators based on the quantum circuit
S320
Calculate a simulation time for the filtered candidate simulators by using a processing time DB for each gate
S330
Present an optimal simulator to the user by using the simulation time
S340

FIG. 5

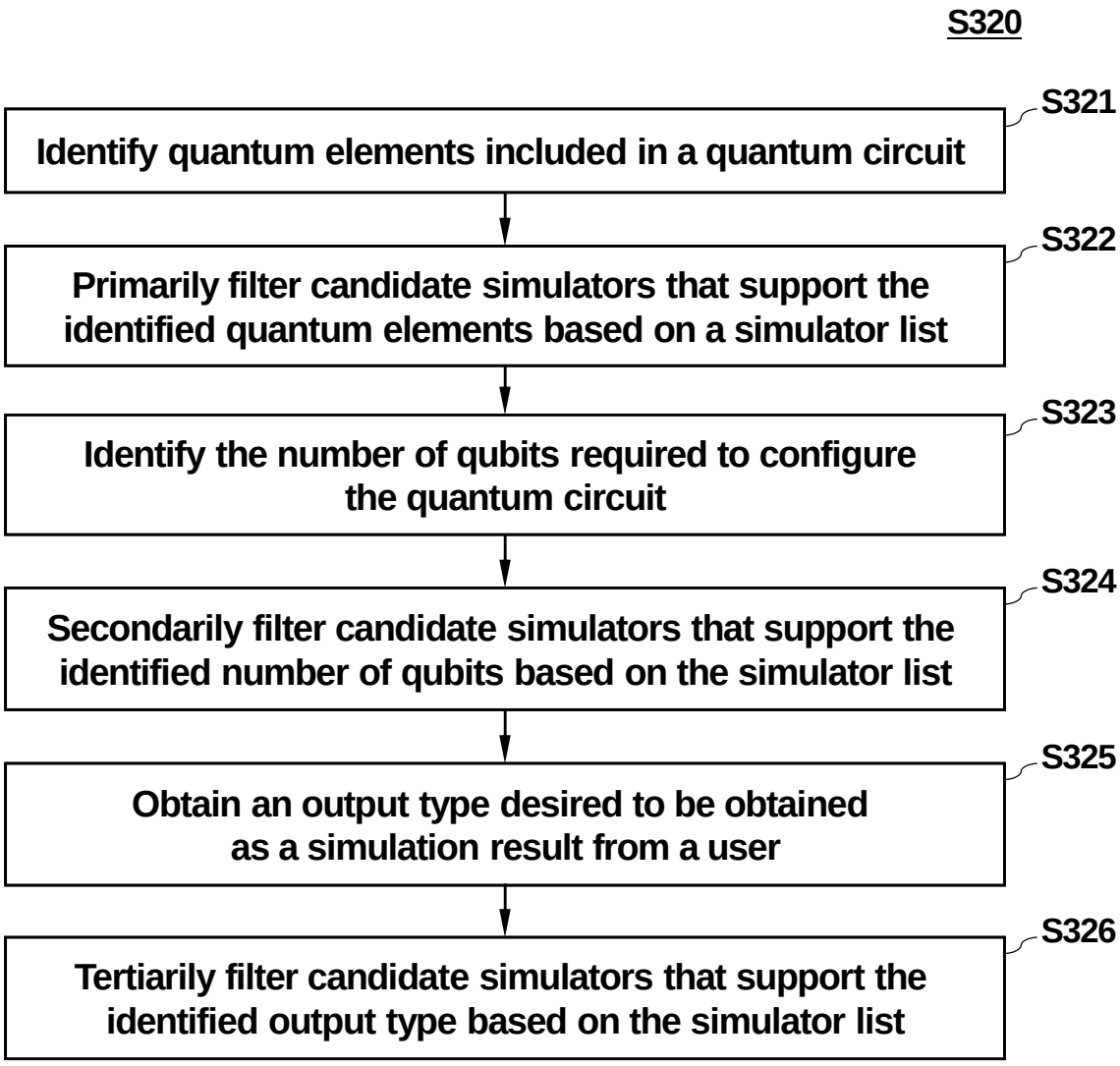

S320
S321
Identify quantum elements included in a quantum circuit
S322
Primarily filter candidate simulators that support the identified quantum elements based on a simulator list
S323
Identify the number of qubits required to configure the quantum circuit
S324
Secondarily filter candidate simulators that support the identified number of qubits based on the simulator list
S325
Obtain an output type desired to be obtained as a simulation result from a user
S326
Tertiarily filter candidate simulators that support the identified output type based on the simulator list

FIG. 6

SL

Simulator	Gate	Qubit	Output Type
SM1	gi, gx, gy, gtf	4	Bit stream
SM2	gh, gcn, gsw	16	Status vector
SM3	gfk, gtf	4	Expected value
SM4	gx, gh, gcn	8	Parameter slope

FIG. 7

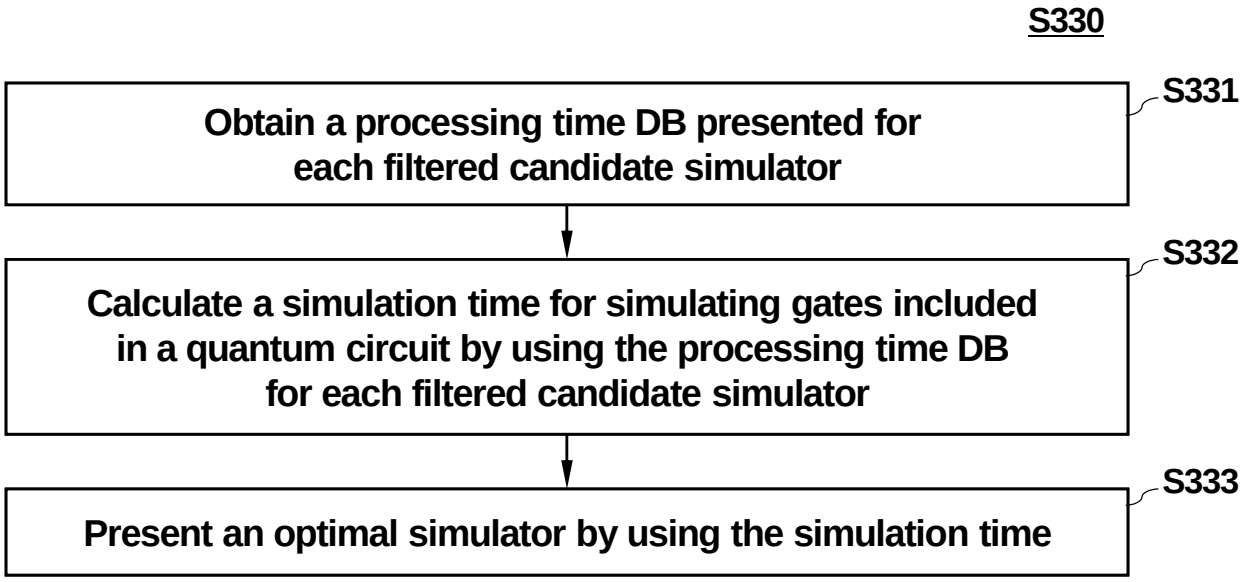

S330
Obtain a processing time DB presented for each filtered candidate simulator
S331
Calculate a simulation time for simulating gates included in a quantum circuit by using the processing time DB for each filtered candidate simulator
S332
Present an optimal simulator by using the simulation time
S333

FIG. 8

GDB1

SM1	
Gate	**Simulation time**
gx	t1
gh	t2
gfk	t3
gx, gh	t4

GDB2

SM2	
Gate	**Simulation time**
gx	t5
gh	t6
gfk	t7
gx, gh	t8

FIG. 9A

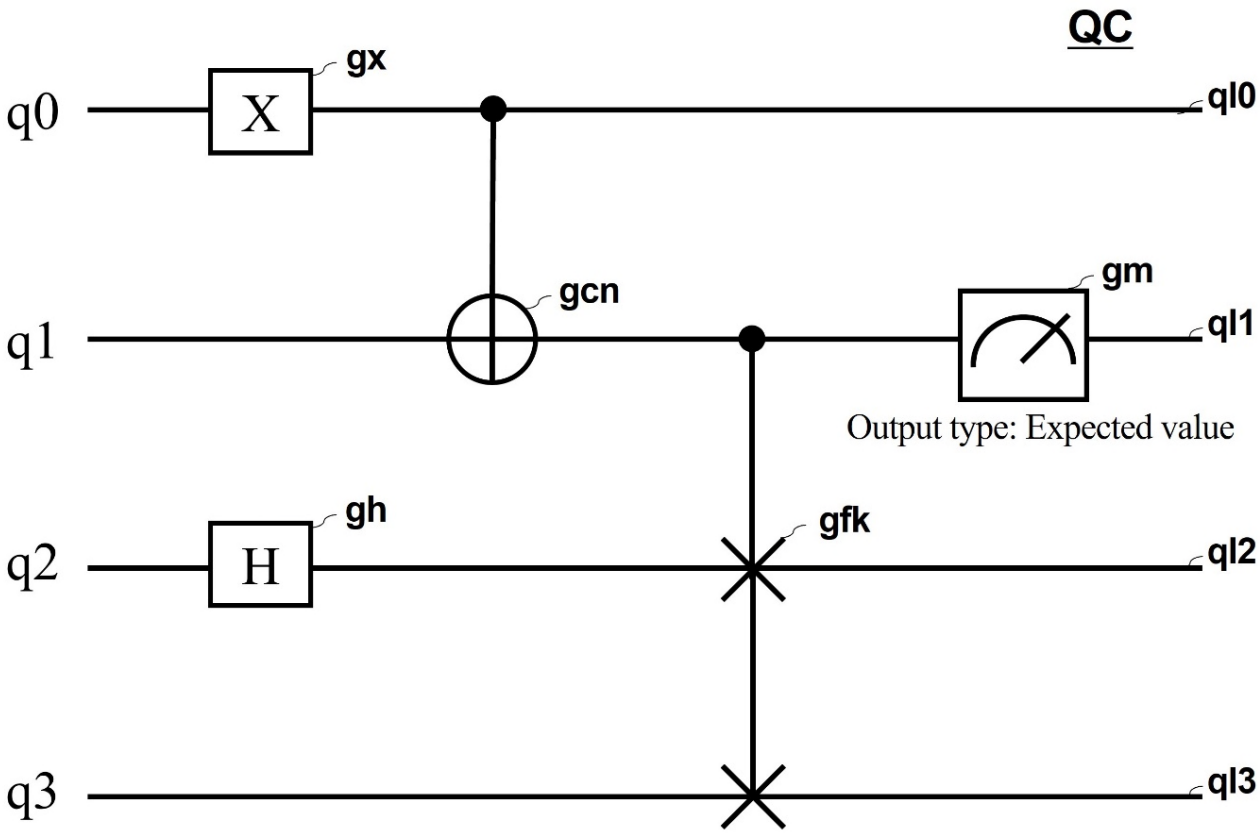

QC
q0
X
gx
ql0
gcn
q1
gm
ql1
Output type: Expected value
q2
H
gh
gfk
ql2
q3
ql3

FIG. 9B

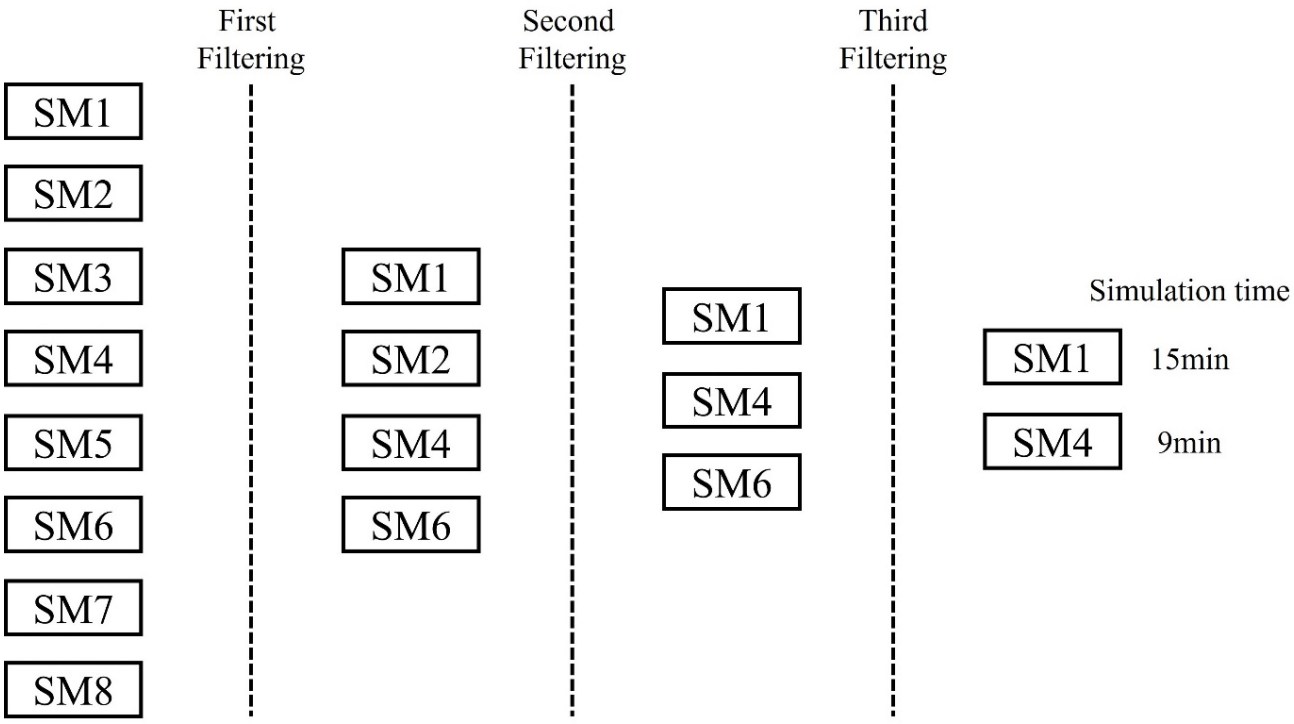

First Filtering
Second Filtering
Third Filtering
SM1
SM2
SM3
SM4
SM5
SM6
SM7
SM8
SM1
SM2
SM4
SM6
SM1
SM4
SM6
Simulation time
SM1
15min
SM4
9min

FIG. 10

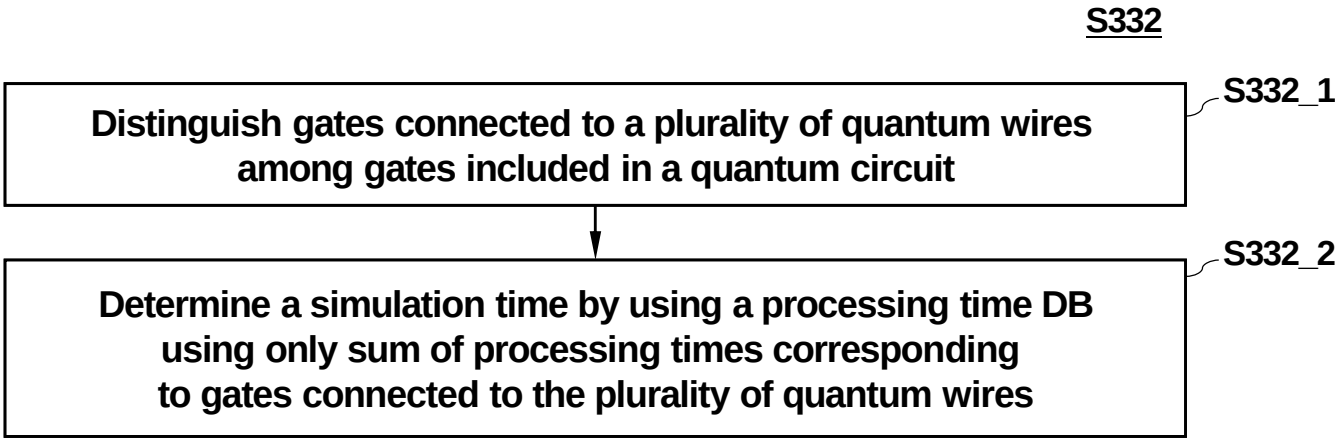
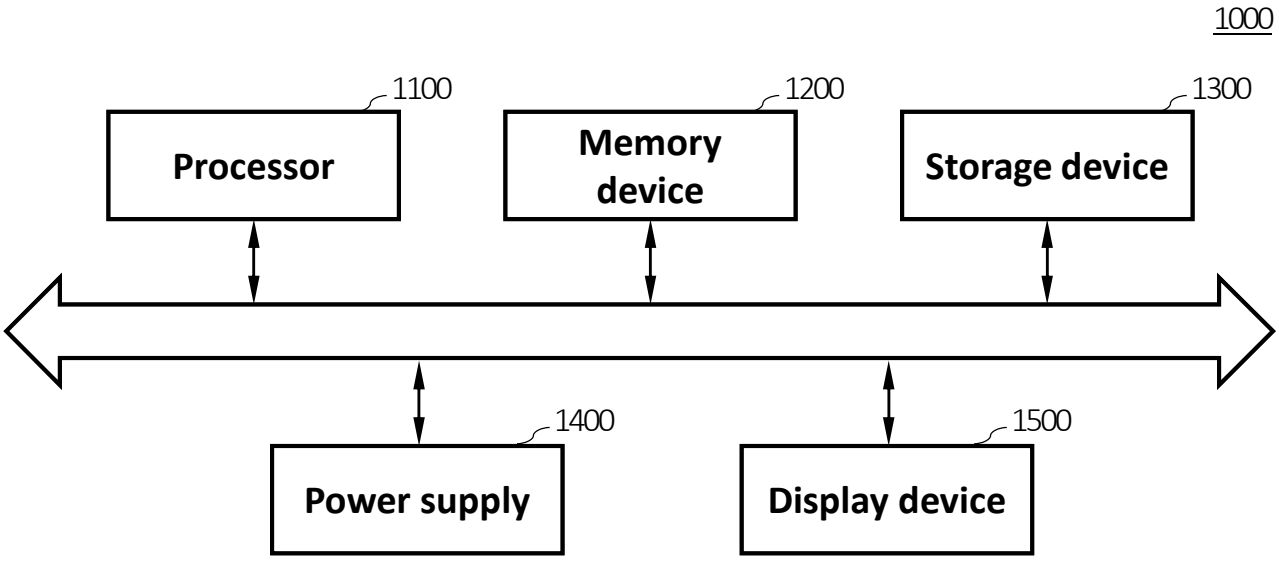

S332
Distinguish gates connected to a plurality of quantum wires among gates included in a quantum circuit
S332_1
Determine a simulation time by using a processing time DB using only sum of processing times corresponding to gates connected to the plurality of quantum wires
S332_2

FIG. 11


1000
1100
Processor
1200
Memory device
1300
Storage device
1400
Power supply
1500
Display device