The invention relates to an integrated circuit for the colour decoder of a PAL colour television receiver having an adding stage and a subtraction stage for the chrominance carriers from two lines succeeding one another in time and having an oscillator serving for the demodulation of the chrominance carrier.

It is known to combine the components necessary for the decoding of the chrominance carrier and the production of the colour-difference signals, particularly chrominance-carrier amplifiers, synchronous demodulators, reference-carrier oscillators, matrix circuits, amplifiers for the colour-difference signals, the line-frequency PAL and/or SECAM switches and PLL circuits, in an integrated circuit, a so-called chroma IC. Such an integrated circuit is fed with the modulated chrominance carrier and the sandcastle pulse and delivers the two colour-difference signals (B-Y) and (R-Y) at its outputs. Such an integrated circuit of the type TDA 3560 for a PAL decoder is described, for example, in "Funk-Technik", 1979, No. 9 Pages T 445 - T 448.

An integrated circuit for a PAL colour television receiver is also known (minutes of the 10th annual session of the FKTG in Munich from the 13th - 17th September 1982, pages 485 - 391) which also contains the adding stage and the subtraction stage for the PAL chrominance carriers from two lines succeeding one another in time, the so-called PAL matrix. In this case, the line delay line for acquiring the chrominance carrier of the preceding line in time is connected to terminals of the integrated circuit as an external component. For satisfactory operation of the so-called PAL decoder, a particularly accurate amplitude and phase adjustment is necessary for the chrominance carriers at the inputs of the adding stage and of the subtraction

stage because a vectorial addition and subtraction of the chrominance carriers is effected in the said stages. For these adjustments, therefore, an adjustable coil for the phase adjustment and an adjustable resistor for the amplitude adjustment are provided outside the integrated circuit. In addition, a crystal, as a standard frequency generator, is connected externally to the integrated circuit as a reference element for the synchronization of the reference-carrier oscillator contained in the circuit. Such external components are relatively expensive components. In addition, the coil and the resistor have to be adjusted manually, individually for each receiver, during the production of the colour television receiver, particularly because of tolerances in the values of the external line delay line.

It is the object of the invention to develop an integrated circuit of the kind described so that the expenditure on external components and in particular the manual expense for the adjustment of external components is reduced.

This problem is solved by the invention described in Claim 1. Advantageous further developments of the invention are described in the dependent claims.

The invention is based on recognition of the following: The components hitherto needed externally for the adjustment of certain parameters inside the integrated circuit can be replaced by an internal control circuit which automatically adjusts the particular parameters necessary. This has several advantages. In the first place, fewer external, adjustable components or synchronizing components are needed. Thus a former adjustable coil can be replaced by a coil with fixed inductance for example, or a potentiometer serving for the amplitude adjustment can be replaced by

a fixed resistor, as a result of which a saving is achieved. The external crystal tuned to the chrominance-carrier frequency, hitherto needed for the synchronization of the reference-carrier oscillators, can also be eliminated. In addition, the absence of the adjustable external components leads to a saving in expenditure on labour during the installation of the integrated circuit, that is to say the production of the colour television receiver, because the manual adjustment hitherto necessary for a plurality of parameters is eliminated. A further advantage consists in that the respective operating conditions to be adhered to are retained over a lengthy period of time of several years. If the particular mode of operation is adjusted, for example with an external trimmer, and deviations occur over the years through ageing of components, a manual re-adjustment is necessary as a rule. With the control circuit provided internally, this re-adjustment is not necessary because the control circuit always re-adjusts the particular mode of operation automatically again. In themselves, the control circuits provided internally represent a greater expenditure on circuitry than the external adjustable components. Additional expense on individual components or stages in an integrated circuit only increases the costs of such a circuit insignificantly. The advantage of the saving in external components for the adjustment is considerably greater than the disadvantage of the slight additional expense in the integrated circuit.

One example of embodiment of the invention is explained in connection with the example of an integrated circuit for a multi-standard colour decoder for NTSC-PAL and SECAM operation, with reference to the drawing. In this:

Figure 1 shows a block circuit diagram of the integrated circuit with the components still needed,

Figure 2 shows, in detail, the digital frequency control circuit illustrated in Figure 1 and

Figure 3 shows a graph to explain the mode of operation of the control circuit according to Figure 2.

The integrated circuit 1 illustrated in Figure 1 is fed with the sandcastle pulse SC at the terminal M and with the modulated chrominance carrier F at the terminals B and C. Capacitors for achieving the necessary time constants of the internal identification circuit 19 are connected to the terminals K and G. A crystal oscillator 2 is connected to the terminal H and delivers a stabilized frequency of 62.5 kHz. This crystal oscillator does not correspond to the crystal otherwise necessary with the chrominance-carrier frequency of 4.43 MHz for PAL or 3.58 MHz for NTSC. In this case, it is a question of a crystal which is in any case present elsewhere in the television receiver and which is contained, for example in a synthesizer or a tuner for example and the frequency of which does not have to coincide with the frequency of the chrominance carrier. The input of the line delay line 3 necessary for PAL and SECAM operation is connected to the terminals AC and AB and its output is connected to the terminals Y and X. At the terminals Q, P, the circuit 1 delivers the colour-difference signals (B-Y) and (R-Y) for the picture reproduction.

The symbols used in Figure 1 have the following meaning:

P - Output on identification of a PAL signal by recognition of the PAL colour burst switched over in phase in accordance with line frequency,

N3 - Output on identification of an NTSC signal with the NTSC chrominance-carrier frequency of 3.58 MHz,

N4 - Output on identification of an NTSC signal with a chrominance-carrier frequency of 4.43 MHz, for example in NTSC video recorders with PAL chrominance-carrier frequency,

S - Output on identification of a SECAM signal by evaluation of the typical SECAM chrominance-carrier frequencies,

A - Operation of the circuit for signals with amplitude modulation, that is to say NTSC and PAL. The switches designated by "A" are switched out of the position illustrated, during operation with amplitude modulation.

F - Operation of the circuit for signals with frequency modulation, that is to say SECAM. The switches designated by "F" are switched out of the position illustrated, during operation with frequency modulation.

N - Operation for an NTSC signal. The switches designated by "N" are switched out of the position illustrated, during NTSC operation.

N' - Operation for NTSC with a chrominance-carrier frequency of 3.58 MHz. The switches designated by "N'" are switched out of the position illustrated, for NTSC with 3.58 MHz.

BG - (burst gate) - Gating of the colour burst. At the positions designated by "BG", the signal path is only connected through for the duration of the colour burst. For the duration of the colour burst, the switches designated by "BG" are switched out of the position illustrated.

LP - (line pulse) - line-frequency pulse which is obtained from the sandcastle pulse.

FP - (frame pulse) - Vertical-frequency pulse with 50 Hz which is obtained from the sandcastle pulse.

H/2* - Half-line frequency control voltage with correct switching phase for the PAL and SECAM switches.

Various modes of operation for NTSC, PAL and SECAM and the individual internal control and synchronizing operations will be described in succession below.

NTSC Operation

The switch N' is closed so that the band-pass filter 4 between the input terminals B and C is switched over to the lower chrominance-carrier frequency of 3.58 MHz through the connecting in of the capacitor 5. The NTSC chrominance carrier F passes from the terminal B through the stage 60 serving for the automatic control of the colour gain (AGC) and the controllable phase shifter 6 to the adding stage 7 and the subtraction stage 8. The switch N1, which is likewise actuated, switches off the amplifier 39 so that the upper inputs of the stages 7, 8 do not receive any signal. The chrominance carrier F thus appears, unaltered, at the two inputs of the synchronous demodulators 9, 10. The synchronous demodulator 9 is fed by the reference-carrier oscillator VCO3 with a reference carrier with the constant phase 0° and delivers the colour-difference signal (B-Y) at the terminal Q via the change-over switch 11 (connections in full lines) and the switched-off deemphasis stage 12. The synchronous demodulator 10 receives a reference carrier with the constant phase +90° from the oscillator VCO3 and delivers the colour-difference signal (R-Y) at the terminal L via the change-over switch 11 and the switched-off deemphasis stage 13. The switch N2 is opened. As a result, the half-line frequency control voltage H/2* does not reach the synchronous demodulator 10 so that the switching-over of phase of the reference carrier between +90° and -90° indicated there and only

necessary during PAL operation, does not take place. In the phase comparison stage 14, which is controlled by the gating pulse BG so as to be effective only for the duration of the colour burst, the colour burst from the output of the adding stage 7 and the output voltage of the reference-carrier oscillator VCO3 are compared. The control voltage obtained as a result controls the reference-carrier oscillator CVO3 through the closed switch 15 and the adding stage 16 so that this oscillator oscillates at the chrominance-carrier frequency of 3,58 MHz. The further synchronization through the crystal oscillator 2 is described later under the heading "synchronization of the oscillators". Thus, as a result of the blocking of the amplifier 39, the line delay line 3, which is not necessary during NTSC operation, is inoperative and the upper inputs of the stages 7 and 8 do not receive any signal.

PAL Decoding

The switch N1 is opened and the amplifier 39 is effective. The undelayed chrominance carrier from the phase shifter 6 and the chrominance carrier delayed by the duration of one line from the controllable amplifier 39 reach the stages 7, 8 acting as a PAL matrix and are there split into the two chrominance-carrier frequency signals F(B-Y) and $\pm$F(R-Y). These are demodulated in the synchronous demodulators 9, 10 so that the colour-difference signals (B-Y) and (R-Y) appear at the terminals Q and L. Through the closed switch N2, the half-line frequency control voltage H/2* reaches the synchronous demodulator 10 and there causes the necessary switching over, at line frequency, of the phase of the reference carrier serving for the demodulation and coming from the oscillator VCO3, between +90° and -90°.

PAL Amplitude Adjustment

For the satisfactory operation of the PAL matrix 7, 8, the chrominance carriers at each of the two inputs of these stages must have the same amplitude. For this purpose, a potentiometer is usually provided at the output of the delay line 3 in known circuits. The internal control circuit provided to adjust the amplitude equalization works as follows: The chrominance-carrier frequency output signals of the stages 7, 8 are supplied to the phase comparison stage 17 which is effective, through the gating pulse BG, only for the duration of the colour burst. With correct amplitude adjustment, the colour burst components at the outputs U, V of the stages 7, 8 have a phase rotation of 90° in relation to one another so that the phase comparison stage 17 does not deliver any control voltage. When there is a difference in amplitude, this angle alters. With an amplitude deviation in the one direction, it becomes larger and with an amplitude deviation in the other direction, it becomes smaller. As a result, the correcting variable at the output of the phase comparison stage 17 becomes larger or smaller and controls the gain of the amplifier 39 in the sense that the colour burst components at the inputs of the phase comparison stage 17 are displaced in phase by 90° in relation to one another. Then assurance is provided that the chrominance carriers at the inputs of the stages 7, 8 have the same amplitude. Thus an external adjuster for adjusting this amplitude condition is no longer needed.

PAL Phase Adjustment

For the satisfactory mode of operation of the PAL matrix with the stages 7, 8, the basic phase, that is to say the phase in a chrominance carrier with the (B-Y) axis, must coincide at the two inputs of these

stages. For this purpose, the inductance at the output of the delay line 3 is adjustable in known circuits. With correct phase adjustment, the colour burst component at the output V of the subtraction stage 8 has alternately, from line to line, the phase +90° of the axis (R-Y) and the phase -90° of the axis -(R-Y). This colour burst component reaches the input of the synchronous demodulator 10. As a result of the pulse BG, the line-frequency switching over of the (R-Y) reference carrier phase between +90° and -90° is discontinued during the line fly-back time so that the colour burst component is continuously demodulated at the axis +90°. As a result of the switching over of the phase of the colour burst component at the output V between +90° and -90°, pulses of the same amplitude and with polarity alternating from line to line appear at the output of the synchronous demodulator 10 each time for the duration of this colour burst component. These pulses are evaluated time selectively by the gate 18 which is controlled by the gating pulse BG so as to be transmissive only for the duration of the colour burst. Because of the same amplitude and the alternately different polarity, a control voltage with the value zero results at the control input of the phase shifter 6 through filtering the pulses. Thus this control voltage does not alter the correct phase rotation of the phase shifter 6. Let it be assumed that as a result of an incorrect phase adjustment, the angle between the colour bursts with the desired phase 135° and the desired phase 225° alters at the inputs of the subtraction stage 8. Then the pulses obtained from the colour burst components again have a different polarity from line to line at the output of the synchronous demodulator 10. According to the direction of the phase deviation, however, the

amplitude of the positively directed pulses becomes greater and of the negatively directed pulses less, or vice versa. As a result, a positive or negative control voltage appears at the control input of the phase shifter 6 after appropriate filtering. This control voltage alters the phase rotation of the phase shifter 6 in the sense that the colour bursts at the inputs of the subtraction stage 8 and hence also of the adding stage 7 again have the correct desired phases of 135° and 235° As a result, assurance is provided that even the modulated chrominance carriers have the correct phase in relation to one another at the inputs of the stages 7, 8 during the line trace interval.

PAL Switching Phase

As already described under the heading "PAL Phase Adjustment", pulses with polarity reversed from line to line appear at the output of the synchronous demodulator 10. Since these pulses are obtained from the colour burst, they contain information for the correct switching phase of the PAL change-over switch, which phase is specified by the colour burst. These pulses reach the identification circuit 19 so that the control voltage H/2*, which is correct in the switching phase, always appears at the output of this circuit 19. The said circuit for the correction of the PAL switching phase is described in more detail in French Patent Application No. 8220772. In addition, the identification circuit 19 identifies the standard of the particular signal received, for the switching-over of standards, from the line-frequency switching over of the pulse train from the output of the synchronous demodulator 10. This function will be described in more detail later in the section "Switching-over of standards".

SECAM Decoding

The resistor 20 is disconnected by the switch at the terminal E, which is closed only for signals with amplitude modulation. As a result, the band-pass filter 4 is less damped and causes the correction of the chrominance carrier, necessary during SECAM operation, by means of a bell-shaped pass curve (bell) within the bandwidth of the chrominance carrier. With amplitude modulation (PAL, NTSC), the bell-shaped pass curve necessary for SECAM operation for the correction of the chrominance carrier, is undesired. Therefore, during these modes of operation, the band-pass filter 4 is damped by the resistor 20 so that the pass curve of the band-pass filter 4 does not drop appreciably over the bandwidth of the modulated chrominance carrier. The undelayed SECAM chrominance carrier from the output of the phase shifter 6 and the SECAM chrominance carrier delayed by the period of one line from the output of the amplifier 39 reach the SECAM cross-connecting switch 21 which is actuated at line frequency and is controlled by the half-line frequency control voltage H/2* and which delivers separately, at its two outputs, the two line-sequentially transmitted SECAM chrominance carriers with the different frequencies of 4.406 MHz and 4.250 MHz. These chrominance carriers are supplied to two separate FM demodulators. These FM demodulators are constructed in the form of PLL FM demodulators and contain the two oscillators VCO1 and VCO2. Through the PLL control loop with the phase comparison stage 22 and the adding stage 23, the frequency of the oscillator VCO2 is always regulated to the frequency of the modulated chrominance carrier supplied. This means that the output voltage of the phase comparison stage 22 is proportional to the frequency of the chrominance carrier and thus represents the colour-difference

signal (R-Y). This passes via the change-over switch 11 (connection in broken line) and the deemphasis stage 13 switched on through F to the terminal L. The phase comparison stage 24, the adding stage 25 and the oscillator VCO1 work in a corresponding manner for the colour-difference signal (B-Y). This passes via the change-over switch 11 and the deemphasis stage 12, which is switched on, to the terminal Q. An additional synchronization of the oscillators VCO1 and VCO2 by the crystal oscillator 2 is described under the heading "Synchronization of the oscillators". The phase comparison stages 22, 24 are controlled by the vertical-frequency pulse FP so as to be inoperative. This time is used to match the D/A converters 42, 43 connected to the outputs of the registers 40,41.

Amplitude control for SECAM

The amplitude adjustment with the amplifier 39, described for PAL operation, is also effective for SECAM operation. During SECAM operation, the SECAM chrominance carriers likewise reach the PAL matrix 7,8. This is not actually used for the production of the colour signal. A control voltage likewise results at the control input of the amplifier 39 through multiplication of the SECAM chrominance carriers in the phase comparison stage 17 which is controlled so as to be effective only for the duration of the colour burst. This control voltage controls the gain of the amplifier 39 in the sense that the SECAM chrominance carriers have the same amplitudes at the output of the phase shifter 6 and at the output of the amplifier 39, that is to say at the inputs of the SECAM switch 21.

SECAM Switching Phase

The SECAM chrominance carrier with frequency switched over from line to line reaches the phase

comparison stage 26 which, together with the oscillator VCO3 and the adding stage 16, forms a PLL circuit. As a result, the frequency of the oscillator VCO3 is adjusted to the two different SECAM chrominance-carrier frequencies alternately from line to line. This adjustment is effected in the same manner as that of the oscillators VCO1 and VCO2 for the SECAM decoding. If the oscillator VCO3 is adjusted to the mean value 4.328 MHz of the two different chrominance-carrier frequencies, the control voltage at the output of the phase comparison stage 26 has different polarity from line to line. By means of the switch 27, which is closed by the pulse BG for the duration of the unmodulated SECAM chrominance-carrier oscillations at the beginning of each line, the control voltage is evaluated during these chrominance-carrier oscillations. As a result, a voltage with different polarity from line to line is likewise obtained at the input of the identification circuit 19 and should be equated with the pulse train from the synchronous demodulator 10 during PAL operation. Thus the two lower right-hand inputs of the identification circuit 19 receive practically the same pulse train during PAL operation and during SECAM operation. Thus during SECAM operation, the correct switching phase of the control voltage H/2* for the change-over switch 21 is likewise ensured in the identification circuit 19 by the pulse train from the output of the phase comparison stage 26.

Synchronization of the oscillators

The voltage delivered by the crystal oscillator 2 with the constant frequency fo of 62.5 kHz is supplied, via the terminal H, to the circuit 28 which contains a counter and a pulse generator. By counting the cycles of the reference-frequency voltage, the stage 28 generates a measuring pulse 29 with a defined duration of about

850 µs to 1 ms. This measuring pulse 29 serves as a time window in the digital frequency control circuit 30. During this time, the cycles of the oscillations supplied are counted and hence a frequency measurement is effected in the circuit 30. In the position b of the change-over switch 31 provided with four inputs a, b, c, d, the reference carrier passes from the oscillator VCO3 to the input of the control circuit 30. The frequence of the reference carrier is measured in the control circuit 30 and compared with the desired value likewise obtained from the reference-frequency voltage. In the event of a deviation, a digital signal reaches the register 32. From the output voltage of this, an analogue control voltage is obtained in the D/A converter 33 and is added, in the adding stage 16, to the control voltage from the phase comparison stage 14. After each measuring time, the frequency of the oscillator VCO3 is altered by the analogue control voltage until it has the desired value. Thus the oscillator VCO3 is adjusted by the frequency control circuit 30 and is additionally adjusted to the correct frequency by analogue control voltages from the colour burst. This is necessary for the following reason: A precise frequency and phase control of the oscillator VCO3 by the colour burst alone is not possible. The colour burst not only has the singular PAL chrominance-carrier frequency of 4.43361875 MHz but also spectral lines each spaced apart at half the line frequency. Thus the oscillator may also lock in on a spectral line which differs from the correct frequency by a whole multiple of the line frequency. Then a satisfactory synchronous demodulation would no longer be possible. With the known use of a crystal, this is not possible since, because of the extremely narrow bandwidth of a crystal of about 100-200 Hz, the oscillator cannot

lock in on a side spectral line. Now in order to synchronize the oscillator VCO3 to the correct frequency, the additional adjustment is effected by the digital frequency control circuit 30 which in turn is controlled by the crystal-stabilized voltage at the terminal H.

The oscillators VCO1 and VCO2 are adjusted to the correct frequency in the same manner via the registers 40, 41 and the D/A converters 42, 43. Thus the analogue control voltage of the D/A converters adjusts the correct resting frequency of the oscillators VCO1 and VCO2, that is to say the centre frequency of the modulated SECAM chrominance carriers, and the analogue control voltage from the outputs of the phase comparison stages 22, 24 alters this frequency according to the frequency modulation of the SECAM chrominance carriers.

Thus, during the individual modes of operation, the oscillators VCO1, VCO2 and VCO3 are adjusted to the following frequencies:

SECAM operation:

VCO1 with 4.250 MHz for the transmission of the signal (B-Y)

VCO2 with 4.406 MHz for the transmission of the signal (R-Y)

VCO3 to the centre frequency (4.250 + 4.406)/2 = 4.328 MHz.

PAL operation:

VCO3 with 4.433 MHz

NTSC operation N4:

VCO3 with 4.433 MHz

NTSC operation N3:

VCO3 with 3.58 MHz.

The measurement of the frequencies of the oscillators VCO1 and VCO2 and VCO3 is effected by the switch 31 sequentially from field to field, during the vertical blanking time in each case.

Thus the switch 31 is stepped on by the pulse FP at the beginning of each field. In position b, the frequency of the oscillator VCO3 is measured in the control circuit 30, in position c that of the oscillator VCO2 and in position d that of the oscillator VCO1, and the deviation from the desired value is converted into a digital correcting variable for the register.

Band-pass filter tuning

The band-pass filter 4 at the terminals B, C is tuned to the frequency of the chrominance carrier in each case. This tuning must be precisely adhered to, particularly with the SECAM chrominance carrier, because the pass curve formed causes the deemphasis for the modulated SECAM chrominance carrier. The internal oscillator 34 is so coupled to the band-pass filter 4 that its oscillating frequency depends on the resonant frequency of the band-pass filter 4. The output voltage of the oscillator 34 passes, via the change-over switch 31 in its position a for the duration of one field, likewise to the control circuit 30 and is there evaluated. On a deviation in the resonant frequency, the oscillating frequency of the oscillator 34 alters. A digital signal corresponding to the deviation is generated in the control circuit 30 and supplied to the register 35. According to the deviation, the register 35 connects in or disconnects additional capacitors between the terminals B and C in such a manner that the resonant frequency of the band-pass filter 4 is adjusted to its correct value.

Thus the change-over switch 31 works differently for NTSC, PAL and SECAM. During NTSC operation it only assumes the positions a and b because the SECAM demodulators are not needed. During PAL operation, the same applies. During SECAM operation, the change-over switch 31 assumes all the positions a; b, c, d

sequentially because then all four oscillators 34, VCO1, VCO2 and VCO3 are operative.

The registers 35, 32, 41, 40 are connected in parallel by their inputs and are controlled sequentially by digital signals from the control circuit 30 in accordance with the measuring cycle determined by the change-over switch 31. For this purpose, the registers 35, 32, 41, 40 are controlled successively in time, from field to field, via the control lines C1, C2, C3, C4, so as to be operative for the duration of the vertical blanking time of the control circuit 30. If the control circuit 30 delivers the digital signal for the frequency control of the oscillator CVO3 for example, only the register 32 is activated via the line C2 while the registers 35, 41, 40 are controlled via the lines C1, C3, C4 so as to be inoperative.

Hue adjustment for NTSC

During NTSC operation, a phase control of the chrominance carrier with the phase shifter 6 is not necessary because the stages 7, 8 only receive one chrominance carrier and so the adjustment of a phase relationship between two chrominance carriers supplied is not necessary. During NTSC operation, the phase shifter 6 is utilized for the manual adjustment of the hue. For this purpose, a control voltage which can be adjusted manually externally, passes from the terminal Z to the phase shifter 6, the phase rotation of which is adjustable thereby. The phase shifter 6 is controlled by the voltages N and BG supplied, so that the alteration in the phase rotation is effected only during the pefiod of the colour burst and the phase of the modulated chrominance carrier remains unaltered during the line trace interval. On an alteration in the phase rotation of the phase shifter 6 during the line fly-back time, the phase of the colour burst alters at the input of the phase comparison

stage 14 and hence the phase of the reference carrier produced in the oscillator VCO3. Since the synchronous demodulation is then effected on another demodulation axis, the hue in the picture reproduced alters in the desired manner. It is also possible, during the hue adjustment, to leave the phase of the colour burst unaltered and to alter the phase of the modulated chrominance carrier during the line trace interval. The first-mentioned solution with alteration of the phase of the colour burst has the advantage, however, that the phase change is only necessary for the colour burst and not for the modulated chrominance carrier during the line trace interval. This is an advantage because disturbances in the change in the phase rotation can affect the modulated chrominance carrier directly but are suppressed in the control path of the oscillator VCO3 because of the high time constant.

The search circuit 44 is provided for switching over the standard. The search circuit 44 is actuated by the FP pulse and switches the whole circuit over to the individual modes of operation, namely amplitude modulation for NTSC and PAL (A), NTSC with 4.43 MHz (N), NTSC with 3.58 MHz (N') and SECAM (F) with the switches illustrated, via the outputs A, N, N' and F in succession, each for the duration of about 6-8 complete frames. At the same time, the search circuit 44 interrogates the outputs of the identification circuit 19 as to whether a signal with the standard of the particular mode of operation set is being received. As soon as the identification circuit 19 indicates the presence of a signal of the particular mode of operation set, the search circuit 44 is stopped and locks in on this position so that now the signal of the particular standard can be received. Let it be assumed that

an NTSC signal with 3.58 MHz is applied to the input terminal B, the search circuit 44 is at first in the position A and interrogates the output P of the identification circuit 19. Since no PAL signal is being received, the identification circuit 19 delivers the logical value "0" at the output P. The search circuit 44 thereupon switches over to the mode of operation N = NTSC with 4.43 MHz and interrogates the output N4 of the identification circuit 19. Since this signal is likewise not being received, the voltage value "0" appears at the output N4 and the search circuit 44 switches over to the mode of operation N' and interrogates the output N3 of the identification circuit 19. In this case, the switch N' is also closed so that the band-pass filter 4 is tuned to the frequency of 3.58 MHz by the capacitor 5. The identification circuit 19 now detects a signal of the mode of operation set, namely the NTSC signal with 3.58 MHz, and delivers the logical voltage value "1" at the output N3. The search circuit 44 now recognizes that, in the mode of operation set, a signal of the associated standard is being received and locks in this position. The NTSC signal received with 3.58 MHz can now be processed by the integrated circuit 1. If no signal at all which can be recognized by the circuit 1 is being received, the search circuit 44 continues to run cyclically and goes on interrogating until a signal which can be recognized by the circuit 1 is again detected.

The mode of operation of the frequency control of the oscillator VCO and of the oscillator 34, indicated in Figure 1, is described in more detail with reference to Figure 2. The components which are already contained in Figure 1 are provided with the same reference numerals. The frequency f1 produced

by the oscillator VCO1 is measured during a defined reference time. For this purpose, the measuring pulse 29 is produced from the reference frequency fo of 62.5 kHz by means of the counter 28 and controls the gate 46 so as to be transmissive. The frequency f1 produced by the oscillator VCO1 is applied, via the cyclically actuated change-over switch 31, to the input of the digital comparator 47. Through a control signal at the "MODE" input of the comparator 47, this works alternately as a shift register and as a comparing counter which compares the values read in from the gate 46 with a value preset by the director 48. The shift pulses 49 serve for the read-in and readout of the comparator 47. During the frequency control, a deviation between actual value and desired value is generally detected as a difference in the first instance. The voltage corresponding to this difference is added, in the adding stage 50, to the value which is stored in the register 40 and was obtained from a preceding measurement and which passes from the register 40, via the change-over switch 51 turning cyclically, to the adding stage 50.

Let it be assumed that this has the value "0" at first. The result from the adding stage 50 reaches the register 40 clocked via the cyclic change-over switch 52. An analogue control voltage is formed from the digital value present in the register 40, by means of the D/A converter 42, and passes to the oscillator VCO1 to control the frequency. As a result, a new output frequency f1 appears which again enters the digital comparator 47 and is there compared with the desired value from the director 48. A new, smaller differential value appears which is added, in the adding stage 50, to the value in the register 40 obtained from the preceding measurement and is

again read into the register 40. After that, a new control voltage for the oscillator VCO1 is again obtained through the D/A converter 42. These operations are repeated until the differential value has become "0". Then nothing more is added in the adding stage 50 and the value in the register 40 as well as the analogue control voltage delivered by the D/A converter 42 now assume a stable state at which the frequency f1 has its desired value. When the comparator 47 detects the differential value "0", that is to say when all the outputs of the comparator 47 assume the state "0", the switch 54 is opened through the detector 53 so that no further shift pulses 49 can reach the register 40.

The procedure described can also be applied to any desired number of oscillators for the production of a plurality of stable frequencies f1 - f4, as indicated by the additional oscillators VCO2, VCO3, 34 and the register 35 illustrated. Resonant frequency of the band-pass filter 4 and hence frequency of the oscillator 34 are controlled from the register 35 by connecting in and disconnecting capacitors by means of digital signals in the manner described with reference to Figure 1.

The course of the control operation is illustrated by a graph in Figure 3. The graph shows the function of the measured oscillator frequency f depending on the value present in the register and hence the controlling control voltage. The desired value of the frequency f is entered as "100" on the ordinate. The function is represented by the curve 56. It is assumed that the voltage value produced by the D/A converter adjusts the oscillator to a frequency which produces the measured value "60" which differs from the desired value "100" by the value -40. The value of the register is reduced by this difference by means of the adding stage 50.

A new frequency value of "90" is given by the function. The new difference is now -10. Thereupon, the value "99" is set after a further control operation. It can be seen that the oscillator frequency f steadily settles down to the desired value step by step. The individual points to which it is adjusted are represented by the figures 1, 2, 3, 4, the figure 1 representing the initial value of the frequency f and the figure 4 the final desired value of the frequency f.

The simultaneous use of the control circuits described and contained in the integrated circuit 1 is particularly advantageous in an integrated circuit because the number of components inside an integrated circuit does not appreciably influence the costs of the circuit. The circuits described may, however, also be used individually on their own in conventional circuitry in order to solve the problems described.

* C L M S *

CLAIMS

1. An integrated circuit for the colour decoder of a PAL colour television receiver having an adding stage (7) and a subtraction stage (8) for the chrominance carriers from two lines succeeding one another in time and having an oscillator (VCO) serving for the demodulation of the chrominance carrier, characterised in that control circuits (17,39; 18,6) evaluating the colour bursts taken from the adding stage (7) and the subtraction stage (8) for the amplitude adjustment and the phase adjustment of the chrominance carriers (F) supplied to the adding stage (7) and the subtraction stage (8) are provided in the integrated circuit (1) and the integrated circuit (1) contains a digital frequency control circuit (30) to determine the frequency of the oscillator (VCO), which circuit is connected to a terminal (H) for the connection of an external reference-frequency voltage source (2).

2. A circuit according to claim 1, characterised in that a control voltage for controlling the amplification (stage 39) of the undelayed or delayed chrominance carrier (F) is obtained for the amplitude adjustment by phase comparison (17) of the colour bursts at the outputs of the adding stage (7) and the subtraction stage (8).

3. A circuit according to claim 1, characterised in that for the amplitude adjustment during SECAM operation, the SECAM chrominance carriers of lines succeeding one another in time are applied to the inputs of a phase comparison stage (17) of which the output voltage appearing during the period of the unmodulated SECAM chrominance-carrier oscillations at the beginning of each line is used to control the amplification of the undelayed or delayed SECAM chrominance carrier.

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4. A circuit according to claim 1, characterised in that a control voltage to control the phase shift of a phase shifter (6) lying in the path of the undelayed or delayed chrominance carrier is obtained for the phase adjustment by evaluation of the phase of the colour burst appearing at the output of the adding stage (7) or the subtraction stage (8) in relation to a fixed modulation axis (V).

5. A circuit according to claim 4, characterised in that the phase shifter (6) is utilized during NTSC operation (N) for the manual adjustment of the hue.

6. A circuit according to claim 5, characterised in that an externally adjustable voltage appearing at a terminal (Z) of the circuit (1) is applied to a control terminal of the phase shifter (6).

7. A circuit according to claim 5, characterised in that the variation in the phase shift of the phase shifter (6) to adjust the hue is effective only during the period of the colour burst or only during the line trace interval.

8. A circuit according to claim 1, characterised in that the PAL oscillator and/or an NTSC reference-carrier oscillator (VC03) is synchronized both by the frequency control circuit (30) and by the colour burst through a PLL circuit (14-16).

9. A circuit according to claim 1, characterised in that a measuring pulse (29) of defined duration is produced from the reference-frequency voltage and the particular frequency measurement is effected in the frequency control circuit (30) by counting the number of cycles of the particular voltage to be measured during the period of the measuring pulse (29).

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10. A circuit according to claim 1, characterised in that the measurement of the frequencies of a plurality of oscillators (VC01, VC02, VC03, 34) is effected cyclically in succession, in that an input of the frequency control circuit (30) is switched over, by a change-over switch (31), cyclically in succession between the outputs of the oscillators.

11. A circuit according to claim 1, characterised in that for a plurality of synchronizing functions, the output of the frequency control circuit (30) feeds separate registers (32, 41, 40) cyclically in succession, the outputs of which registers produce control voltages for the synchronizing functions through D/A converters (33, 43, 42).

12. A circuit according to claim 11, characterised in that the output of the frequency control circuit (30) is connected in parallel with the inputs of the registers (35, 32, 41, 40) and the registers are activated cyclically in succession.

13. A circuit according to claim 10, 11 or 12, characterised in that the cyclic switching over from field to field and the measurement or activation are effected during the vertical blanking time.

14. A circuit according to claim 1, characterised in that an internal oscillator (34) is connected to the input of the frequency control circuit (30) and is wired so that its frequency depends on the resonance frequency of an external oscillatory circuit (4) and in that a correcting variable is obtained by measuring the oscillator frequency and is superimposed on the internal reactances of the oscillatory circuit (4) in such a manner that the oscillatory circuit (4) has the desired resonant frequency.

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15. A circuit according to claim 14, characterised in that the oscillatory circuit (4) is part of a band-pass filter (4) lying in the path of the chrominance carrier (F).

16. A circuit according to claim 9, characterised in that the voltage obtained by the frequency measurement is fed to a digital comparator (47) which is fed with the desired frequency value and which works alternately as a shift register and as a comparative counter (Figure 2).

17. A circuit according to claim 16, characterised in that a differential voltage obtained in the comparator (47) by desired/actual comparison is added, in an adding stage (50), to the voltage stored in a register (40) and obtained from a preceding measurement and the sum signal serves for the frequency control (Figure 2).