

162162

SOI TRANSISTOR WITH POLYSILICON SEED

ABSTRACT



G00002

Short channel effects are effectively suppressed by steep impurity concentration gradients which can be placed with improved accuracy of location and geometry while relaxing process tolerances by implanting impurities (14) in a polysilicon seed adjacent to a conduction channel of a transistor and diffusing impurities (14) therefrom into the conduction channel. The polysilicon seed also allows the epitaxial growth of polysilicon source/drain contacts (10) therefrom having a configuration which minimizes current density and path length therein while providing further mechanical advantages.

FIG. 1