

METHODS AND DEVICES USING PVD RUTHENIUM

TECHNICAL FIELD

[0001] The present disclosure relates generally to methods and electronic devices
5 incorporating physical vapor deposited (PVD) ruthenium. In particular, the present
disclosure related to methods and electronic devices in which PVD Ru layer replaces
PVD tungsten to provide lower resistivity films.

BACKGROUND

[0002] The continuing miniaturization of semiconductor integrated circuits has
10 forced many conventional structures to change and has required the accompanying
need to improve the processes used to create the new structures. A conventional
MOS (metal oxide semiconductor) transistor gate structure for larger feature sizes
includes a deposited tungsten nitride barrier layer and a tungsten via layer. Sputtering
is the generally preferred method of depositing the WN barrier layer and the W via
15 layer. However, tungsten resistivity increases with reduced film thickness, resulting in
a decrease in usefulness for future node DRAM in bitline applications.

[0003] Therefore, there is a need in the art for films and methods to deposit films
with lower bitline resistivity and insensitivity to oxidation.

SUMMARY

20 **[0004]** One or more embodiments of the disclosure are directed to methods of
forming a gate stack. A plasma sputter chamber including a target comprising
ruthenium and a pedestal for supporting a substrate to be sputter deposited in
opposition to the target is provided. The pedestal comprises a high current
electrostatic chuck at a temperature greater than or equal to about 350 °C. Krypton is
25 flowed into the chamber and excited into a plasma to deposit a ruthenium layer on the
substrate. An anneal chamber is provided and the ruthenium layer on the substrate is
annealed at a temperature greater than or equal to about 500 °C.

[0005] Additional embodiments of the disclosure are directed to gate stacks comprising: a polysilicon layer on a substrate; a silicide layer on the polysilicon layer; a barrier layer on the silicide layer; a ruthenium layer on the barrier layer; and a spacer layer comprising a nitride on sides of the ruthenium layer. The ruthenium layer
5 comprises substantially no ruthenium nitride after formation of the spacer layer.

[0006] Further embodiments of the disclosure are directed to methods of forming a gate stack. A polysilicon layer is formed on the substrate. A silicide layer is formed on the polysilicon layer. The silicide layer comprises titanium silicide with a thickness of about 20 Å. A barrier layer is formed on the silicide layer. The barrier layer
10 comprises one or more of TiN, TaN, WN or TiSiN. An optional interface layer is formed on the barrier layer. A PVD Ru layer is deposited on the barrier layer or the optional interface layer. The PVD Ru layer is deposited with the substrate on a high current electrostatic chuck comprising a high resistivity ceramic at a temperature greater than or equal to about 350 °C in a krypton environment. The PVD Ru layer
15 has a thickness in the range of about 100 Å to about 300 Å. The PVD Ru layer is annealed at a temperature greater than or equal to about 500 °C. A spacer layer is formed on the sides of the annealed PVD Ru layer. The spacer layer comprises SiN and forms substantially no ruthenium nitride.

BRIEF DESCRIPTION OF THE DRAWINGS

[0007] So that the manner in which the above recited features of the present invention can be understood in detail, a more particular description of the invention, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this invention and are
25 therefore not to be considered limiting of its scope, for the invention may admit to other equally effective embodiments.

[0008] FIG. 1 gas stack in accordance with one or more embodiment of the disclosure;

[0009] FIG. 2 shows a schematic cross-sectional view of a physical vapor
30 deposition chamber in accordance with one or more embodiment of the disclosure;

[0010] FIG. 3 shows a graph of the metal resistivity for ruthenium and tungsten films as a function of film thickness; and

[0011] FIG. 4 shows a graph of the resistivity of the ruthenium film as a function of electrostatic chuck temperature.

5 DETAILED DESCRIPTION

[0012] Before describing several exemplary embodiments of the invention, it is to be understood that the invention is not limited to the details of construction or process steps set forth in the following description. The invention is capable of other embodiments and of being practiced or being carried out in various ways.

10 **[0013]** A "substrate" as used herein, refers to any substrate or material surface formed on a substrate upon which film processing is performed during a fabrication process. For example, a substrate surface on which processing can be performed include materials such as silicon, silicon oxide, strained silicon, silicon on insulator (SOI), carbon doped silicon oxides, amorphous silicon, doped silicon, germanium,
15 gallium arsenide, glass, sapphire, and any other materials such as metals, metal nitrides, metal alloys, and other conductive materials, depending on the application. Substrates include, without limitation, semiconductor wafers. Substrates may be exposed to a pretreatment process to polish, etch, reduce, oxidize, hydroxylate, anneal and/or bake the substrate surface. In addition to film processing directly on the
20 surface of the substrate itself, in the present invention, any of the film processing steps disclosed may also be performed on an under-layer formed on the substrate as disclosed in more detail below, and the term "substrate surface" is intended to include such under-layer as the context indicates. Thus for example, where a film/layer or partial film/layer has been deposited onto a substrate surface, the exposed surface of
25 the newly deposited film/layer becomes the substrate surface.

[0014] As used in this specification and the appended claims, the terms "precursor", "reactant", "reactive gas" and the like are used interchangeably to refer to any gaseous species that can react with the substrate surface.

30 **[0015]** In one or more embodiments of the disclosure, lower resistivity Ru films are deposited with a high temperature bias able electrostatic chuck (ESC). Some

embodiments use a Kr sputtered Ru process in a temperature range of about 190 °C to about 550 °C. A two-step process may be used in some embodiments to improve the Ru resistivity as well as film surface morphology. With increased process temperatures in the range of about 190 °C to about 550 °C, the Ru resistivity
5 decreases with increased ESC temperature and annealing at a temperature in the range of about 680 °C to about 900 °C. By combining the high temperature Ru process and higher temperature anneal process, a lower resistivity Ru film can be formed as compared to a W film.

[0016] Referring to FIG. 1, one or more embodiments of the disclosure are directed
10 to a metal oxide semiconductor transistor gate stack 40. The transistor gate stack 40 includes highly doped source/drain (S/D) regions 10, 12 formed into a lesser doped silicon layer substrate 14, which may be formed epitaxially over a silicon wafer or even in a silicon-on-insulator (SOI) structure. A thin gate oxide layer 16 may be formed over the entire MOS area, possibly before the implantation and anneal steps for the
15 S/D regions 10, 12. Gate stacks 40 are formed over the gate oxide layer 16. The gate stack 40 of various embodiments comprises a polysilicon layer 20, a silicide layer 42, a barrier layer 44 and a ruthenium layer 46. An oxide-nitride-oxide (ONO) structure may be sandwiched within the polysilicon layer 20.

[0017] Source/Drain holes 26 may be photolithographically etched down to the
20 gate oxide layer 16 over the S/D regions 10, 12 to define the gate stacks 40. Spacers 28, which may be made of silicon oxide can be formed on the sides of the gate stacks 40. The S/D regions 10, 12 may be implanted following the formation of the gate stacks 40 to use the stacks 40 as implant masks.

[0018] Subsequent processing steps may open the gate oxide layer 16 at the
25 bottom of the S/D holes 26, provide an ohmic contact layer if necessary, and fill the S/D holes 26 with polysilicon or a metal to electrically contact the S/D regions 10, 12. The cap layer 24 can be removed to provide electrical contact to the top of the gate oxide layer 16 between the S/D regions 10, 12 forming the MOS gate.

[0019] The ruthenium layer 46 of various embodiments is formed directly on the
30 barrier layer 44. As used in this regard, the term "directly on" means that there is no interface layer between the ruthenium layer 46 and the barrier layer 44.

[0020] One or more embodiment of the disclosure is directed to a gate stack comprising a polysilicon layer 20 on a substrate 14. The polysilicon layer 20 can have an suitable thickness and can be formed by any suitable technique. The polysilicon layer 20 of some embodiments comprises an oxide-nitride-oxide (ONO) structure.

5 **[0021]** A silicide layer 42 is formed on the polysilicon layer 20. The silicide layer 42 of some embodiments comprises titanium silicide (TiSi). The thickness of the silicide layer 42 can be any suitable thickness. In some embodiments, the silicide layer 42 has a thickness in the range of about 10 Å to about 50 Å, or in the range of about 15 Å to about 40 Å, or in the range of about 20 Å to about 30 Å.

10 **[0022]** The silicide layer 42 can be formed by any suitable technique or process. For example, the silicide layer 42 can be formed by chemical vapor deposition (CVD), plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), plasma-enhanced atomic layer deposition (PEALD) or physical vapor deposition (PVD).

15 **[0023]** A barrier layer 44 is formed on the silicide layer 42. The barrier layer can be made from any suitable material and by any suitable technique. In some embodiments, the barrier layer comprises a nitride. In one or more embodiments, the nitride comprises one or more of TiN, TaN, WN or TiSiN.

[0024] The thickness of the barrier layer can be any suitable thickness. In some
20 embodiments, the barrier layer 44 has a thickness in the range of about 20 Å to about 200 Å, or in the range of about 30 Å to about 150 Å, or in the range of about 50 Å to about 100 Å.

[0025] The barrier layer 44 can be formed by any suitable technique or process. For example, the barrier layer 44 can be formed by chemical vapor deposition (CVD),
25 plasma-enhanced chemical vapor deposition (PECVD), atomic layer deposition (ALD), plasma-enhanced atomic layer deposition (PEALD) or physical vapor deposition (PVD).

[0026] A ruthenium layer 46 is formed on the barrier layer 44. The ruthenium layer 46 is formed by physical vapor deposition and may be referred to as a PVD Ru layer.
30 The ruthenium layer 46 can be formed directly on the barrier layer 44 without an

interface layer. As used in this regard, an "interface layer" is a separately and intentionally formed layer between the barrier layer 44 and the ruthenium layer 46. In some embodiments, the ruthenium layer 46 is formed on an optional interface layer (not shown).

- 5 **[0027]** The ruthenium layer 46 can be formed to any suitable thickness. In some embodiments, the ruthenium layer 46 has a thickness in the range of about 100 Å to about 300 Å, or in the range of about 100 Å to about 200 Å, or in the range of about 150 Å to about 300 Å, or in the range of about 200 Å to about 300 Å.

- 10 **[0028]** In some embodiments, forming the ruthenium layer 46 comprises providing a plasma sputter chamber including a target comprising ruthenium and a pedestal for supporting a substrate to be sputter deposited in opposition to the target. The pedestal of some embodiments comprises a high current electrostatic chuck maintained at a temperature greater than or equal to about 350 °C. In some
15 embodiments, the electrostatic chuck is maintained at a temperature in the range of about 450 °C to about 550 °C. In some embodiments, the high current electrostatic chuck comprises high resistivity ceramic.

- 20 **[0029]** The plasma processing gas (e.g., krypton gas) is flowed into the plasma sputter chamber and exited into a plasma. The plasma causes ruthenium atoms to be sputtered from the ruthenium target onto the substrate to deposit the ruthenium layer 46. In some embodiments, the plasma processing gas comprises substantially only krypton. As used in this regard, the term "substantially only" means that the active
25 plasma species is greater than or equal to about 90 atomic % Kr.

- 30 **[0030]** An example of a sputter chamber 50 useful for sputtering the ruthenium layer 46 is schematically illustrated in the cross-sectional view of FIG. 2. The sputter chamber 50 includes a vacuum chamber 52 arranged about a central axis 54 on which a ruthenium target 56 is supported through an isolator 58, which vacuum seals
35 the target 56 to the vacuum chamber 52 and electrically isolates the target 56 from the electrically grounded vacuum chamber 52. A vacuum pump system (not shown) pumps the interior of the vacuum chamber 52 to a pressure in the low milli Torr range.

5 [0031] The shape of the front surface of the ruthenium target 56 can be planar or generally concave with thicker outer peripheral edges than inner diameter portions. The ruthenium target 56 includes a layer of ruthenium facing the interior of the vacuum chamber 52 and which typically contains no more than 5 atomic % of elements other than ruthenium to provide a source of sputtered ruthenium.

[0032] A DC power source 60 negatively biases the target to about 600 to 1000 VDC with respect to the grounded vacuum chamber 52 or grounded sidewall shield (not shown) to excite a plasma processing gas into a plasma.

10 [0033] Conventionally, argon is the plasma processing gas and is supplied into the vacuum chamber 52 from an argon gas source through a mass flow controller. However, the inventors have found that argon atoms can become embedded in the deposited ruthenium layer 46 and that using a krypton gas source 62 as a plasma processing gas does not result in embedding of the krypton atoms. Therefore, the plasma processing gas of various embodiments comprises, consists essentially of, or
15 consists of krypton. In some embodiments, the plasma processing gas comprises substantially only krypton atoms. The krypton gas source 62 is connected to the vacuum chamber 52 through a mass flow controller 64.

[0034] The target power excites the plasma processing gas into a plasma and positively charged ions of the plasma are accelerated towards the target 54 and
20 sputter ruthenium atoms from it. The density of the plasma is increased by placing in back of the target 56 a magnetron 66 having an inner magnetic pole 68 of one magnetic polarity surrounded by an outer magnetic pole 70 of the opposed magnetic polarity. The poles 68, 70 project a magnetic field into the vacuum chamber 52 parallel to the face of the target 56 to trap electrons and hence increase the plasma
25 density and the resultant sputtering rate. To improve the sputtering uniformity and target utilization, the magnetic poles 68, 70 are asymmetric about the central axis 54 but supported on an arm 72 connected to a shaft 74 extending along the central axis 54. A motor 76 rotates the shaft 74 and hence the magnetron 66 about the central axis 54 to provide at least azimuthal uniformity.

30 [0035] A pedestal 80 within the vacuum chamber 52 supports a wafer 82 or other substrate in opposition to the target 56 to be coated with the ruthenium sputtered from

the target 56. A wafer is generally planar and circular except for alignment indicia. Optionally, an RF power source 84 biases the pedestal 80 through a capacitive coupling circuit 86. The pedestal 80 is conductive so that it acts as an electrode. The RF bias in the presence of a plasma within the vacuum chamber 52 causes a negative
5 DC self-bias to develop on the pedestal 80 so that sputtered ruthenium ions are accelerated towards the wafer 82 and their trajectories enter deep within any high aspect-ratio holes formed in the wafer 82.

[0036] After sputtering the ruthenium layer 46, an anneal chamber is provided to anneal the ruthenium layer 46. The anneal chamber can be any chamber suitable for
10 elevating the temperature of the substrate with the ruthenium layer 46 to a temperature greater than or equal to about 500 °C. Suitable annealing chambers include, but are not limited to, thermal processing chambers, rapid thermal annealing (RTA) chambers, spike annealing chambers and laser annealing chamber. In some embodiments, annealing the ruthenium layer occurs at a temperature of about 900 °C
15 for about 30 seconds in a N₂ environment. In some embodiments, annealing the ruthenium layer comprises heating the ruthenium layer to about 500 °C, increasing the temperature to about 900 °C at a rate greater than or equal to about 50 °C/sec, holding the temperature for about 30 seconds and cooling the temperature at a rate equal to or greater than about 70°C/sec.

[0037] After formation of the ruthenium layer 46, including annealing, a spacer layer 28 comprising a nitride is formed on the sides 46a of the ruthenium layer 46. The spacer layer 28 of some embodiments comprises SiN. In one or more
20 embodiments, formation of the spacer layer 28 results in the formation of substantially no ruthenium nitride on the sides of the ruthenium layer 46. As used in this manner, "substantially no ruthenium nitride" means that less than about 5% of the width of the
25 ruthenium layer 46 become ruthenium nitride. In some embodiments, less than about 2% of the width of the ruthenium layer 46 becomes ruthenium nitride.

[0038] An optional capping layer 24 can be formed on top of the ruthenium layer 46 before, during or after formation of the spacer layer 28. The capping layer 24 can be
30 made of the same material as the spacer layer 28, or can be a different material.

[0039] Examples

[0040] FIG. 3 shows a graph of the metal resistivity ($\mu\Omega\text{-cm}$) for as-deposited ruthenium, annealed ruthenium and as-deposited tungsten films as a function of film thickness. The post-annealed ruthenium resistivity was similar to the as-deposited tungsten resistivity. The ruthenium film was annealed at a temperature of about 900
5 °C for about 30 seconds in a nitrogen environment.

[0041] FIG. 4 shows a graph of the ruthenium resistivity ($\mu\Omega\text{-cm}$) for as-deposited ruthenium and annealed ruthenium films. The films were deposited with an electrostatic chuck temperature of about 450 °C and annealed at about 825 °C or 900 °C for about 30 seconds in a nitrogen environment.

10 **[0042]** Reference throughout this specification to "one embodiment," "certain embodiments," "one or more embodiments" or "an embodiment" means that a particular feature, structure, material, or characteristic described in connection with the embodiment is included in at least one embodiment of the invention. Thus, the appearances of the phrases such as "in one or more embodiments," "in certain
15 embodiments," "in one embodiment" or "in an embodiment" in various places throughout this specification are not necessarily referring to the same embodiment of the invention. Furthermore, the particular features, structures, materials, or characteristics may be combined in any suitable manner in one or more embodiments.

[0043] Although the invention herein has been described with reference to
20 particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It will be apparent to those skilled in the art that various modifications and variations can be made to the method and apparatus of the present invention without departing from the spirit and scope of the invention. Thus, it is intended that the present invention
25 include modifications and variations that are within the scope of the appended claims and their equivalents.

What is claimed is:

1. A method of forming a gate stack, the method comprising:
providing a plasma sputter chamber including a target comprising
5 ruthenium and a pedestal for supporting a substrate to be sputter deposited in
opposition to the target, the pedestal comprising a high current electrostatic
chuck at a temperature greater than or equal to about 350 °C;
flowing krypton into the chamber and exciting the krypton into a plasma
to deposit a ruthenium layer on the substrate;
10 providing an anneal chamber; and
annealing the ruthenium layer on the substrate at a temperature greater
than or equal to about 500 °C.
2. The method of claim 1, wherein the electrostatic chuck is at a temperature in
15 the range of about 450 °C to about 550 °C.
3. The method of claim 1, wherein the electrostatic chuck comprises high
resistivity ceramic.
- 20 4. The method of claim 1, wherein annealing the ruthenium layer occurs at a
temperature of about 900 °C for about 30 seconds in a N₂ environment.
5. The method of claim 1, wherein annealing the ruthenium layer comprises
heating the ruthenium layer to about 500 °C, increasing the temperature to
25 about 900 °C at a rate greater than or equal to about 50 °C/sec, holding the
temperature for about 30 seconds and cooling the temperature at a rate equal
to or greater than about 70°C/sec.
6. The method of claim 1, wherein the ruthenium layer is deposited directly on a
30 barrier layer without an interface layer.
7. The method of any of claims 1 to 6, wherein the barrier layer comprises one or
more of TiN, TaN, WN or TiSiN.

8. The method of claim 7, wherein the barrier layer is formed on a silicide layer.
9. The method of claim 8, wherein the silicide layer comprises TiSi with a
5 thickness of about 20 Å.
10. The method of claim 1, further comprising forming a spacer layer on sides of the ruthenium layer, the spacer layer comprising SiN, wherein forming the spacer layer forms substantially no ruthenium nitride.
- 10 11. A gate stack comprising:
a polysilicon layer on a substrate;
a silicide layer on the polysilicon layer;
a barrier layer on the silicide layer;
15 a ruthenium layer on the barrier layer; and
a spacer layer comprising a nitride on sides of the ruthenium layer,
wherein the ruthenium layer comprises substantially no ruthenium nitride
after formation of the spacer layer.
- 20 12. The gate stack of claim 11, wherein the silicide layer comprises titanium silicide with a thickness of about 20 Å.
13. The gate stack of claim 12, wherein the barrier layer comprises one or more of TiN, TaN, WN or TiSiN.
- 25 14. The method of claim 13, wherein the ruthenium layer is formed directly on the barrier layer without an interface layer.
15. The method of claim 13, further comprising an interface layer between the
30 ruthenium layer and the barrier layer.