CLAIMS

1. A resistive memory arrangement comprising:

a nanowire having a longitudinal axis; and

a resistive memory cell comprising:

a resistive layer comprising a resistive changing material, wherein at least a section of the resistive layer is arranged covering at least a portion of a surface of the nanowire, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

a conductive layer arranged on at least a part of the resistive layer.

2. The resistive memory arrangement as claimed in claim 1, ~~wherein the nanowire has a longitudinal axis, and~~ wherein the surface of the nanowire is arranged at least substantially parallel to a plane which intersects the longitudinal axis.

~~3. The resistive memory arrangement as claimed in claim 1, wherein the nanowire has a longitudinal axis, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire.~~

43. The resistive memory arrangement as claimed in claim ~~3~~1, wherein at least a portion of the conductive layer is arranged at least substantially surrounding the portion of the resistive layer.

~~5~~4. The resistive memory arrangement as claimed in claim ~~3~~1, wherein the portion of the resistive layer is arranged at least substantially surrounding a partial portion of the nanowire.

~~6~~5. The resistive memory arrangement as claimed in claim 1, wherein the nanowire is doped.

~~7~~6. The resistive memory arrangement as claimed in claim 1, wherein the nanowire comprises a semiconductor material.

~~8~~7. The resistive memory arrangement as claimed in claim 1, wherein the nanowire has a diameter of between about 10 nm and about 200 nm.

~~9~~8. The resistive memory arrangement as claimed in claim 1, wherein the nanowire has a length of between about 100 nm and about 2 μm.

~~10~~9. The resistive memory arrangement as claimed in claim 1, further comprising a substrate from which the nanowire extends monolithically.

~~11~~10. The resistive memory arrangement as claimed in claim 1, wherein the nanowire comprises a core portion and a peripheral portion at least substantially surrounding the core portion, wherein the core portion is doped with doping atoms of a first conductivity type, wherein the peripheral portion is doped with doping atoms of a second conductivity type, and wherein the second conductivity type is different from the first conductivity type.

~~12~~11. The resistive memory arrangement as claimed in claim 1, further comprising a second conductive layer in between the nanowire and the resistive layer, wherein at least a portion of the second conductive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire.

~~13~~12. The resistive memory arrangement as claimed in claim 1, further comprising a peripheral layer in between the nanowire and the resistive layer, wherein at least a portion of the peripheral layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire, wherein the nanowire is doped with doping atoms of a first conductivity type, wherein the peripheral layer is doped with doping atoms of a second conductivity type, and wherein the second conductivity type is different from the first conductivity type.

~~14~~13. The resistive memory arrangement as claimed in claim ~~13~~12, wherein the peripheral layer comprises a material selected from the group consisting of silicon, germanium, a III-V semiconductor and any alloy thereof.

~~15~~14. The resistive memory arrangement as claimed in claim ~~14~~13, wherein the alloy is selected from the group consisting of nickel silicide, titanium silicide, cobalt silicide, nickel-platinum silicide, nickel germanide and nickel-germanosilicide.

~~16~~15. The resistive memory arrangement as claimed in claim 1, further comprising:

a first peripheral layer in between the nanowire and the resistive layer, wherein at least a portion of the first peripheral layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

a second peripheral layer in between the first peripheral layer and the resistive layer, wherein at least a portion of the second peripheral layer is arranged around the longitudinal axis and at least substantially surrounding the portion of the first peripheral layer,

wherein the first peripheral layer is doped with doping atoms of a first conductivity type, wherein the second peripheral layer is doped with doping atoms of a second conductivity type, and wherein the second conductivity type is different from the first conductivity type.

~~17~~16. The resistive memory arrangement as claimed in claim 1, further comprising a transistor having a first source/drain terminal, a second source/drain terminal and a gate terminal, wherein the first source/drain terminal is electrically coupled to the resistive memory cell.

~~18~~17. The resistive memory arrangement as claimed in claim 1, comprising

a plurality of resistive memory cells spaced apart from each other along a length of the nanowire, each resistive memory cell comprising

a resistive layer comprising a resistive changing material, wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

a conductive layer arranged on at least a part of the resistive layer.

~~19~~18. A resistive memory arrangement comprising:

a plurality of nanowires, each nanowire of the plurality of nanowires having a longitudinal axis; and

a plurality of resistive memory cells, wherein each resistive memory cell of the plurality of resistive memory cells comprises

a resistive layer comprising a resistive changing material, wherein at least a section of the resistive layer is arranged covering at least a portion of a surface of a respective nanowire of the plurality of nanowires, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis of the respective nanowire and at least substantially surrounding the respective nanowire; and

a conductive layer arranged on at least a part of the resistive layer; and

a plurality of conductive lines electrically coupled to the plurality of nanowires and the plurality of resistive memory cells.

~~20~~19. A method of forming a resistive memory arrangement, the method comprising:

forming a nanowire, the nanowire having a longitudinal axis;

forming a resistive layer comprising a resistive changing material, wherein at least a section of the resistive layer is arranged covering at least a portion of a surface of the nanowire, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

forming a conductive layer on at least a part of the resistive layer.

CLAIMS

1. A resistive memory arrangement comprising:

a nanowire having a longitudinal axis; and

a resistive memory cell comprising:

a resistive layer comprising a resistive changing material, wherein at least a section of the resistive layer is arranged covering at least a portion of a surface of the nanowire, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

a conductive layer arranged on at least a part of the resistive layer.

2. The resistive memory arrangement as claimed in claim 1, wherein the surface of the nanowire is arranged at least substantially parallel to a plane which intersects the longitudinal axis.

3. The resistive memory arrangement as claimed in claim 1, wherein at least a portion of the conductive layer is arranged at least substantially surrounding the portion of the resistive layer.

4. The resistive memory arrangement as claimed in claim 1, wherein the portion of the resistive layer is arranged at least substantially surrounding a partial portion of the nanowire.

5. The resistive memory arrangement as claimed in claim 1, wherein the nanowire is doped.

6. The resistive memory arrangement as claimed in claim 1, wherein the nanowire comprises a semiconductor material.

7. The resistive memory arrangement as claimed in claim 1, wherein the nanowire has a diameter of between about 10 nm and about 200 nm.

8. The resistive memory arrangement as claimed in claim 1, wherein the nanowire has a length of between about 100 nm and about 2 μm.

9. The resistive memory arrangement as claimed in claim 1, further comprising a substrate from which the nanowire extends monolithically.

10. The resistive memory arrangement as claimed in claim 1, wherein the nanowire comprises a core portion and a peripheral portion at least substantially surrounding the core portion, wherein the core portion is doped with doping atoms of a first conductivity type, wherein the peripheral portion is doped with doping atoms of a second conductivity type, and wherein the second conductivity type is different from the first conductivity type.

11. The resistive memory arrangement as claimed in claim 1, further comprising a second conductive layer in between the nanowire and the resistive layer, wherein at least a portion of the second conductive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire.

12. The resistive memory arrangement as claimed in claim 1, further comprising a peripheral layer in between the nanowire and the resistive layer, wherein at least a portion of the peripheral layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire, wherein the nanowire is doped with doping atoms of a first conductivity type, wherein the peripheral layer is doped with doping atoms of a second conductivity type, and wherein the second conductivity type is different from the first conductivity type.

13. The resistive memory arrangement as claimed in claim 12, wherein the peripheral layer comprises a material selected from the group consisting of silicon, germanium, a III-V semiconductor and any alloy thereof.

14. The resistive memory arrangement as claimed in claim 13, wherein the alloy is selected from the group consisting of nickel silicide, titanium silicide, cobalt silicide, nickel-platinum silicide, nickel germanide and nickel-germanosilicide.

15. The resistive memory arrangement as claimed in claim 1, further comprising:

a first peripheral layer in between the nanowire and the resistive layer, wherein at least a portion of the first peripheral layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

a second peripheral layer in between the first peripheral layer and the resistive layer, wherein at least a portion of the second peripheral layer is arranged around the longitudinal axis and at least substantially surrounding the portion of the first peripheral layer,

wherein the first peripheral layer is doped with doping atoms of a first conductivity type, wherein the second peripheral layer is doped with doping atoms of a second conductivity type, and wherein the second conductivity type is different from the first conductivity type.

16. The resistive memory arrangement as claimed in claim 1, further comprising a transistor having a first source/drain terminal, a second source/drain terminal and a gate terminal, wherein the first source/drain terminal is electrically coupled to the resistive memory cell.

17. The resistive memory arrangement as claimed in claim 1, comprising

a plurality of resistive memory cells spaced apart from each other along a length of the nanowire, each resistive memory cell comprising

a resistive layer comprising a resistive changing material, wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

a conductive layer arranged on at least a part of the resistive layer.

18. A resistive memory arrangement comprising:

a plurality of nanowires, each nanowire of the plurality of nanowires having a longitudinal axis; and

a plurality of resistive memory cells, wherein each resistive memory cell of the plurality of resistive memory cells comprises

a resistive layer comprising a resistive changing material, wherein at least a section of the resistive layer is arranged covering at least a portion of a surface of a respective nanowire of the plurality of nanowires, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis of the respective nanowire and at least substantially surrounding the respective nanowire; and

a conductive layer arranged on at least a part of the resistive layer; and

a plurality of conductive lines electrically coupled to the plurality of nanowires and the plurality of resistive memory cells.

19. A method of forming a resistive memory arrangement, the method comprising:

forming a nanowire, the nanowire having a longitudinal axis;

forming a resistive layer comprising a resistive changing material, wherein at least a section of the resistive layer is arranged covering at least a portion of a surface of the nanowire, and wherein at least a portion of the resistive layer is arranged around the longitudinal axis and at least substantially surrounding the nanowire; and

forming a conductive layer on at least a part of the resistive layer.