

**MULTI-METAL LAYER ASSEMBLIES FOR WIREBOND
TAPE BALL GRID ARRAY PACKAGES**

Background

5 The disclosures herein relate generally to tape ball grid array (TBGA) circuits and more particularly to flexible circuits provided with a ground plane circuit that is electrically connected to the ground plane using insulation displacement vias (IDV's), solder filled vias, or other known connecting techniques.

10 Tape ball grid array (TBGA) packages offer impressive electrical and thermal performance, high reliability and proven compatibility with the wire bond die assembly and subsequent card assembly processes. One of the distinguishing features of some TBGA package constructions is the use of the carrier film as a solder mask by inverting the tape. The current costs for the TBGA wirebond carrier are significantly higher than the cost of the flexible circuit alone. Key cost drivers for this assembly include the stiffener material, flex circuit preparation, adhesive patterning, 15 and alignment/layup. A close examination of the value proposition of the TBGA wirebond carrier indicates that the market requirement currently satisfied by the wirebond carrier product may be better served with a novel, more cost-effective product construction.

20 To design an effective TBGA circuit, a ground plane is required to be closely spaced adjacent to the fine pitch traces on the TBGA tape. This ground plane provides electromagnetic damping as well as heat dissipation from the circuit. In the prior art, the stiffener was often a metallic component that was grounded to provide the required ground plane. In typical prior art devices, a polyimide tape was provided with fine pitch traces disposed thereon and attached with an adhesive to a rigid 25 metallic stiffener. The problem with prior art solutions was the cost. Patterned adhesive layers were required to provide accurate registration when laminating the flexible circuit to the stiffener. When possible and practical, it is desirable to avoid the patterning, lay-up and registration steps because they add significant expense to the manufacturing process.

30 IDV's are not as reliable as other connection methods such as solder bumps or solder filled vias. However, IDV's are substantially cheaper to produce than other types of connections. There are reliability issues with IDV interconnections which make it unsuitable for signal via connections. IDV connections are suitable for use

for power and ground circuit connections where redundant vias or connections are provided. If one IDV interconnect is bad or fails in use, it may not adversely affect the performance of the overall apparatus. With this being the case, IDV's can be used to connect a ground plane to a flexible circuit.

5 UK Patent 2,157,085 to Caton et al discloses a multi-metal layer circuit configuration including a first circuit layer having at least one first conductive layer thereon, a second circuit layer having at least one conductive trace thereon, the first and second traces each having an enlarged connection pad of a predetermined configuration at opposed locations, and ultrasonic weld means interconnecting the
10 first and second traces at the enlarged connection pads.

 In US Patent 5,379,512 to Ingle et al, a method for bonding the ends of the conductors to the circuit pad is disclosed hereby the cable is placed over the circuit pads. A bonding tool is then pressed against an upper surface of the cable with sufficient pressure to compress the substrate beyond its elastic limit. Ultrasonic
15 energy is applied to the bonding tool and transmitted through the substrate to affect a metallic bond between the conductors and the circuit pads.

 In US Patent 5,661,088, a method of packaging an electronic component includes forming a hole in a substrate having a first surface opposite a second surface. The method also includes disposing and patterning a malleable layer over the first
20 surface and over the hole in the substrate. The malleable layer has a third surface opposite a fourth surface. A portion of the fourth surface is exposed by the hole in the substrate. An electrically conductive layer is simultaneously disposed over a different portion of the third surface of the malleable layer. The malleable layer is deformed into the hole. Then, a semiconductor die is coupled to the malleable layer and an
25 underencapsulant is disposed under the semiconductor die and over the hole.

 U.S. Patent 5,519,936 and U.S. Patent 5,561,323 each disclose an electronic package which includes a rigid support member, e.g., copper sheet, to which is bonded both the package's semiconductor chip and circuitized substrate members. The chip is bonded using a thermally conductive adhesive while the circuitized
30 substrate, preferably a flexible circuit, is bonded using an electrically insulative adhesive. The chip is electrically coupled to designated parts of the circuitry of the substrate, preferably by wire, thermocompression or thermosonic bonding. An encapsulant may be used to cover and protect the connections between the chip and

substrate. This package may in turn be electrically coupled to a separate second substrate such as a PCB.

U.S. Patent 5,585,162 discloses a flexible circuit construction which allows solder balls to be mass reflow attached to the ground plane of a double-sided flexible circuit by providing a first via which is separate from the remainder of the ground plane, but which is electrically connected to the ground plane through a second via at a distance from the first via by a circuit trace on the side of the flexible circuit opposite the ground plane. In this device, metallized through holes or metallized blind vias interconnect layers on the TBGA.

None of the current product constructions or design techniques adequately address a cost-effective approach to making a circuit assembly with a reference plane. Accordingly, a need has arisen for a packaging substrate and method for manufacture in which the shortcomings of the previous techniques are overcome. More particularly, a need has arisen for a PCB construction in which a trace routing circuit and a ground plane circuit can be separately manufactured using processes optimized for the particular design and functional requirements of the circuit. The reference plane circuit does not have the fine pitch detail of the trace routing circuit. Therefore, it is expected that the reference plane circuit can be made using lower cost processes than can the trace routing circuit. The use of low-cost interconnect techniques such as insulation displacement vias is one such technique that will contribute to providing a cost-effective product construction.

Summary

One embodiment, accordingly, provides a multilayer circuit for attaching a semiconductor die to a substrate such as a printed circuit board in cost sensitive applications. To this end, a multi-layer circuit assembly includes a trace routing circuit having a first dielectric substrate. A first conductive layer is formed on a first side of the first dielectric substrate. A first adhesive layer is affixed to the trace routing circuit and a reference plane circuit is affixed to the first adhesive layer. The reference plane circuit includes a second dielectric substrate having at least one conductive reference plane formed on it. Each of the conductive reference planes are in electrical connection with the first conductive layer through the first adhesive layer.

A principal advantage of this embodiment is that the reference plane circuit can be manufactured, attached and electrically interconnected more cost effectively

than with previous reference plane construction techniques. The reference plane circuit and the trace routing circuit can be separately manufactured using the most cost effective techniques and subsequently joined together. A portion of the cost effectiveness comes from patterning the ground planes being integral to the manufacture of the reference plane circuit manufacture. Furthermore, unlike prior techniques, the ground plane circuit may be attached using a readily-available adhesive and electrically interconnected to the trace routing circuit using a low-cost interconnect method such as insulation displacement vias.

Brief Description of the Drawing Figures

Figure 1 is a cross-sectional view showing an illustrative embodiment of a trace routing circuit.

Figure 2 is a cross-sectional view showing an illustrative embodiment of a reference plane circuit.

Figure 3 is a cross-sectional view showing an illustrative embodiment of a circuit assembly having an adhesive layer formed between a trace routing circuit and a reference plane circuit.

Figure 4 is a cross-sectional view showing an illustrative embodiment of a circuit assembly having a two-metal layer trace routing circuit.

Figure 5A and 5B are cross-sectional views showing an illustrative embodiment of an insulation displacement via interconnect process.

Figure 6 is a cross-sectional view showing an electronic package according to the circuit assembly of Figure 3.

Figure 7 is a cross-sectional view showing an illustrative embodiment of a circuit assembly with solder plugs used for forming an interconnect between a trace routing circuit and a reference plane circuit.

Figure 8 is a cross-sectional view showing an illustrative embodiment of a circuit assembly having a reference plane circuit with a reference plane on both sides of the dielectric substrate.

Figure 9 is a cross-sectional view showing an illustrative embodiment of a circuit assembly excise process.

Detailed Description

In one embodiment, as shown in Figures 1 - 3, a trace routing circuit 2 includes a first dielectric substrate 4 having a first conductive layer 8 formed on a first side. A plurality of solder ball receiving passages 6 are formed through the first dielectric substrate 4. The first conductive layer 8 is patterned to include a plurality of traces 10 having a solder ball pad 12 formed adjacent to the solder ball receiving passage 6, forming a closed end 14. The reference plane circuit 16 includes a second dielectric substrate 18 having at least one reference plane 20 formed on a first side. To fabricate a circuit assembly 1 as shown in Figure 3, the trace routing circuit 2 and the reference plane circuit 16 are joined by forming a first adhesive layer 22 between them.

The trace routing circuit and reference plane circuit can be fabricated using one of many different processes that is well known in the art. A preferred process is disclosed in US Patent 5,227,008 to Klun et al. This patent discloses a process in which features are etched into or through the dielectric substrate and conductive materials are plated onto the dielectric substrate. Following is a brief overview discussing the major aspects of the circuit fabrication process disclosed in this patent.

A photoresist is formed on both sides of a dielectric substrate. If so required, the photoresist on the first side of the dielectric substrate is patterned using photolithography techniques to include features that will be plated onto the dielectric substrate. The photoresist on the opposing side of the dielectric substrate may also be patterned using photolithography techniques to include features that will be formed in the dielectric substrate by means such chemical etching. The plated features, if so included, are then plated. If features are to be formed in or through the dielectric substrate, the second side of the substrate is then etched or otherwise processed. The photoresist is stripped off and, if required, subsequent process steps such as cover plating may then be completed.

The reference plane circuit 16 has predominantly only gross features when compared to features of the trace routing circuit 2. Therefore, it is an advantage of the illustrative embodiments presented herein that the reference plane circuit 16 may be made separately from the trace routing circuit 2. It is contemplated that a variety of low-cost circuit fabrication techniques different that the process disclosed in US Patent No. 5,227,008 to Klun et al may be employed for fabricating the reference

plane circuit 16. These types of techniques may include screen printing a conductive material directly onto the dielectric substrate in a desired pattern; laminating die cut conductive foil patterns onto the dielectric substrate using an adhesive, and others techniques.

5 Figure 4 shows a circuit assembly 1 having a trace routing circuit 2 with a second conductive layer 21 formed on a second side of the first dielectric substrate 4. The second conductive layer 21 is patterned to include a plurality of traces 23. One or more conductive vias 25 interconnect at least a portion of the traces 23 of the second conductive layer 21 with traces 10 of the first conductive layer 8. Although a
10 conductive via 25 is shown, other interconnect techniques such as IDV's could also be used. The soldermask 27 may be formed over the second conductive layer with vias 6 formed therein. The solder mask 27 may be made of a photoimageable material such that the vias 6 may be formed using photolithography techniques.

 Figure 5A and 5B show a basic process for forming an IDV connection 28
15 between a trace 10 of the first conductive layer 8 and a reference plane 20. A bonding tool tip 24 applies pressure and/or heat on a solder ball pad 12. The first adhesive layer 22 is displaced from under the bonding tool tip 24 and the trace 12 is bonded to the reference plane 20.

 Referring now to Figure 6, a circuit assembly 1 is attached to a stiffening
20 member 32. One technique for attaching the stiffening member 32 to the circuit assembly 1 is with a second adhesive layer 30 that adheres the stiffening member 32 to the second dielectric substrate 18. Depending on the specific application, the second adhesive layer 30 could be attached to the circuit assembly 1 by the party who manufactures the circuit assembly 1. Alternately, the second adhesive layer 30 could
25 be integral with the stiffening member 32. A second party, at a later time, could then affix the stiffening member 32. In either case, this would simplify the attachment of the stiffening member 32 at a point in time different from when the circuit assembly 1 is made.

 In a preferred embodiment, the first and second dielectric substrates 4, 18
30 would be a polyimide film such as that sold by DuPont under the tradename KAPTON E. The first adhesive layer 22 would be a polyimide-based adhesive sold by DuPont under the tradename KJ. A preferred material for the second adhesive layer 30 would be a pressure sensitive adhesive such that sold by Minnesota Mining

and Manufacturing Co. under the tradename VHB. While the materials delineated above are preferred, it is contemplated that numerous other commercially-available materials suitable for the various dielectric substrates and adhesive layers will become known to those in the art.

5 In Figure 7, a solder plug 38 is formed in a solder plug via 40 for interconnecting the traces 10 of the first conductive layer 8 to the reference plane 20. The solder plug via 40 may be formed using one of many techniques well known in the art. For example, chemical etching, laser milling, plasma etching, mechanical
10 punching or other known processes could be used to form the solder plug via through the reference plane circuit. The first adhesive layer 22 may be attached to the circuit assembly prior to forming the vias to provide passages through it as well. By forming passages in the first adhesive layer 22 at the same time the solder plug vias 40 are formed, issues associated with aligning the first adhesive layer 22 to the trace routing circuit 2 and the reference plane circuit 16 are precluded.

15 Using commercially available and known laminating techniques, the trace routing circuit 2, first adhesive layer 22 and reference plane circuit 16 are held in alignment and laminated to form a circuit assembly 1 having a solder plug via 40 as shown in Figure 7. Following the lamination process, the solder plugs 38 may be formed by screening a solder paste into the vias and subjecting the circuit assembly to
20 a solder reflow operation. Alternately, one of many electro-less plating process known in the art could also be used to form the via 38.

 As shown in Figure 8, a circuit assembly 1 may be provided in a continuous fashion or panel fashion, whereby two or more circuit assemblies 1 need to be separated from each other using an excise process. An important advantage of the
25 illustrative embodiments presented herein is that they are configured to resist shorting between the reference plane 20 and the plating bus 58. In prior construction technique where the stiffening member is used as a reference plane, shorting sometimes results due to the excise process deforming and smearing the plating bus 58 such that it contacts the stiffening member. Excise processes and equipment are
30 well known in the art and will not be discussed herein in further detail.

 A plating bus 58 maintains electrical continuity between two adjacent circuit assemblies 1 to facilitate electro-plating in panel and roll-to-roll formats. By providing a suitable space between the reference plane 20 of two adjacent circuit

assemblies 1 at the location where an excise tool 58 severs the circuit assemblies 1 against a platen 59, the potential for shorting between the bus trace 58 and the reference plane 20 is greatly reduced, if not eliminated. The space between two adjacent reference planes 20 allows the first adhesive layer 22 to effectively insulate
5 each reference plane 20 from the severed plating bus 58.

Figure 9 shows a circuit assembly, indicated generally at 100, having a second reference plane 120' on the side of the second dielectric substrate 118 opposite first reference plane 120. In many electronic packaging applications, it will be desirable to use the first reference plane 120 for providing a first reference voltage and the second
10 reference plane 120' for providing a second reference voltage. Solder plugs 138, 138' may be used to interconnect the reference planes 120, 120' to respective traces 110. As shown, solder plugs 138, 138' are located adjacent to a solder ball pad 112. This is desirable since the area of the solder ball pad 112 is considerably larger than the other portions of the trace 110. The reference plane 120' may have recessed regions 141
15 such that solder plugs 138 for the first reference plane 120 may be formed from the same side as the solder plugs 138' for the second reference plane 120'. The recessed regions 141 prevent the solder plug 138 that is connected to the first reference plane 120 from contacting the second reference plane 120'.

In operation, the illustrative embodiments disclosed herein provide a circuit
20 assembly having a trace routing circuit attached to a separate reference plane circuit by a dielectric material such as an non-conductive adhesive. At least a portion of the conductive traces of the trace routing circuit are connected to a reference plane on the reference plane circuit. The traces route signals and power to and from a device mounted on the PCB. The reference planes are maintained at a desired voltage for
25 providing a reference voltage to the device or devices mounted on the PCB. Depending on the application, the voltage across the reference planes will typically be from 0.0 volts to 5.0 volts. In cases where two circuits having a plating bus therebetween are mechanically severed from each other, it is preferred that there is a gap between the reference planes at the location where the circuits are severed.

30 As a result, one embodiment provides a multi-layer circuit assembly having a trace routing circuit including a first dielectric substrate. At least one solder ball receiving passage is formed through the first dielectric substrate. A first conductive layer is formed on a first side of the first dielectric substrate. A first adhesive layer is

affixed to the trace routing circuit and a reference plane circuit is affixed to the first adhesive layer on a side opposite the trace routing circuit. The reference plane circuit includes a second dielectric substrate having at least one conductive reference plane formed thereon. Each of the at least one reference planes is in electrical connection
5 with the first conductive layer through the first adhesive layer.

Another embodiment provides an apparatus for packaging a semiconductor device having a trace routing circuit including a flexible first dielectric substrate. At least one solder ball receiving passage is formed through the flexible first dielectric substrate. A first conductive layer is formed on a first side of the flexible first
10 dielectric substrate. A first adhesive layer is affixed to the trace routing circuit and a flexible reference plane circuit is affixed to the first adhesive layer on a side opposite the trace routing circuit. The reference plane circuit includes a flexible second dielectric substrate having at least one conductive reference plane formed thereon. Each of the at least one reference planes is in electrical connection with the first
15 conductive layer through the first adhesive layer. A semiconductor device receiving passage is formed to extend through the trace routing circuit, the first adhesive layer and the reference plane circuit. A stiffening member is attached to the flexible second dielectric substrate.

Still another embodiment provides a multi-layer circuit assembly having a
20 trace routing circuit including a first dielectric substrate. The first dielectric substrate trace has at least one solder ball receiving passage formed therethrough and a first conductive layer formed on a first side. The first conductive layer is patterned to include a plurality of traces having a solder ball pad adjacent to a respective solder ball receiving passage, forming a closed end therewith. A first adhesive layer is
25 affixed to the first conductive layer and a reference plane circuit is affixed to the first adhesive layer. The reference plane circuit includes a second dielectric substrate having at least one reference plane formed thereon. Each of the at least one reference planes is in electrical connection with the first conductive layer through the first adhesive layer.

30 Yet another embodiment provides a multi-layer circuit assembly including a trace routing circuit having a first dielectric substrate. The first dielectric substrate has at least one solder ball receiving passage formed therethrough. A first conductive layer is formed on a first side of the first dielectric substrate and a second conductive

layer is formed on its second side. The first and second conductive layers are patterned to include a plurality of traces. The first side traces have a solder ball pad adjacent to a respective solder ball receiving passage for forming a closed end therewith. At least a portion of the first side traces are electrically connected to the
5 second side traces. A first adhesive layer is affixed to the first conductive layer and a reference plane circuit is affixed to the first adhesive layer. The reference plane circuit includes a second dielectric substrate having at least one reference plane formed thereon. Each of the reference planes is in electrical connection through the first adhesive layer with at least a portion of the first side traces.

10 As it can be seen, the principal advantages of these embodiments include the ability to separately manufacture the trace routing circuit and the reference plane circuit. This enables the processes selected for manufacturing each of the circuits to be better optimized. Another key advantage is that the process for manufacturing the reference plane circuit inherently provides the desired patterning of the reference
15 plane. For example, the reference plane may be patterned to be a split reference plane wherein two reference voltages may be provided by a single conductive layer. The reference plane circuit has predominantly only gross features when compared to those of the trace routing circuit. With this being the case, cost advantages will be achieved by employing low-cost fabrication techniques for making the reference plane circuit.

20 Although illustrative embodiments have been shown and described, a wide range of modification, change and substitution is contemplated in the foregoing disclosure and in some instances, some features of the embodiments may be employed without a corresponding use of other features. Accordingly, it is appropriate that the appended claims be construed broadly and in a manner consistent
25 with the scope of the embodiments disclosed herein.



What is claimed is:

1. A multi-layer circuit assembly, comprising:
a trace routing circuit including a first dielectric substrate having a first
conductive layer formed thereon;
5 a first adhesive layer affixed to the trace routing circuit; and
a reference plane circuit affixed to the first adhesive layer, the reference plane
circuit including a second dielectric substrate having at least one reference plane
formed thereon, each of the at least one reference planes being in electrical connection
through the first adhesive layer with the first conductive layer,
10 insulation displacement vias having been formed through the first adhesive layer for
electrically connecting the reference plane to the first conductive layer.
2. The multi-layer circuit assembly of claim 1 wherein the first dielectric
substrate is a flexible polymeric material, and the first conductive layer includes a
plurality of conductive traces having a solder ball pad and at least one solder ball
15 receiving passage formed through the first dielectric layer, the solder ball pad formed
adjacent to a respective solder ball receiving passage establishing a closed end
therewith.
3. The multi-layer circuit assembly of claim 4 further including a plating
bus extending to an edge of the circuit assembly, the reference plane having a portion
20 adjacent to the plating bus being offset from the respective edge of the circuit
assembly.
4. An apparatus for packaging a semiconductor device having a multi-
layer circuit assembly according to claim 1, comprising:
a trace routing circuit including a flexible first dielectric substrate having at
25 least one solder ball receiving passage formed therethrough and a first conductive
layer formed thereon, the first conductive layer including a plurality of conductive
traces having a solder ball pad adjacent to a respective solder ball receiving passage
for forming a closed end therewith;
a first adhesive layer affixed to the trace routing circuit;



- a reference plane circuit attached to the first adhesive layer, the reference plane circuit including a flexible second dielectric substrate having at least one reference plane formed thereon, each of the at least one reference planes being in electrical connection through the first adhesive layer with at least a portion of the traces;
- a semiconductor device receiving passage extending through the trace routing circuit, first adhesive layer and reference plane circuit; and
- a stiffening member attached to the second dielectric substrate on a side opposite the first adhesive layer.
- 5
- 10 5. A multi-layer circuit assembly, comprising:
- a trace routing circuit including a first dielectric substrate having at least one solder ball receiving passage formed therethrough and a first conductive layer formed on a first side, the first conductive layer being patterned to include a plurality of traces having a solder ball pad adjacent to a respective solder ball receiving passage for
- 15 forming a closed end therewith;
- a first adhesive layer affixed to the first conductive layer; and
- a reference plane circuit affixed to the first adhesive layer, the reference plane circuit including a second dielectric substrate having at least one reference plane formed thereon, each of the at least one reference planes being in electrical connection
- 20 through the first adhesive layer with at least a portion of the traces of the first conductive layer.