WHAT IS CLAIMED IS:

1. A semiconductor structure, comprising:

a semiconductor substrate having a first region and a second region;

a shallow trench isolation (STI) feature formed in the semiconductor substrate, wherein the STI feature includes a first portion disposed in the first region and having a first thickness T1 and a second portion disposed in the second region and having a second thickness T2 greater than the first thickness T1, the first portion of the STI feature being recessed from the second portion of the STI feature;

a plurality of fin active regions on the semiconductor substrate; and

a plurality of conductive features disposed on the fin active regions and the STI feature, wherein one of the conductive features covers the first portion of the STI feature in the first region.

2. The semiconductor structure of claim 1, wherein the first portion of the STI feature is recessed from the second portion of the STI feature such that a top surface of the first portion is lower than a top surface of the second portion by (T2-T1).

3. The semiconductor structure of claim 1, further comprising a plurality of dielectric features underlying the conductive features and separating the conductive feature from the fin active regions.

4. The semiconductor structure of claim 3, further comprising:

a capacitor disposed in the first region, wherein the capacitor includes one of the fin active regions, one of the conductive features, and one of the dielectric layer separating the one of the conductive features from the one of the fin active regions; and

a transistor disposed in the second region.

5. The semiconductor structure of claim 4, wherein the capacitor is a de-coupling capacitor and the transistor is a field effect transistor.

6. The semiconductor structure of claim 3, further comprising:

a first transistor disposed in the first region, wherein the first transistor includes a first gate stack having a first one of the dielectric features and a first one of the conductive features overlying the first one of the dielectric features; and

a second transistor disposed in the second region, wherein the second transistor includes a second gate stack having a second one of the dielectric features and a second one of the conductive features overlying the second one of the dielectric features,

wherein the first one of the dielectric features has a first dielectric thickness, and the second one of the dielectric features has a second dielectric thickness different from the first dielectric thickness.

7. The semiconductor structure of claim 3, wherein the plurality of conductive features include:

a first conductive feature disposed in the first region and having a first width W1; and

a second conductive feature disposed in the second region and having a second width W2 less than the first width W1.

8. The semiconductor structure of claim 7, wherein the plurality of dielectric features include:

a first dielectric feature disposed in the first region, underlying the first conductive feature, and having a first dielectric material; and

a second dielectric feature disposed in the second region, underlying the second conductive feature, and having a second dielectric material different from the first dielectric material.

9. The semiconductor structure of claim 8, wherein:

the first conductive feature, the first dielectric feature, and a first subset of the fin active regions are configured to form a capacitor; and

the second conductive feature, the second dielectric feature, and a second subset of the fin active regions are configured to form a fin field effect transistor (FinFET).

10. A semiconductor structure, comprising:

a semiconductor substrate having a first region and a second region;

a fin active region formed on the semiconductor substrate and extended in the first and second regions;

a shallow trench isolation (STI) feature formed in the semiconductor substrate and adjacent the fin active region, wherein the STI feature includes:

a first portion disposed in the first region and a second portion disposed in the second region, and

the first portion of the STI feature has a first top surface and the second portion of the STI feature has a second top surface higher than the first top surface;

a first conductive feature formed on the fin active region and the STI feature, wherein the first conductive feature is disposed in the first region and covers the first portion of the STI feature; and

a second conductive feature formed on the fin active region and the STI feature, wherein the second conductive feature is disposed in the second region.

11. The semiconductor structure of claim 10, further comprising:

a first dielectric feature aligned with the first conductive feature and underlying the first conductive feature; and

a second dielectric feature aligned with the second conductive feature and underlying the second conductive feature.

12. The semiconductor structure of claim 11, wherein:

the fin active region, the first dielectric feature, and the first conductive feature are configured and coupled to form a capacitor; and

the fin active region, the second dielectric feature, and the second conductive feature are configured and coupled to form a field effect transistor.

13. The semiconductor structure of claim 12, wherein:

the first conductive feature includes a first width; and

a second conductive feature includes a second width less than the first width.

14. The semiconductor structure of claim 12, wherein:

the first dielectric feature include a first thickness; and

the second dielectric feature include a second thickness different from the first thickness.

15. The semiconductor structure of claim 12, wherein

the first dielectric feature include a first dielectric material; and

the second dielectric feature include a second dielectric material different from the first dielectric material.

16. The semiconductor structure of claim 10, wherein:

the fin active region is oriented in a first direction; and

the first and second conductive features are oriented in a second direction perpendicular to the first direction.

17. A method, comprising:

etching a semiconductor substrate to form a plurality trenches and define a plurality of fin active regions;

filling in the plurality of trenches with a dielectric material to form shallow trench isolation (STI) features;

recessing a first subset of the STI features in a first region by a first dimension;

recessing a second subset of the STI features in a second region by a second dimension less than the first dimension; and

forming a conductive feature on the STI features and the fin active regions, wherein the conductive feature covers the first subset of the STI features.

18. The method of claim 17, wherein the recessing the first subset of the STI features in the first region by the first dimension; and the recessing the second subset of the STI features in the second region include:

forming a patterned resist layer on the semiconductor substrate, wherein the patterned resist layer has openings exposing the first region and covering the second region;

performing a first STI etch to the first subset of the STI features in the first region through openings of the patterned resist layer;

removing the patterned resist layer; and

performing a second STI etch to the first subset of the STI features in the first region and the second subset of the STI features in the second region, resulting in the first subset of the STI features being recessed from the second subset of the STI features.

19. The method of claim 18, further comprising performing a well implantation to the semiconductor substrate after the performing the first STI etch and before the performing the second STI etch.

20. The method of claim 19, further comprising:

depositing a hard mask layer on the semiconductor substrate;

patterning the hard mask layer using a lithography process, wherein the etching the semiconductor substrate to form the plurality trenches and define the plurality of fin active regions includes etching the semiconductor substrate through openings of the hard mask layer; and

removing the hard mask layer after the first STI etch and before the performing the well implantation.

CLAIMS

1. A semiconductor structure, comprising:

a semiconductor substrate having a first region and a second region;

a shallow trench isolation (STI) feature formed in the semiconductor substrate, wherein the STI feature includes a first portion disposed in the first region and having a first thickness T1 and a second portion disposed in the second region and having a second thickness T2 greater than the first thickness T1, the first portion of the STI feature being recessed from the second portion of the STI feature;

a plurality of fin active regions on the semiconductor substrate;

a plurality of conductive features disposed on the fin active regions and the STI feature, wherein one of the conductive features covers the first portion of the STI feature in the first region and a portion of the second portion of the STI feature in the second region;

a plurality of dielectric features underlying the conductive features and separating the conductive feature from the fin active regions;

a first transistor disposed in the first region, wherein the first transistor comprises a first gate stack having a first one of the dielectric features and a first one of the conductive features overlying the first one of the dielectric features; and

a second transistor disposed in the second region, wherein the second transistor comprises a second gate stack having a second one of the dielectric features and a second one of the conductive features overlying the second one of the dielectric features,

wherein the first one of the dielectric features has a first dielectric thickness, and the second one of the dielectric features has a second dielectric thickness different from the first dielectric thickness.

2. The semiconductor structure of claim 1, wherein the first portion of the STI feature is recessed from the second portion of the STI feature such that a top surface of the first portion is lower than a top surface of the second portion by (T2-T1).

3. The semiconductor structure of claim 1, further comprising: a capacitor disposed in the first region, wherein the capacitor includes one of the fin active regions, one of the conductive features, and one of the dielectric layer separating the one of the conductive

features from the one of the fin active regions; and a transistor disposed in the second region.

4. The semiconductor structure of claim 3, wherein the capacitor is a de-coupling capacitor and the transistor is a field effect transistor.

5. The semiconductor structure of claim 1, wherein the plurality of conductive features include:

a first conductive feature disposed in the first region and having a first width W1; and

a second conductive feature disposed in the second region and having a second width W2 less than the first width W1.

6. A semiconductor structure, comprising:

a semiconductor substrate having a first region and a second region;

a single fin active region formed on the semiconductor substrate that extends in the first and second regions;

a shallow trench isolation (STI) feature formed in the semiconductor substrate and adjacent the fin active region, wherein the STI feature includes:

a first portion disposed in the first region and a second portion disposed in the second region, and the first portion of the STI feature has a first top surface and the second portion of the STI feature has a second top surface higher than the first top surface;

a first conductive feature formed on the fin active region and the STI feature, wherein the first conductive feature is disposed in the first region and covers the first portion of the STI feature, the first conductive feature further comprising a first width;

a second conductive feature formed on the fin active region and the STI feature, wherein the second conductive feature is disposed in the second region, the second conductive feature further comprising a second width less than the first width;

a first dielectric feature aligned with the first conductive feature and underlying the first conductive feature, the first dielectric feature comprising a first thickness;

a second dielectric feature aligned with the second conductive feature and underlying the second conductive feature, the second dielectric feature comprising a second thickness different from the first thickness;

wherein the fin active region, the first dielectric feature, and the first conductive

feature are configured and coupled to form a capacitor; and

wherein the fin active region, the second dielectric feature, and the second conductive feature are configured and coupled to form a field effect transistor.

7. The semiconductor structure of claim 6, wherein: the fin active region is oriented in a first direction; and the first and second conductive features are oriented in a second direction perpendicular to the first direction.

8. The semiconductor structure of claim 1, wherein: each of the fin active regions extends along the first and second portions of the STI feature in a first direction; and each of the conductive features are disposed along the fin active regions and the STI features in a second direction perpendicular to the first direction.

9. The semiconductor structure of claim 1, wherein: the first portion of the first region has a plurality of sides; and the second portion of the second region surrounds the first portion on each of the sides.

10. The semiconductor structure of claim 9, wherein the conductive feature that covers the first and second portions of the STI feature extends out beyond all sides of the first portion to thereby cover the portion of the second portion of the STI feature in the second region.

11. A semiconductor structure, comprising:

a semiconductor substrate having a first region and a second region;

a shallow trench isolation (STI) feature formed in the semiconductor substrate, wherein the STI feature comprises a first portion disposed in the first region and having a first thickness T1 and a second portion disposed in the second region and having a second thickness T2 greater than the first thickness T1, the first portion of the STI feature being recessed from the second portion of the STI feature;

a plurality of fin active regions on the semiconductor substrate;

a plurality of conductive features disposed on the fin active regions and the STI feature, wherein one of the conductive features covers the first portion of the STI feature in the first region and a portion of the second portion of the STI feature in the second region;

wherein the plurality of conductive features further comprise:

a first conductive feature disposed in the first region and having a first width W1; and

a second conductive feature disposed in the second region and having a second width W2 less than the first width W1; and

a plurality of dielectric features underlying the conductive features and separating the conductive feature from the fin active regions, wherein the plurality of dielectric features comprise:

a first dielectric feature disposed in the first region, underlying the first conductive feature, and having a first dielectric material; and

a second dielectric feature disposed in the second region, underlying the second conductive feature, and having a second dielectric material different from the first dielectric material.

12. The semiconductor structure of claim 11, wherein:

the first conductive feature, the first dielectric feature, and a first subset of the fin active regions are configured to form a capacitor; and

the second conductive feature, the second dielectric feature, and a second subset of the fin active regions are configured to form a fin field effect transistor (FinFET).

13. A semiconductor structure, comprising:

a semiconductor substrate having a first region and a second region;

a single fin active region formed on the semiconductor substrate that extends in the first and second regions;

a shallow trench isolation (STI) feature formed in the semiconductor substrate and adjacent the fin active region, wherein the STI feature comprises: a first portion disposed in the first region and a second portion disposed in the second region, and the first portion of the STI feature has a first top surface and the second portion of the STI feature has a second top surface higher than the first top surface;

a first conductive feature formed on the fin active region and the STI feature, wherein the first conductive feature is disposed in the first region and covers the first portion of the STI feature, the first conductive feature further comprising a first width;

a second conductive feature formed on the fin active region and the STI feature, wherein the second conductive feature is disposed in the second region, the second

conductive feature further comprising a second width less than the first width;

a first dielectric feature aligned with the first conductive feature and underlying the first conductive feature, the first dielectric feature further comprising a first dielectric material;

a second dielectric feature aligned with the second conductive feature and underlying the second conductive feature, the second dielectric feature further comprising a second dielectric material different from the first dielectric material;

wherein the fin active region, the first dielectric feature, and the first conductive feature are configured and coupled to form a capacitor; and

wherein the fin active region, the second dielectric feature, and the second conductive feature are configured and coupled to form a field effect transistor.