CLAIMS

1. A memory, comprising:

a clock generation circuit, configured to generate a first oscillation signal and a second oscillation signal, wherein the first oscillation signal and the second oscillation signal have a same frequency but opposite phases, and a duty cycle of the first oscillation signal and a duty cycle of the second oscillation signal are both within a first preset range; and

a differential input circuit, configured to receive a first external signal and a second external signal, and generate a first internal signal and a second internal signal;

wherein the clock generation circuit is further configured to monitor at least one of a duty cycle of the first internal signal or a duty cycle of the second internal signal, and enable the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal to be within a second preset range.

2. The memory of claim 1, wherein the clock generation circuit comprises:

an oscillation circuit, configured to generate the first oscillation signal and the second oscillation signal;

a comparison unit, configured to receive the first oscillation signal and the second oscillation signal, and compare the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal; and

a logical unit, connected with the comparison unit and the oscillation circuit, the logical unit being configured to control the oscillation circuit according to an output result of the comparison unit, so that the duty cycle of the first oscillation signal and the duty cycle of the second oscillation signal are within the first preset range.

3. The memory of claim 2, wherein the comparison unit is further connected with an output terminal of the differential input circuit, and the comparison unit is configured to compare the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal; and

wherein the logical unit is further connected with the differential input circuit, and configured to control the differential input circuit according to the output result of the comparison unit, so that the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal is within the second preset range.

4. The memory of claim 3, wherein the comparison unit comprises:

an integral unit, having a first input terminal and a second input terminal, wherein the first input terminal is configured to receive one of the first internal signal and the second internal signal, and the second input terminal is configured to receive another one of the second internal signal and the first internal signal; or, the first input terminal is configured to receive one of the first oscillation signal and the second oscillation signal, and the second input terminal is configured to receive another one of the second oscillation signal and the first oscillation signal; and

a comparator, connected with an output terminal of the integral unit.

5. The memory of claim 4, wherein the integral unit is configured to:

in response to an inversion identification signal being at a low level, receive, through the first input terminal, the first internal signal, and in response to the inversion identification signal being at a high level, receive, through the first input terminal, the second internal signal; and

in response to the inversion identification signal being at the low level, receive, through the second input terminal, the second internal signal, and in response to the inversion identification signal being at the high level, receive, through the second input terminal, the first internal signal;

or,

in response to the inversion identification signal being at the low level, receive, through the first input terminal, the first oscillation signal, and in response to the inversion identification signal being at the high level, receive, through the first input terminal, the second oscillation signal; and

in response to the inversion identification signal being at the low level, receive, through the second input terminal, the second oscillation signal, and in response to the inversion identification signal being at the high level, receive, through the second input terminal, the first oscillation signal.

6. The memory of claim 5, wherein the logical unit comprises:

a counter, configured to adjust the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal, or, configured to adjust the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal;

a first register group, configured to store a first value of the counter according to an output of the comparator in response to the inversion identification signal being at the low level; and

a second register group, configured to store a second value of the counter according to an output of the comparator in response to the inversion identification signal being at the high level.

7. The memory of claim 6, wherein the logical unit further comprises:

an arithmetic component, connected with the first register group and the second register group, wherein the arithmetic component is configured to perform operations of addition, subtraction, multiplication and division on an output of the first register group and an output of the second register group; and

a third register group, connected with the arithmetic component, and configured to store an output result of the arithmetic component.

8. The memory of claim 7, wherein the comparison unit is driven by a sampling clock, a frequency of the sampling clock is lower than at least one of a frequency of the first internal signal or a frequency of the second internal signal, and the frequency of the sampling clock is lower than at least one of a frequency of the first oscillation signal or a frequency of the second oscillation signal.

9. The memory of claim 8, wherein the counter is driven by a calculator clock, a frequency of the calculator clock is lower than the at least one of the frequency of the first internal signal or the frequency of the second internal signal, and the frequency of the calculator clock is lower than the at least one of the frequency of the first oscillation signal or the frequency of the second oscillation signal.

10. The memory of claim 9, wherein the frequency of the sampling clock is the same as the frequency of the calculator clock.

11. The memory of claim 10, further comprising:

a frequency divider, configured to receive an external clock signal, and generate the sampling clock and the calculator clock.

12. The memory of claim 11, further comprising:

a fifth register group, connected with the frequency divider, wherein the fifth register group is configured to configure the frequency of the sampling clock and the frequency of the calculator clock.

13. The memory of any one of claims 2 to 12, wherein the oscillation circuit comprises:

an oscillator, configured to generate a first initial oscillation signal and a second initial oscillation signal, wherein the first initial oscillation signal and the second initial oscillation signal have a same frequency but opposite phases; and

a path analog circuit, arranged between the oscillator and the comparison unit, wherein one terminal of the path analog circuit is connected with an output terminal of the oscillator, another terminal of the path analog circuit is connected with an input terminal of the comparison unit, and the path analog circuit is configured to simulate circuit characteristics of a first path, receive the first initial oscillation signal to generate the first oscillation signal, and receive the second initial oscillation signal to generate the second oscillation signal.

14. The memory of claim 13, further comprising:

a fourth register group, connected with the oscillator, wherein the fourth register group is configured to configure the frequency of the first oscillation signal and the frequency of the second oscillation signal.

15. The memory of claim 14, further comprising:

a sixth register group, connected with the path analog circuit, wherein the sixth register group is configured to configure electrical parameters of the path analog circuit.

16. The memory of any one of claims 3 to 12, further comprising:

a first selector, wherein the first oscillation signal, the second oscillation signal, the first internal signal, the second internal signal, the first external signal and the second external signal are connected with the comparison unit through the first selector, and wherein the first oscillation signal and the second oscillation signal are taken as a first differential signal pair, the first external signal and the second external signal are taken as a second differential signal pair and the first internal signal and the second internal signal are taken as a third differential signal pair; and

wherein the first selector is configured to select one of the first differential signal pair, the second differential signal pair and the third differential signal pair to be input into the comparison unit.

17. The memory of claim 16, wherein the control terminal of the first selector is configured to receive a Select Enable Signal (SEL), and select one of the first differential signal pair, the second differential signal pair and the third differential signal pair based on the SEL to be input into the comparison unit.

18. The memory of any one of claims 1 to 12, further comprising:

a second selector, wherein the first oscillation signal, the second oscillation signal, the first external signal and the second external signal are connected with the differential input circuit through the second selector, and wherein the first oscillation signal and the second oscillation signal are taken as a first differential signal pair, and the first external signal and the second external signal are taken as a second differential signal pair; and

wherein the second selector is configured to select one of the first differential signal pair and the second differential signal pair to be input into the differential input circuit.

19. The memory of claim 18, wherein the control terminal of the second selector is configured to receive a calibration enable signal;

in response to the calibration enable signal being at a low level, the first external signal and the second external signal are input into the differential input circuit, and in response to the calibration enable signal being at a high level, the first oscillation signal and the second oscillation signal are input into the differential input circuit.

~~20. A memory, comprising:~~

~~a calibration circuit, configured to receive a first external signal and a second external signal, and generate a first internal signal and a second internal signal, wherein at least one of a duty cycle of the first internal signal and a duty cycle of the second internal signal are within a third preset range; and~~

~~a clock generation circuit, configured to generate a first oscillation signal and a second oscillation signal, wherein the first oscillation signal and the second oscillation signal have a same frequency but opposite phases;~~

~~wherein the calibration circuit is further configured to adjust at least one of a duty cycle of the first oscillation signal or a duty cycle of the second oscillation signal, and enable the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal to be within a fourth preset range.~~

21. The memory of claim 20, wherein the calibration circuit comprises:

a differential input circuit, configured to receive the first external signal and the second external signal, and generate the first internal signal and the second internal signal;

a comparison unit, connected with an output terminal of the differential input circuit, and the comparison unit is configured to compare the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal; and

a logical unit, connected with the comparison unit and the differential input circuit, wherein the logical unit is configured to control the differential input circuit according to an output result of the comparison unit, so that the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal is within the third preset range.

22. The memory of claim 21, wherein the comparison unit is further connected with an output terminal of the clock generation circuit, and the comparison unit is configured to receive the first oscillation signal and the second oscillation signal, and compare the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal; and

wherein the logical unit is further connected with the clock generation circuit, and configured to control the clock generation circuit according to the output result of the comparison unit, so that the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal is within the fourth preset range.

23. The memory of claim 22, wherein the comparison unit comprises:

an integral unit, having a first input terminal and a second input terminal, wherein the first input terminal is configured to receive one of the first internal signal and the second internal signal, and the second input terminal is configured to receive another one of the second internal signal and the first internal signal; or, the first input terminal is configured to receive one of the first oscillation signal and the second oscillation signal, and the second input terminal is configured to receive another one of the second oscillation signal and the first oscillation signal; and

a comparator, connected with an output terminal of the integral unit.

24. The memory according to claim 23, wherein the integral unit is configured to:

in response to an inversion identification signal being at a low level, receive, through the first input terminal, the first internal signal, and in response to the inversion identification

signal being at a high level, receive, through the first input terminal, the second internal signal; and

in response to the inversion identification signal being at the low level, receive, through the second input terminal, the second internal signal, and in response to the inversion identification signal being at the high level, receive, through the second input terminal, the first internal signal;

or,

in response to the inversion identification signal being at the low level, receive, through the first input terminal, the first oscillation signal, and in response to the inversion identification signal being at the high level, receive, through the first input terminal, the second oscillation signal; and

in response to the inversion identification signal being at the low level, receive, through the second input terminal, the second oscillation signal, and in response to the inversion identification signal being at the high level, receive, through the second input terminal, the first oscillation signal.

25. The memory of claim 24, wherein the logical unit comprises:

a counter, configured to adjust the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal, or, configured to adjust the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal;

a first register group, configured to store a first value of the counter according to an output of the comparator in response to the inversion identification signal being at the low level; and

a second register group, configured to store a second value of the counter according to an output of the comparator in response to the inversion identification signal being at the high level.

26. The memory of claim 25, wherein the logical unit further comprises:

an arithmetic component, connected with the first register group and the second register group, wherein the arithmetic component is configured to perform operations of addition, subtraction, multiplication and division on an output of the first register group and an output of the second register group; and

a third register group, connected with the arithmetic component, and configured to store an output result of the arithmetic component.

27. The memory of claim 26, wherein the comparison unit is driven by a sampling clock, a frequency of the sampling clock is lower than at least one of a frequency of the first internal signal or a frequency of the second internal signal, and the frequency of the sampling clock is further lower than at least one of a frequency of the first oscillation signal or a frequency of the second oscillation signal.

28. The memory of claim 27, wherein the counter is driven by a calculator clock, a frequency of the calculator clock is lower than the at least one of the frequency of the first internal signal or the frequency of the second internal signal, and the frequency of the calculator clock is lower than the at least one of the frequency of the first oscillation signal or the frequency of the second oscillation signal.

29. The memory of claim 28, wherein the frequency of the sampling clock is the same as the frequency of the calculator clock.

30. The memory of claim 29, further comprising:

a frequency divider, configured to receive an external clock signal, and generate the sampling clock and the calculator clock.

31. The memory of claim 30, further comprising:

a fifth register group, connected with the frequency divider, wherein the fifth register group is configured to configure the frequency of the sampling clock and the frequency of the calculator clock.

32. The memory of any one of claims 22 to 30, wherein the clock generation circuit comprises:

an oscillation circuit, configured to generate the first oscillation signal and the second oscillation signal, wherein an output terminal of the oscillation circuit is connected with the comparison unit.

33. The memory of claim 32, wherein the oscillation circuit comprises:

an oscillator, configured to generate a first initial oscillation signal and a second initial oscillation signal, wherein the first initial oscillation signal and the second initial oscillation signal have a same frequency but opposite phases; and

a path analog circuit, arranged between the oscillator and the comparison unit, wherein one terminal of the path analog circuit is connected with an output terminal of the oscillator,

another terminal of the path analog circuit is connected with an input terminal of the comparison unit, and the path analog circuit is configured to simulate circuit characteristics of a first path, receive the first initial oscillation signal to generate the first oscillation signal, and receive the second initial oscillation signal to generate the second oscillation signal.

34. The memory of claim 33, further comprising:

a fourth register group, connected with the oscillator, wherein the fourth register group is configured to configure the frequency of the first oscillation signal and the frequency of the second oscillation signal.

35. The memory of claim 34, further comprising:

a sixth register group, connected with the path analog circuit, wherein the sixth register group is configured to configure electrical parameters of the path analog circuit.

36. The memory of claim 35, further comprising:

a first selector, wherein the first oscillation signal, the second oscillation signal, the first internal signal, the second internal signal, the first external signal and the second external signal are connected with the comparison unit through the first selector, and wherein the first oscillation signal and the second oscillation signal are taken as a first differential signal pair, the first external signal and the second external signal are taken as a second differential signal pair and the first internal signal and the second internal signal are taken as a third differential signal pair; and

wherein the first selector is configured to select one of the first differential signal pair, the second differential signal pair and the third differential signal pair to be input into the comparison unit.

37. The memory of claim 36, wherein the control terminal of the first selector is configured to receive a Select Enable Signal (SEL), and select one of the first differential signal pair, the second differential signal pair and the third differential signal pair based on the SEL to be input into the comparison unit.

38. The memory of any one of claims 21 to 30, further comprising:

a second selector, wherein the first oscillation signal, the second oscillation signal, the first external signal and the second external signal are connected with the differential input circuit through the second selector, and wherein the first oscillation signal and the second

~~oscillation signal are taken as a first differential signal pair, and the first external signal and the second external signal are taken as a second differential signal pair; and~~

~~wherein the second selector is configured to select one of the first differential signal pair and the second differential signal pair to be input into the differential input circuit.~~

~~39. The memory of claim 38, wherein the control terminal of the second selector is configured to a calibration enable signal;~~

~~in response to the calibration enable signal being at a low level, the first external signal and the second external signal are input into the differential input circuit, and in response to the calibration enable signal being at a high level, the first oscillation signal and the second oscillation signal are input into the differential input circuit.~~

~~40. A memory, comprising:~~

~~a clock generation circuit, configured to generate a first oscillation signal and a second oscillation signal, wherein the first oscillation signal and the second oscillation signal have a same frequency but opposite phases, and a duty cycle of the first oscillation signal and a duty cycle of the second oscillation signal are both within a fifth preset range; and~~

~~a first external signal and a second external signal, coming from an outside of the memory, wherein a duty cycle of the first external signal and a duty cycle of the second external signal are both within a sixth preset range;~~

~~a differential input circuit, configured to receive the first oscillation signal and the second oscillation signal, and output a first internal signal and a second internal signal in a test mode; and the differential input circuit is further configured to receive the first external signal and the second external signal, and output the first internal signal and the second internal signal in a normal operating mode;~~

~~wherein the differential input circuit has data interaction with the clock generation circuit, so that at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal is within a seventh preset range in the test mode or in the normal operating mode.~~

~~41. The memory of claim 40, wherein the clock generation circuit comprises:~~

~~an oscillation circuit, configured to generate the first oscillation signal and the second oscillation signal;~~

a comparison unit, configured to receive the first oscillation signal and the second oscillation signal, and compare the at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal; and

a logical unit, connected with the comparison unit and the oscillation circuit, the logical unit being configured to control the oscillation circuit according to an output result of the comparison unit, so that at least one of the duty cycle of the first oscillation signal or the duty cycle of the second oscillation signal is within the fifth preset range.

42. The memory of claim 41, wherein the data interaction comprises:

in the test mode or in the normal operating mode, the comparison unit being configured to receive the first internal signal and the second internal signal, and compare the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal; and

wherein the logical unit is further connected with the differential input circuit, and configured to control the differential input circuit according to the output result of the comparison unit, so that the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal is within the seventh preset range.

43. The memory of claim 42, wherein the comparison unit comprises:

an integral unit, having a first input terminal and a second input terminal, wherein in the test mode, the first input terminal is configured to receive one of the first oscillation signal and the second oscillation signal, and the second input terminal is configured to receive another one of the second oscillation signal and the first oscillation signal; or, the first input terminal is configured to receive one of the first internal signal and the second internal signal, and the second input terminal is configured to receive another one of the second internal signal and the first internal signal; in the normal operating mode, the first input terminal is configured to receive one of the first internal signal and the second internal signal, and the second input terminal is configured to receive another one of the second internal signal and the first internal signal; and

a comparator, connected with an output terminal of the integral unit.

44. The memory according to claim 43, wherein the integral unit is configured to:

in the test mode or in the normal operating mode, in response to an inversion identification signal being at a low level, receive, through the first input terminal of the

integral unit, the first internal signal, and in response to the inversion identification signal being at a high level, receive, through the first input terminal of the integral unit, the second internal signal; and

in the test mode or in the normal operating mode, in response to the inversion identification signal being at the low level, receive, through the second input terminal of the integral unit, the second internal signal, and in response to the inversion identification signal being at the high level, receive, through the second input terminal of the integral unit, the first internal signal.

45. The memory of claim 44, wherein the integral unit is configured to:

in the test mode, in response to the inversion identification signal being at the low level, receive, through the first input terminal of the integral unit, the first oscillation signal, and in response to the inversion identification signal being at the high level, receive, through the first input terminal, the second oscillation signal; and

in the test mode, in response to the inversion identification signal being at the low level, receive, through the second input terminal of the integral unit, the second oscillation signal, and in response to the inversion identification signal being at the high level, receive, through the second input terminal, the first oscillation signal.

46. The memory of claim 45, wherein the logical unit comprises:

a counter, configured to adjust the at least one of the duty cycle of the first internal signal or the duty cycle of the second internal signal;

a first register group, configured to store a first value of the counter according to an output of the comparator in response to the inversion identification signal being at the low level; and

a second register group, configured to store a second value of the counter according to an output of the comparator in response to the inversion identification signal being at the high level.

47. The memory of claim 46, wherein the logical unit further comprises:

an arithmetic component, connected with the first register group and the second register group, wherein the arithmetic component is configured to perform operations of addition, subtraction, multiplication and division on an output of the first register group and an output of the second register group; and

a third register group, connected with the arithmetic component, wherein the third register group is configured to store an output result of the arithmetic component.

48. The memory of claim 41, further comprising:

a first selector, wherein the first oscillation signal, the second oscillation signal, the first internal signal, the second internal signal, the first external signal and the second external signal are connected with the comparison unit through the first selector, and wherein the first oscillation signal and the second oscillation signal are taken as a first differential signal pair, the first external signal and the second external signal are taken as a second differential signal pair and the first internal signal and the second internal signal are taken as a third differential signal pair; and

wherein the first selector is configured to select one of the first differential signal pair, the second differential signal pair and the third differential signal pair to be input into the comparison unit.

49. The memory of claim 48, wherein

in the test mode, the first selector is configured to select the first differential signal pair or the third differential signal pair to be input into the comparison unit; and

in the normal operating mode, the first selector is configured to select the second differential signal pair or the third differential signal pair to be input into the comparison unit.

50. The memory of claim 41, further comprising:

a second selector, wherein the first oscillation signal, the second oscillation signal, the first external signal and the second external signal are connected with the differential input circuit through the second selector, and wherein the first oscillation signal and the second oscillation signal are taken as a first differential signal pair, and the first external signal and the second external signal are taken as a second differential signal pair; and

wherein the second selector is configured to select one of the first differential signal pair and the second differential signal pair to be input into the differential input circuit.

51. The memory of claim 50, wherein

in the test mode, the second selector is configured to select the first differential signal pair to be input into the differential input circuit; and

in the normal operating mode, the second selector is configured to select the second differential signal pair to be input into the differential input circuit.