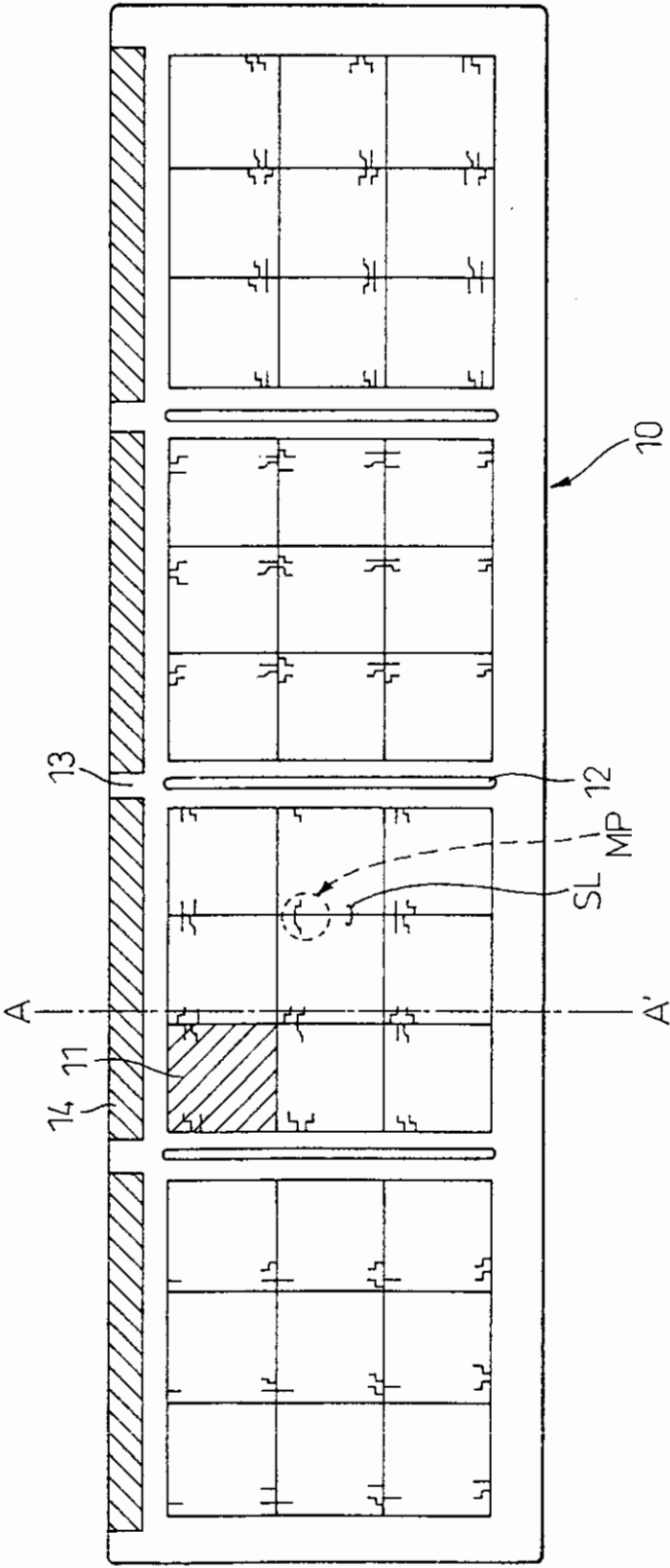


Fig.1



$\frac{2}{21}$ 

Fig.2(a)

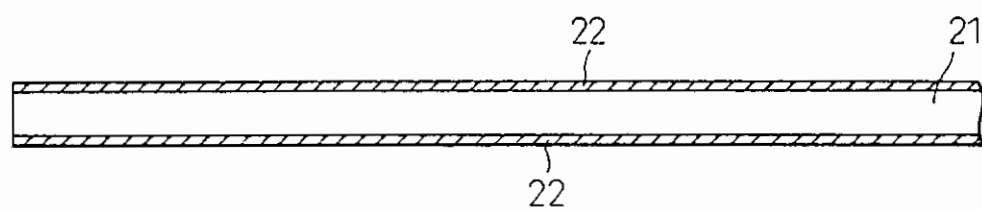


Fig.2(b)

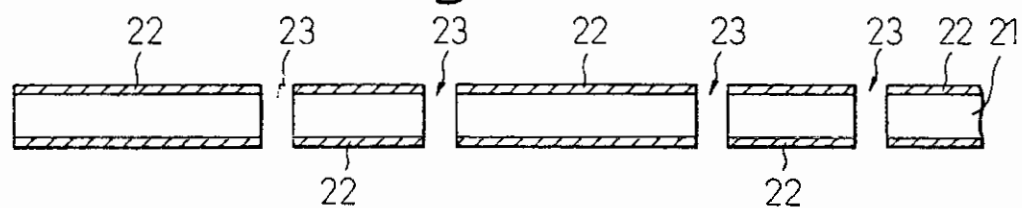


Fig.2(c)

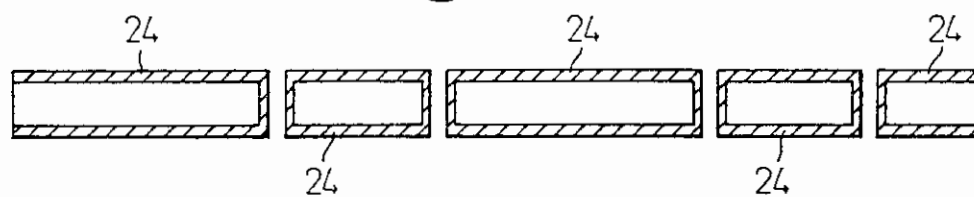


Fig.2(d)

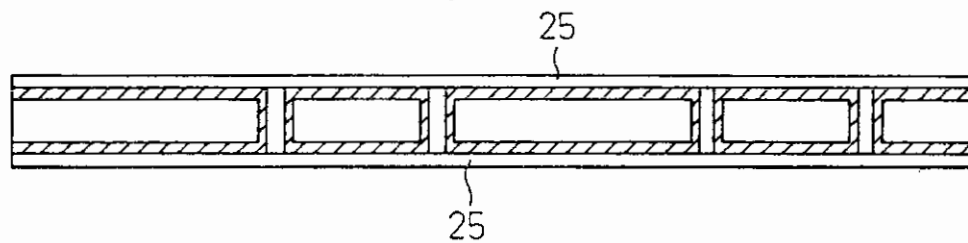


Fig.3(a)

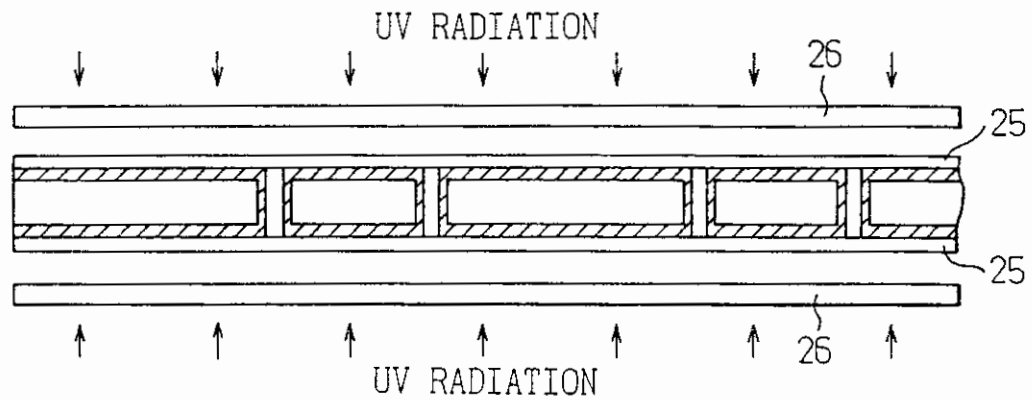


Fig.3(b)

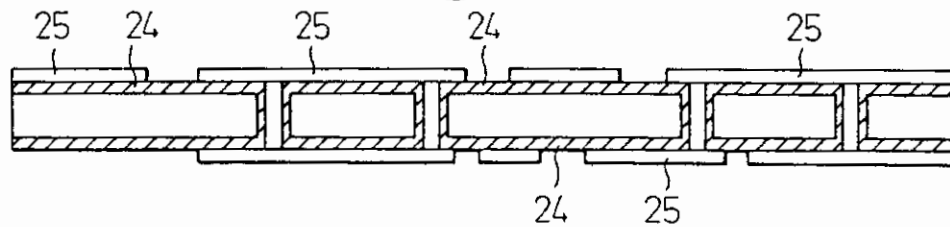


Fig.3(c)

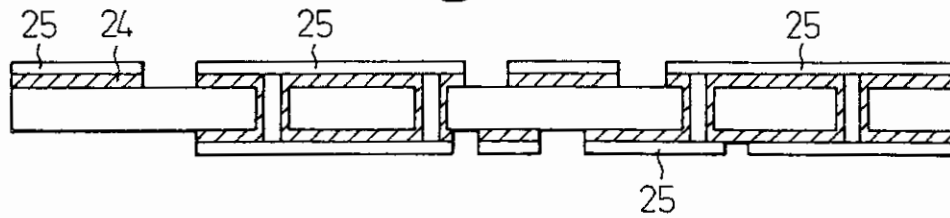
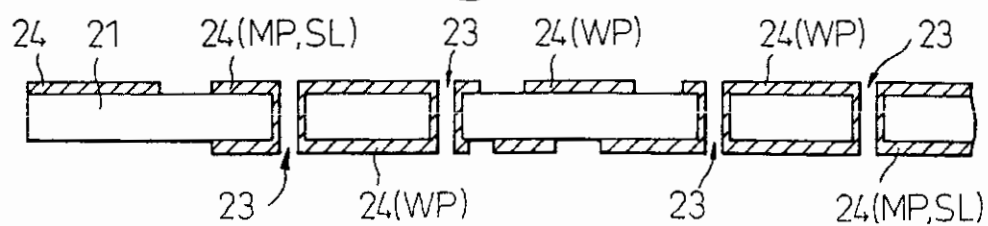


Fig.3(d)



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Fig.4(a)

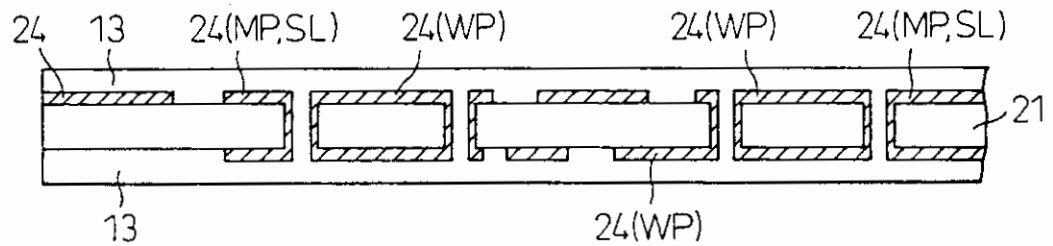


Fig.4(b)

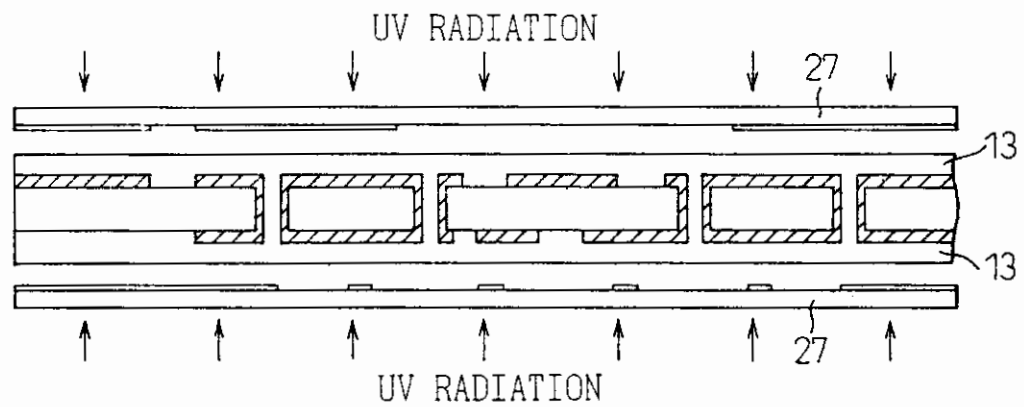


Fig.4(c)

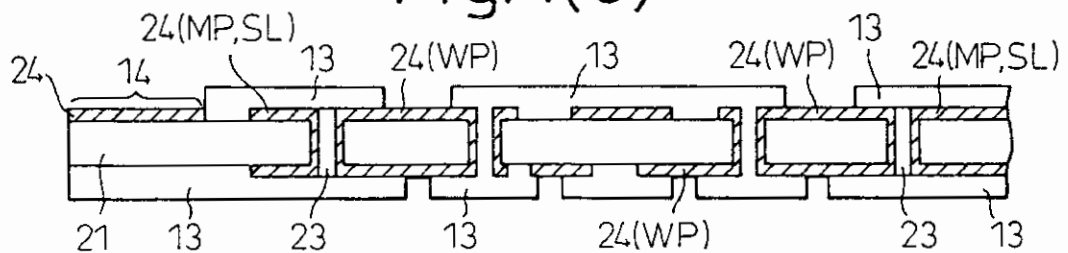
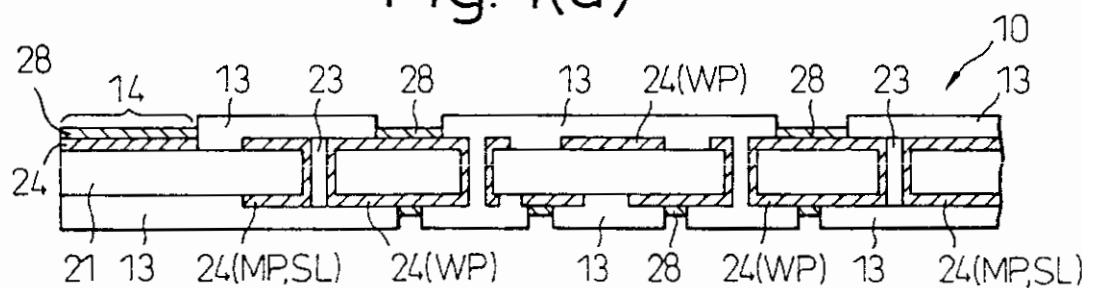


Fig.4(d)



[illegible]

Figure 1 is a cross-sectional view of a semiconductor device 10. The device includes a substrate 13 with a top layer 14. A series of rectangular blocks 31 are mounted on the substrate, connected by a conductive layer 32. A top layer 33 is shown above the blocks.

Fig.6(a)

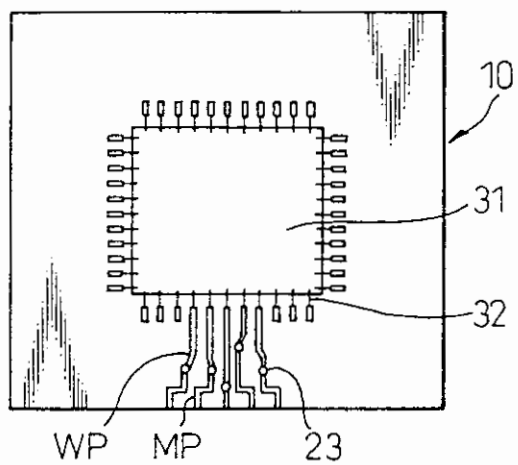


Fig.6(b)

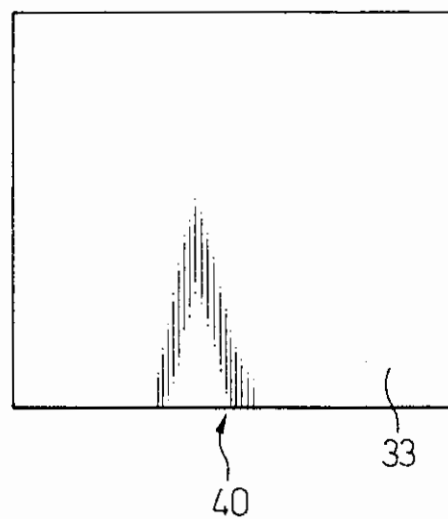


Fig.6(c)

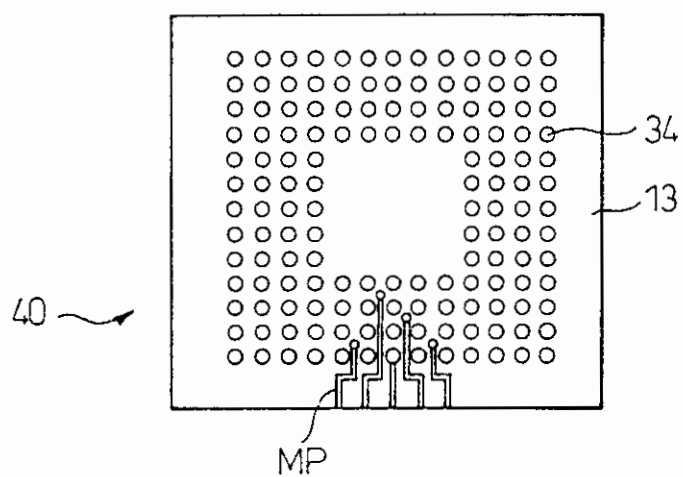


Fig.7(a)

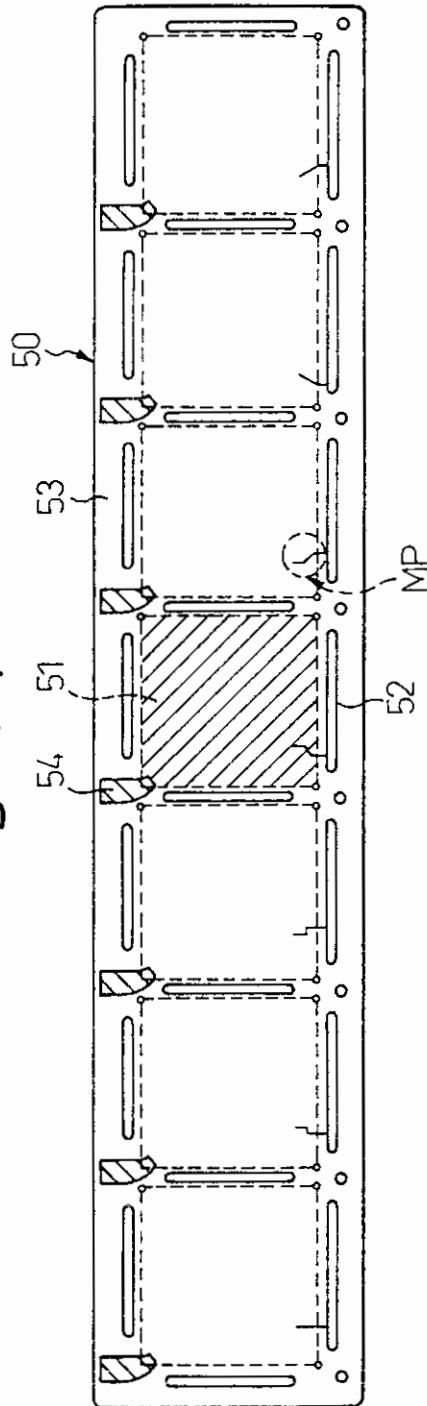


Fig.7(b)

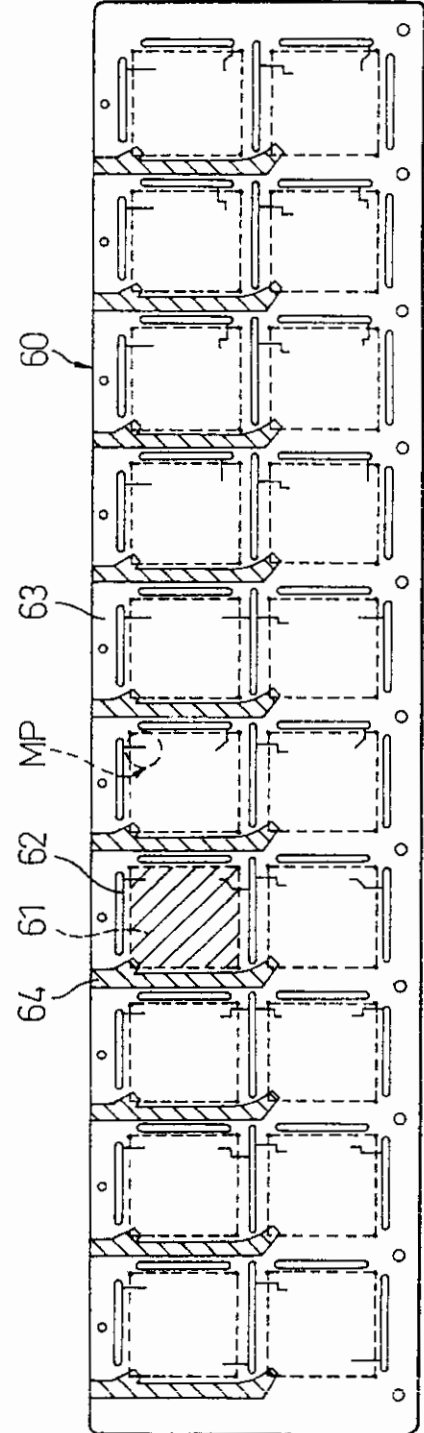


Fig.8

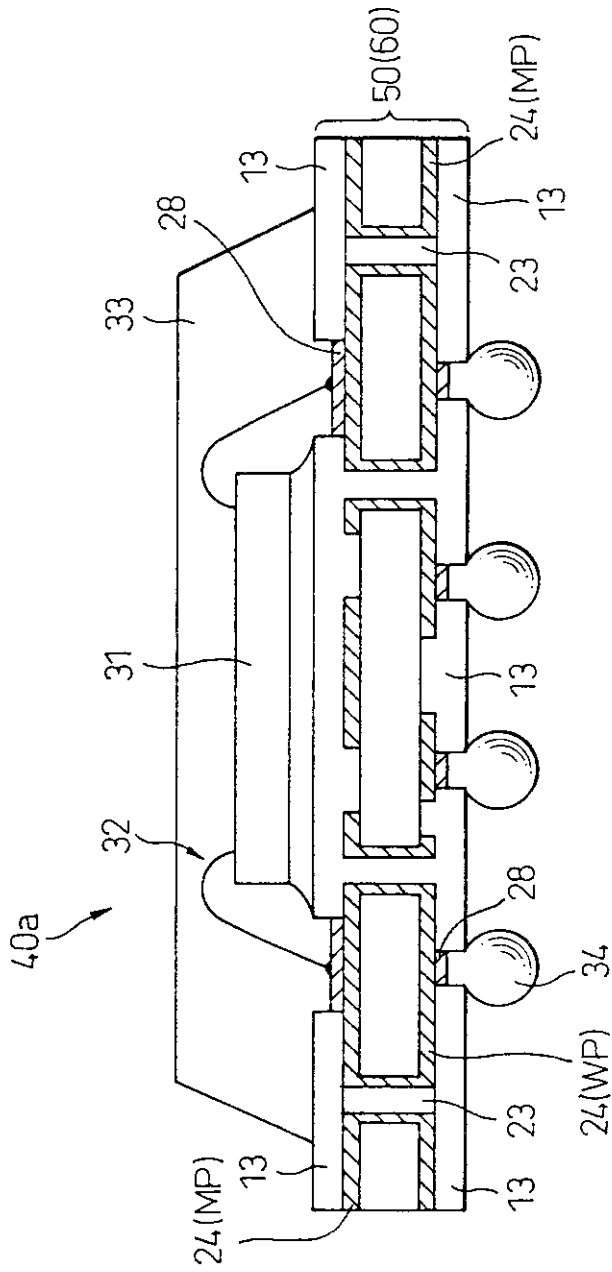


Fig.9(a)

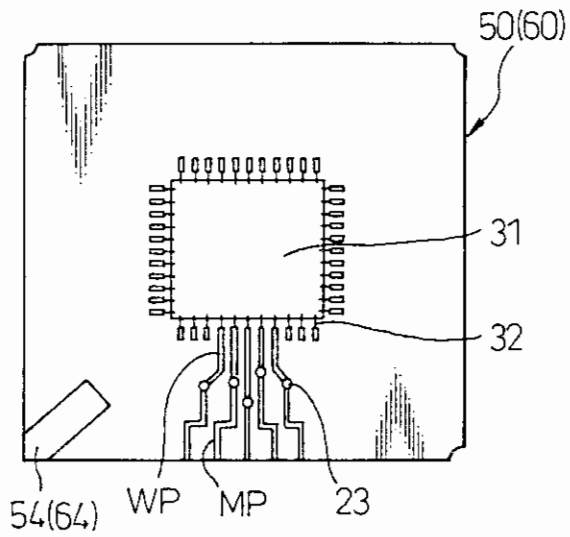


Fig.9(b)

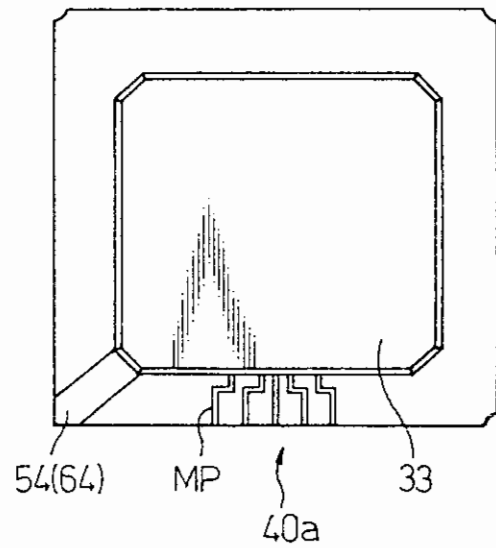


Fig.9(c)

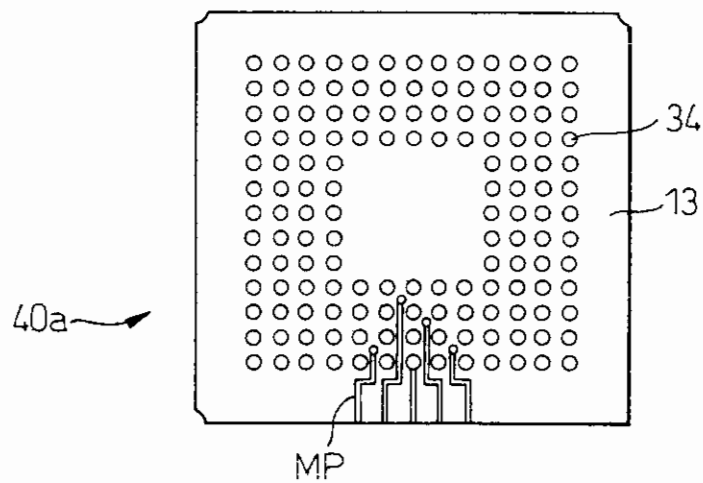


Fig.10(a)

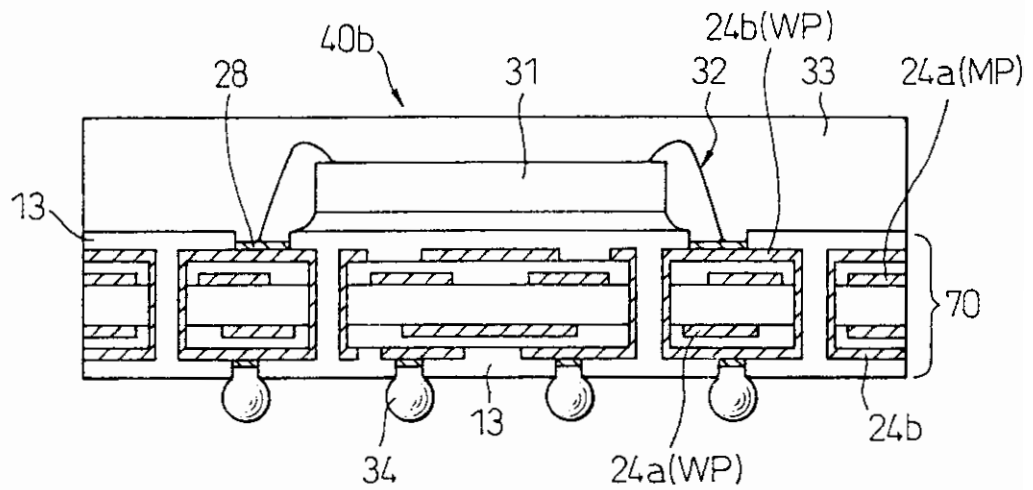


Fig.10(b)

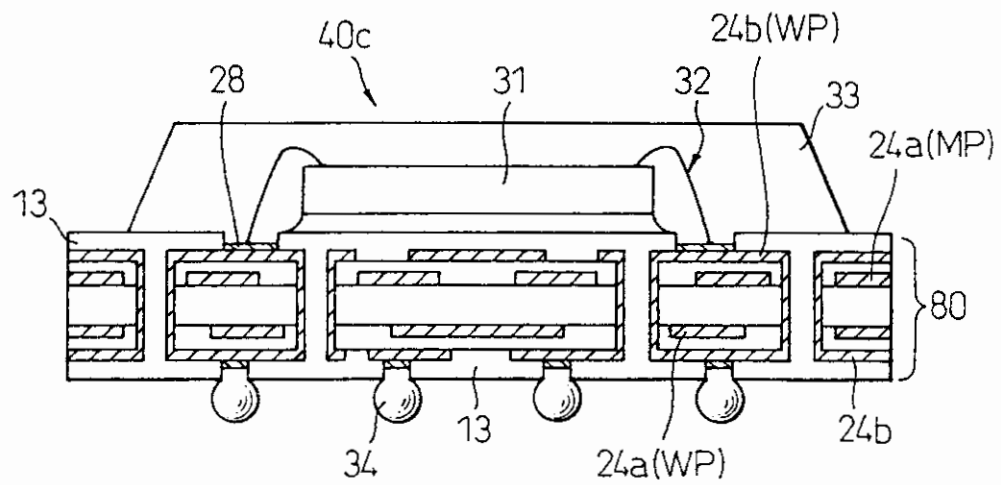


Fig.11

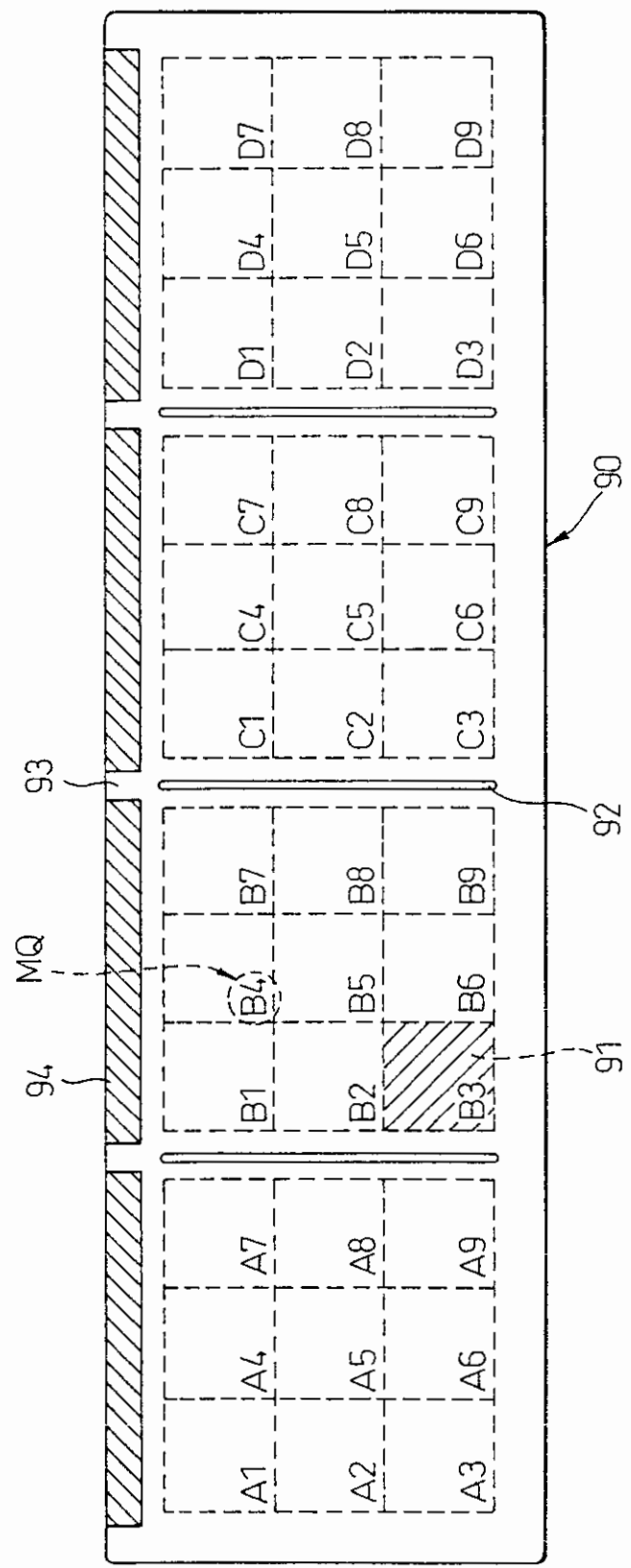


Fig.12

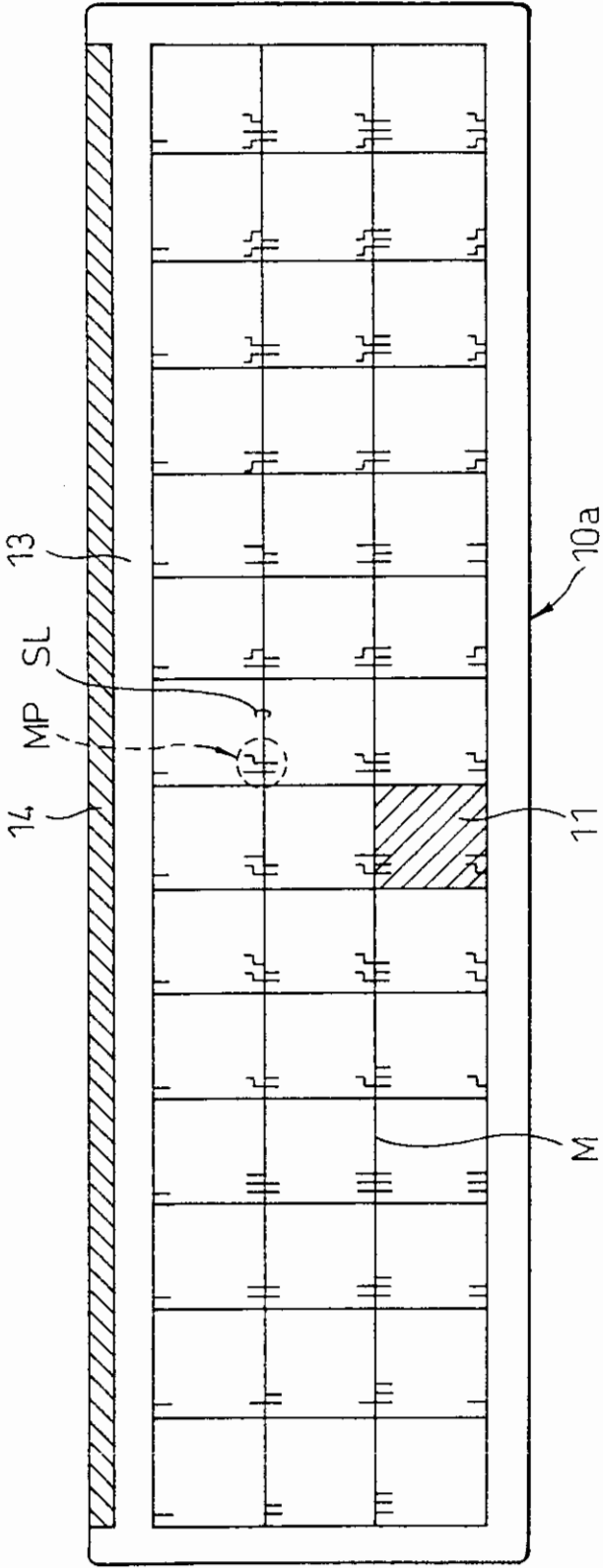


Fig.13(a)

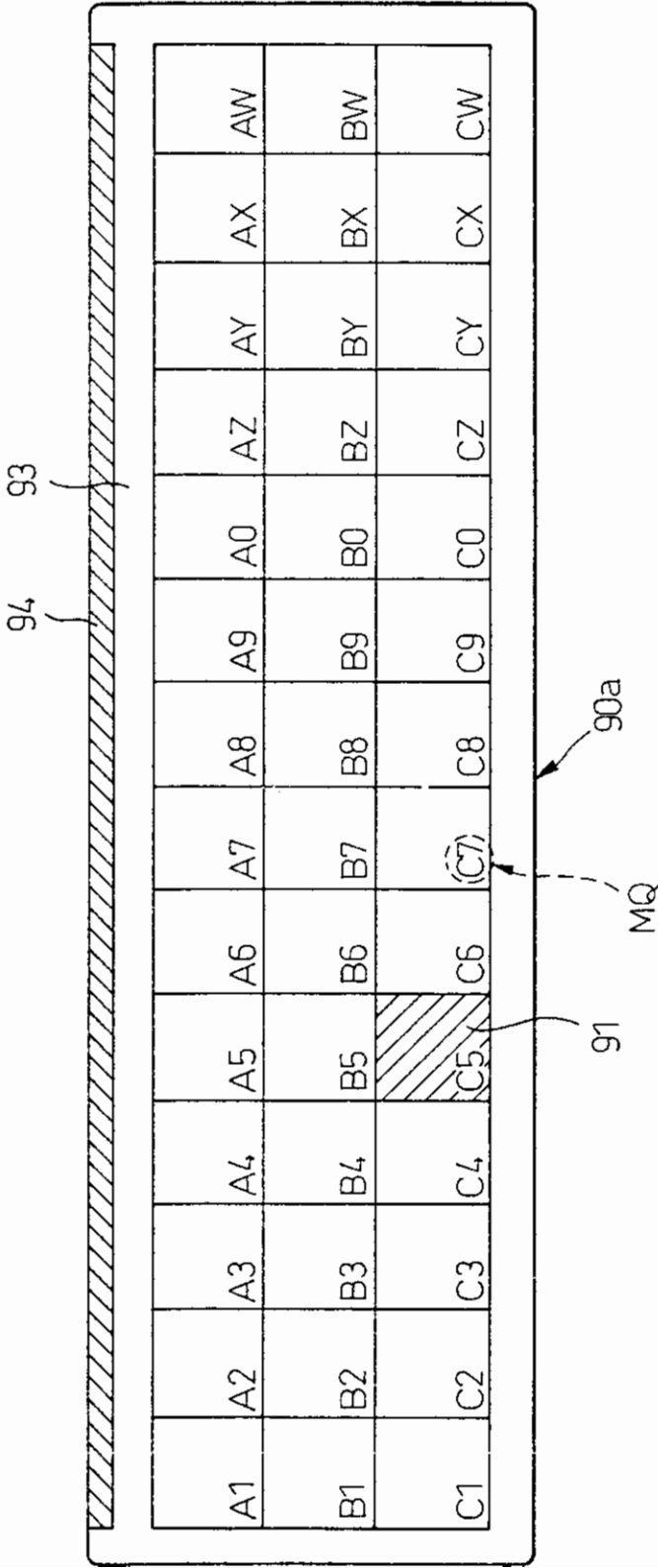


Fig.13(b)

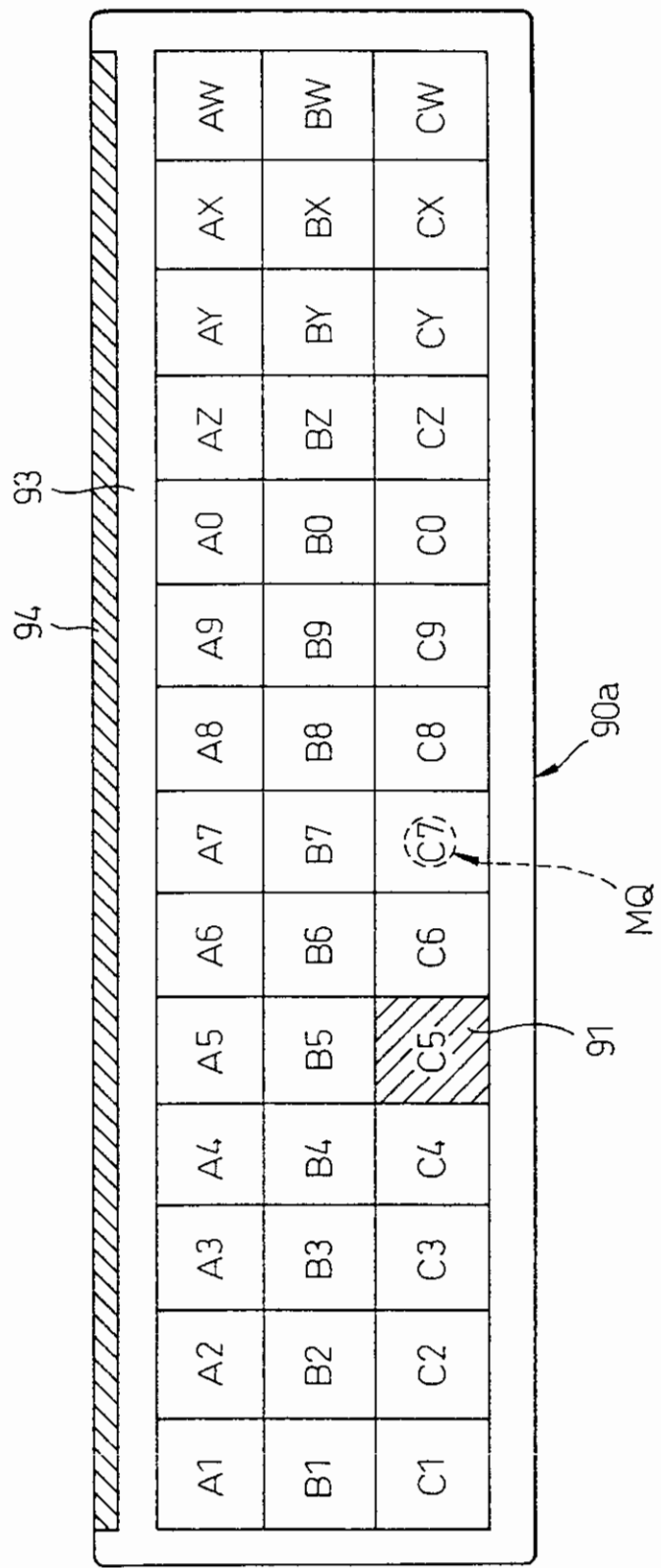


Fig.14(a)

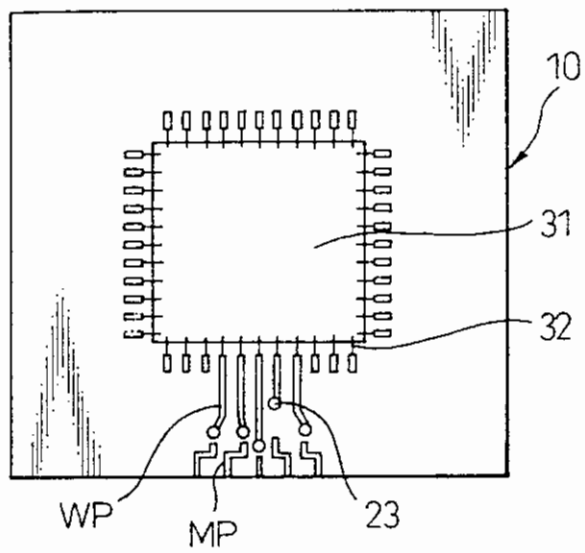


Fig.14(b)

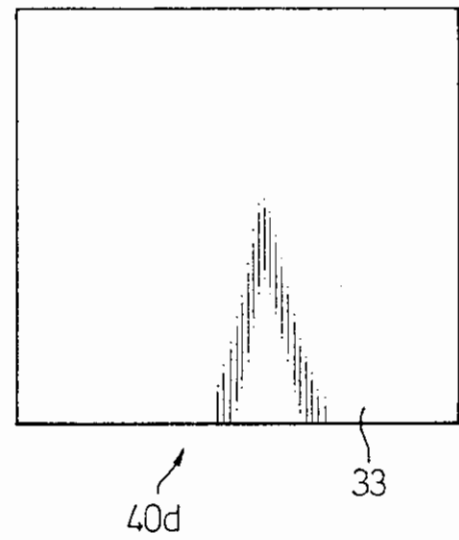


Fig.14(c)

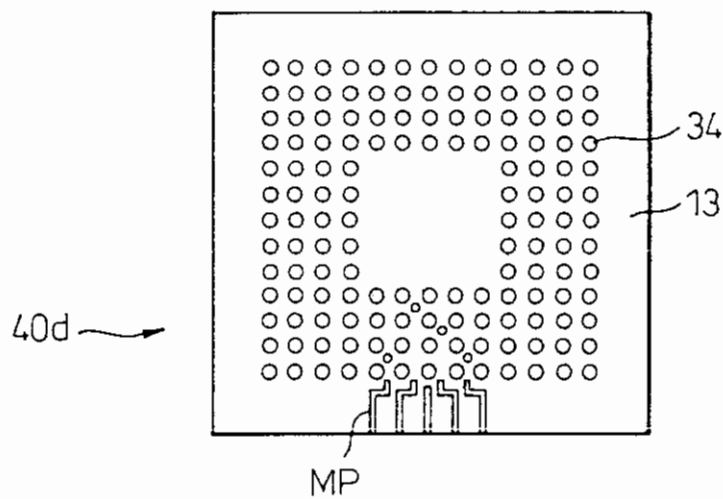


Fig.15(a)

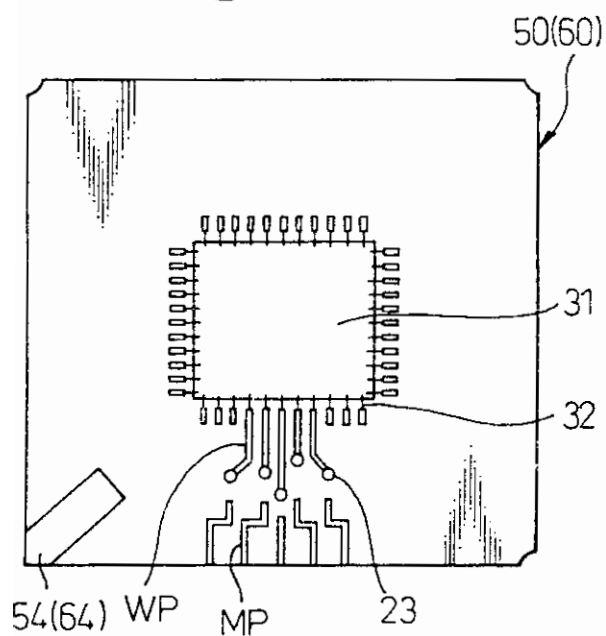


Fig.15(b)

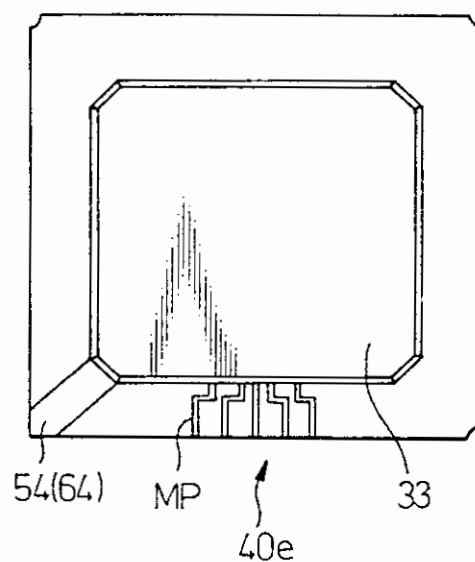


Fig.15(c)

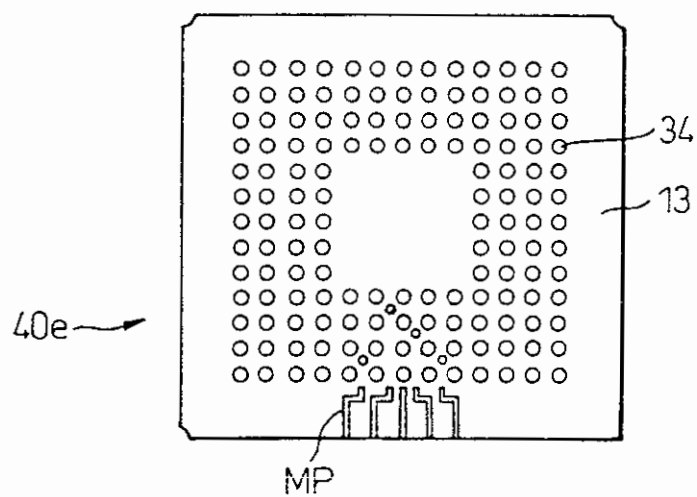


Fig.16(a)

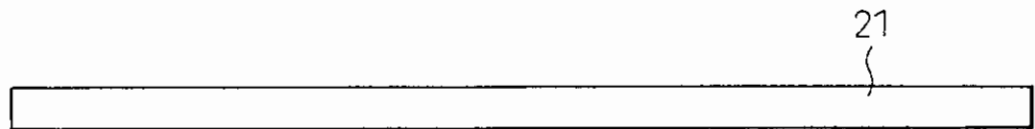


Fig.16(b)

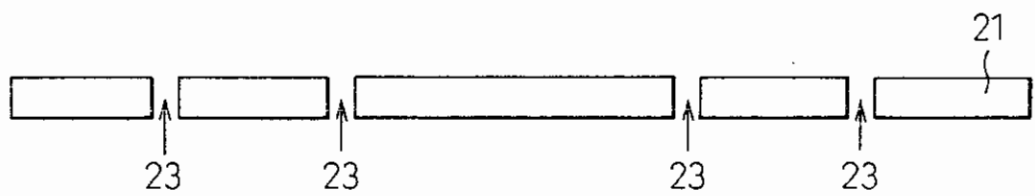


Fig.16(c)

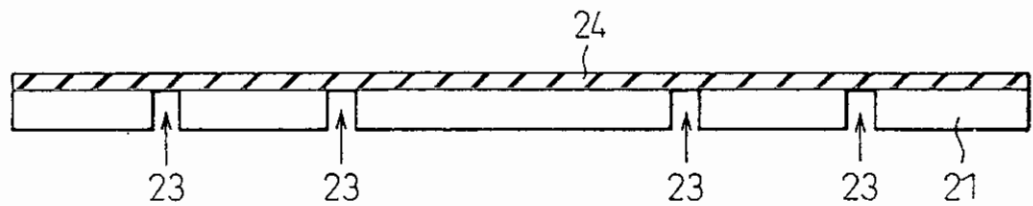


Fig.16(d)

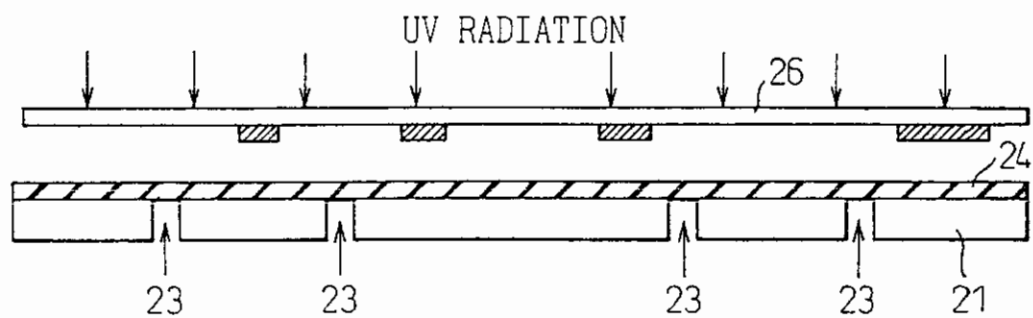


Fig.17(a)

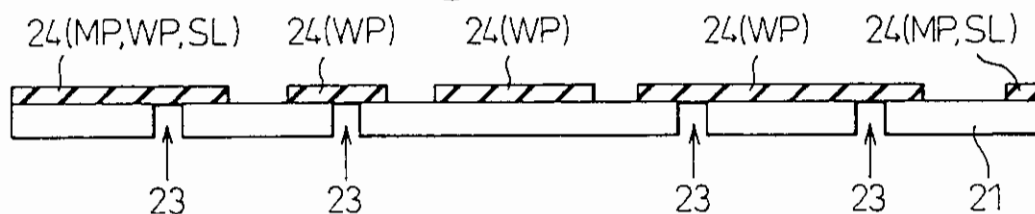


Fig.17(b)

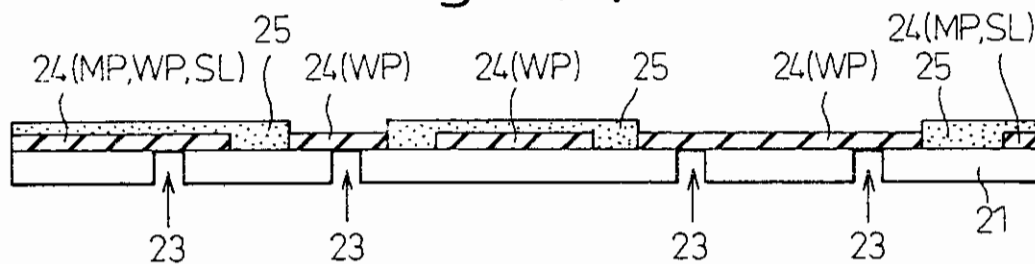


Fig.17(c)

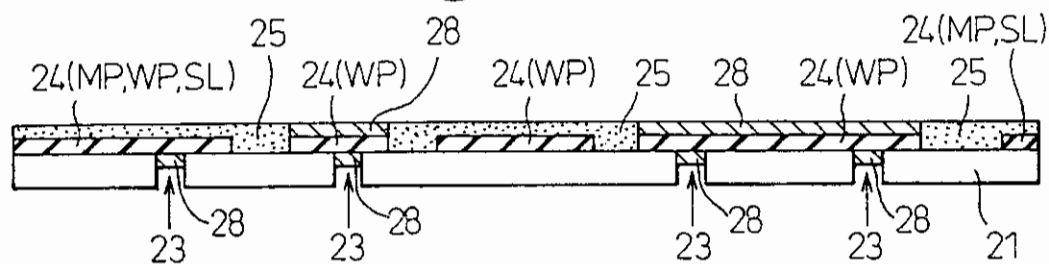


Fig.17(d)

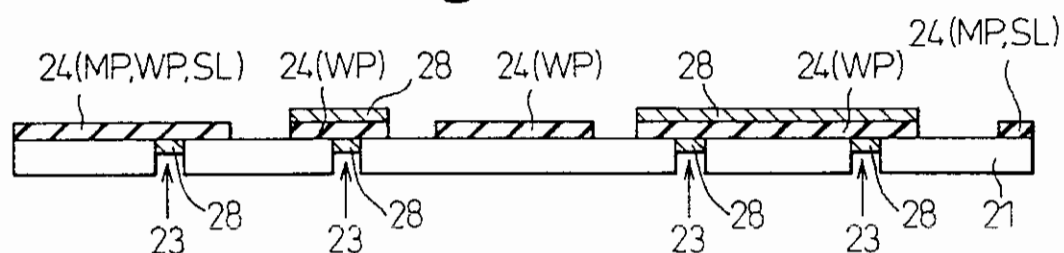


Fig.18(a)

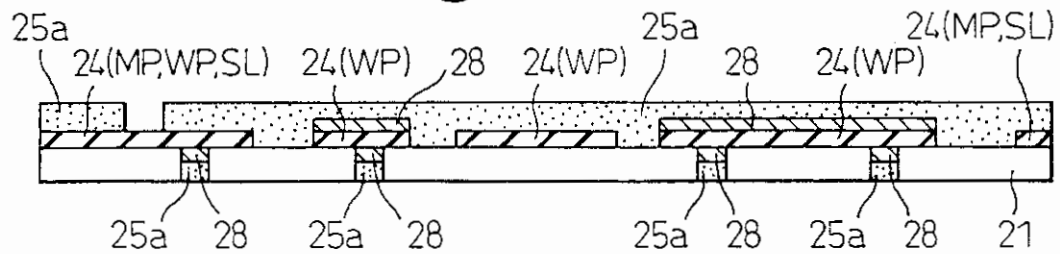
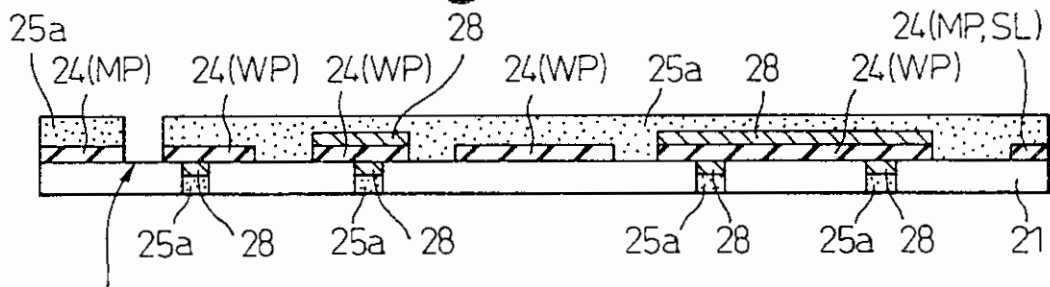
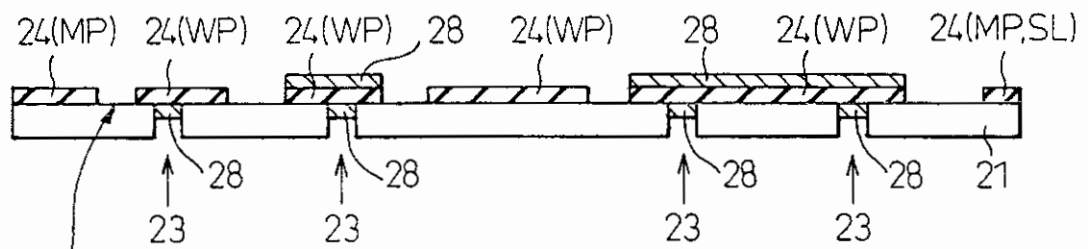


Fig.18(b)



DISCONNECT POWER LINE FOR PLATING FROM SIGNAL LINE

Fig.18(c)



DISCONNECT POWER LINE FOR PLATING FROM SIGNAL LINE

Fig.19(a)

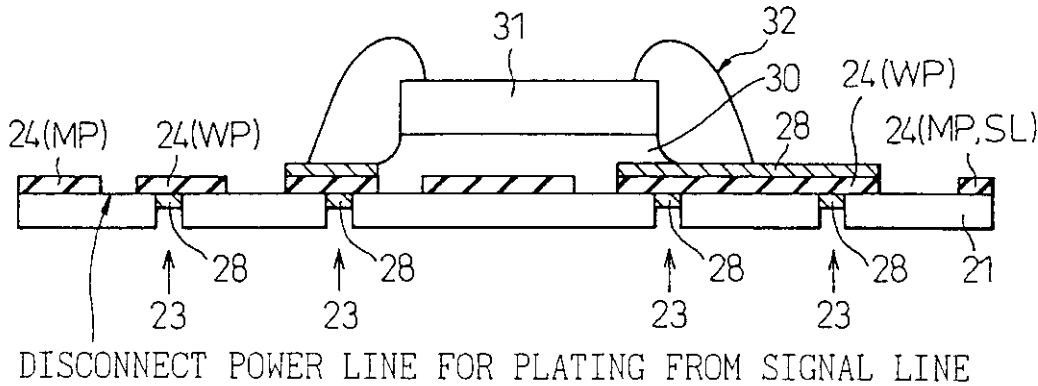


Fig.19(b)

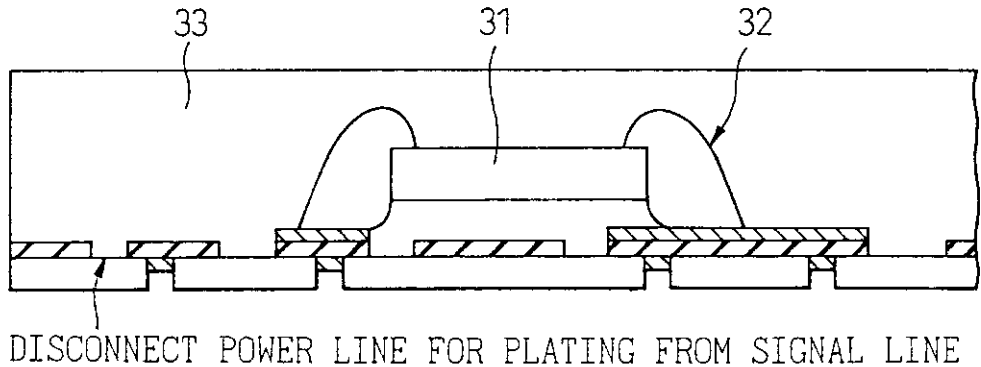
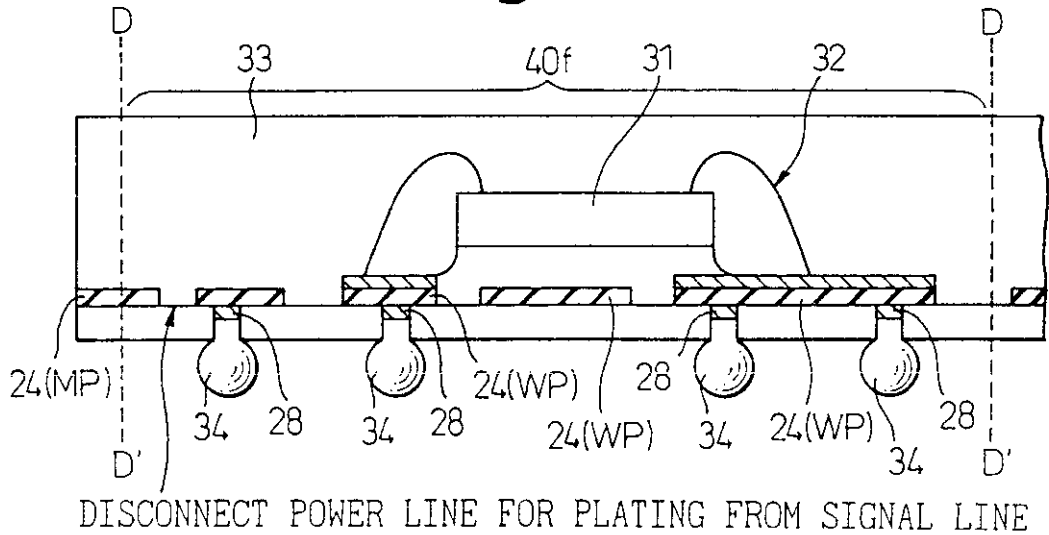
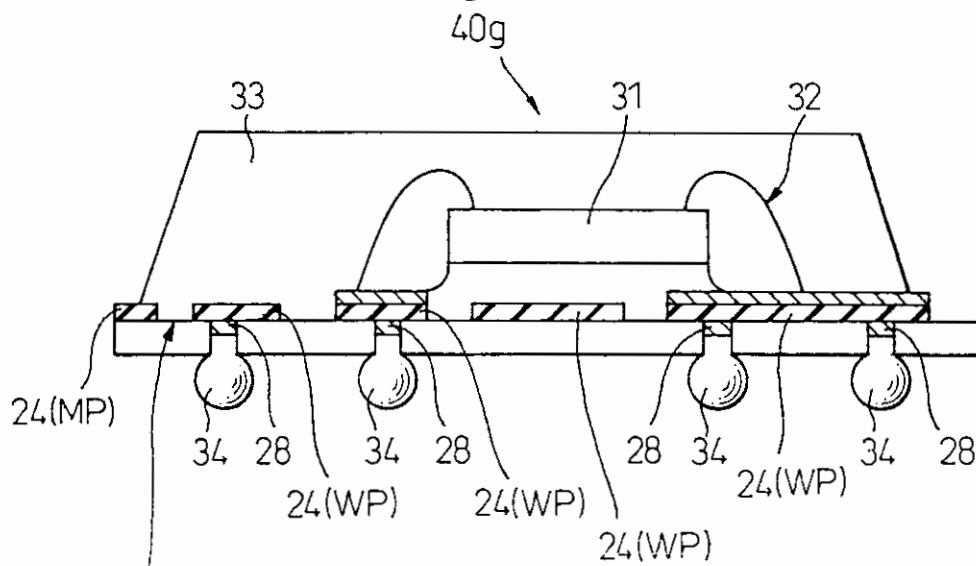


Fig.19(c)



A cross-sectional view of a semiconductor device 40f. The device features a substrate 33 with a central raised region 31. On the left side of the raised region, there is a structure 24(MP) which includes a layer 28 and a component 34. On the right side, there are two structures 24(WP), each consisting of a layer 28 and a component 34. Wires or connections 32 are shown extending from the raised region 31 to the structures 24(MP) and 24(WP). The entire assembly is labeled 40f.

Fig.20(b)



DISCONNECT POWER LINE FOR PLATING FROM SIGNAL LINE