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ACTIVE PIXEL SENSOR WITH
PHOTO DIODE DISCHARGE



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FIELD OF THE INVENTION

The present invention relates to active pixel sensors and, more specifically, to the removal of image artifacts associated with incomplete or inconsistent pixel reset in
10 such sensors.

BACKGROUND OF THE INVENTION

Referring to Figs. 1A-1B, a representative prior art pixel cell (hereinafter referred to as a "pixel") 10 and a
15 timing diagram therefor are respectively shown. Pixel 10 includes a photo diode 11, a reset transistor 13, a read transistor 15, a photo diode output node 17 and pixel output node 19, amongst other components. A typical active pixel sensor (APS) is formed of a plurality of such pixels
20 arranged in an array and having necessary control logic.

Before exposure, the photo diode of pixel 10 (and of all other pixels in an array) is reset by a reset signal, RST, i.e., charged to a reset voltage, V_{RST} , that approaches V_{DD} . During exposure, the photo diode 11
25 discharges to a voltage level, V_{EXP} , that will vary with the amount of incident light. The difference between the V_{RST} and V_{EXP} is thus representative of the amount of incident light on a particular pixel during an exposure time period and is used to generate a resultant image.

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After exposure, a reset signal is propagated to the reset transistor 13 which recharges the photo diode from V_{EXP} towards V_{RST} (shown in Fig. 1B). The actual V_{RST} of each pixel will typically differ, however, based on the V_{EXP} from which the pixel is charged. For example, a photo diode with a low V_{EXP} (i.e., one that was exposed to more incident light) will not charge to the same V_{RST} as a photo diode with a high V_{EXP} . This results in artifacts or ghost images in the resultant output image signal.

The failure to obtain a constant or consistent reset value occurs in part because reset transistor 13 is a MOS transistor that enters the subthreshold region as the photo diode voltage approaches V_{DD} . In this region, the conduction of the MOS transistor wanes and becomes exponential (to a first order). This results in the photo diode never reaching V_{DD} , but slowly converging towards it. With a fixed duration reset signal, pixels charge to different levels based on their respective V_{EXP} at the time charging began. As alluded to above, this in turn results in different final V_{RST} levels at the plurality of photo diodes and the appearance of "ghosting" or "capacitive image light" and the resultant image.

A need thus exists for an APS that minimizes or reduces the presence of artifacts in the resultant image. A need also exists for an APS that reduces these artifacts by providing a consistent reset voltage.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide an APS that reduces or eliminates artifacts in resultant images.

It is another object of the present invention to provide an APS that achieves a consistent reset level for substantially all pixels.

It is also an object of the present invention to
5 provide such an APS that provides these benefits in an efficient and economical manner.

These and related objects of the present invention are achieved by use of an active pixel sensor with photo diode discharge as described herein.

10 In one embodiment, the present invention includes a pixel cell, having a photo diode having an output node, a reset transistor coupled to the photo diode, and a selectably enableable discharging circuit coupled to the photo diode that selectably discharges the photo diode to a low level
15 reference voltage. The discharge circuit may include a gatable connection between the photo diode and the low level reference voltage. Alternatively, the discharge circuit may include a supply voltage to the photo diode that is switchable between a high level reference voltage
20 and the low level reference voltage.

In another embodiment, the present invention includes an active pixel sensor circuit having a plurality of pixel cells each having a photo diode, control logic that propagates a reset signal to the photo
25 diode of each pixel cell, and a discharge circuit coupled to each of the photo diodes for selectably discharging the photo diode. The discharge circuit preferably discharges the photo diodes prior to issuance of a reset signal by the control logic. The present invention also
30 includes an active pixel sensor circuit having pixel cells that each contain a photo diode discharge circuit.

The attainment of the foregoing and related advantages and features of the invention should be more

readily apparent to those skilled in the art, after review of the following more detailed description of the invention taken together with the drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

5 Figs. 1A-1B is a schematic diagram of a representative prior art pixel cell and a timing diagram therefor.

10 Fig. 2 is a schematic diagram of an active pixel sensor in accordance with the present invention.

Figs. 3A-3B is a schematic diagram of a pixel with photo diode discharge and a timing diagram therefor in accordance with the present invention.

15 Figs. 4A-4B is a schematic diagram of an alternative embodiment of a pixel with photo diode discharge and a timing diagram therefor in accordance with the present invention.

DETAILED DESCRIPTION

20 Referring to Fig. 2, a schematic diagram of an APS in accordance with the present invention is shown. APS 20 includes an active pixel array 22 (with a plurality of pixels 30,40, one at each row and column intersection), control logic 24, row decode logic 26 and column output
25 processing logic 28. Control logic 24 produces row select and reset signals (and "discharge signals" as discussed below). Column output processing logic 28 includes column amplifiers, a row buffer and other known circuitry for processing array output signals. Suitable decode and
30 column output processing logic is known in the art. Suitable control logic is also known, albeit without the provision of photo diode discharge and related aspects that are taught herein.

Referring to Figs. 3A-3B, a schematic diagram of a first embodiment of a pixel 30 with photo diode discharging, and a timing diagram therefor, in accordance with the present invention are respectively shown. Pixel cell 30 includes a photo diode 31, reset transistor 33, a read transistor 35, a photo diode output node 37 and a pixel output node 39. Pixel 30 also includes a discharge transistor 36 that discharges the photo diode after V_{EXP} is read.

Control logic 24 (of Fig. 2) generates a discharge signal, DSC, (shown in Fig. 3B) that causes the voltage on photo diode 31 to discharge to ground (or to another suitable low level reference voltage) before the reset signal, RST (also shown in Fig. 3B), is issued. By permitting the photo diodes to be discharged (after V_{EXP} is read), all of the photo diodes of an array are at the same voltage level, e.g., ground or a chosen reference, before the reset signal is issued. Issuance of the reset signal now causes each of the photo diodes to charge to approximately the same voltage level (indicated as V_{RST} in Figs. 3B and 4B) because, in large part, the photo diodes are identical and are charged with the same voltage for the same period of time.

This achieves a consistent V_{RST} among pixels in the array and hence the removal of V_{EXP} dependent artifacts from the resultant image.

Referring to Figs. 4A-4B, a schematic diagram of an alternative embodiment of a pixel 40 with photo diode discharging, and a timing diagram therefor, in accordance with the present invention are respectively shown. Similar to pixels 10 and 30, pixel 40 includes a photo diode 41, a reset transistor 43, a read transistor 45, a photo diode output node 47 and pixel output node 49.

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Pixel 40 also includes a MOS transistor switch 44 (represented in functional form in Fig. 4A) that couples a supply node 51 between a high and a low reference voltage, for example, between V_{DD} and ground. Switch 44
5 may be implemented, for example, as a CMOS inverter with the discharge signal (DSC of Fig. 3B) as the input signal. When switched to ground or the low level reference voltage switch 44 discharges photo diode 41.

Control logic 24 generates the discharge signal that
10 controls switch 44 and has a voltage level that is effectively the complement of the supply node voltage V_{S1} (when switch 44 is implemented as a CMOS inverter). When node 51 is driven low, photo diode 41 discharges through this path causing V_{EXP} to ground. Node 51 is then returned
15 to a high level voltage (V_{DD}) and a reset signal, RST, is generated which pulls the photo diodes (of all pixels in the array) to $V_{RST'}$.

Similar to the arrangement of Fig. 3A, the arrangement of Fig. 4A also achieves a consistent V_{RST}
20 among the pixels of the array and hence the removal of V_{EXP} dependent artifacts from the resultant image.

Figs. 3A and 4A illustrate two embodiments for achieving photo diode discharge and reset, but the present invention is not limited to these two
25 embodiments. Any design that provides photo diode discharge and a uniform reset voltage is within the present invention. Figs. 3A and 4A represent pixel designs that are readily mass producible in a "cell" format and thus lend themselves to use in APS
30 fabrication.

While the invention has been described in connection with specific embodiments thereof, it will be understood that it is capable of further modification, and this

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application is intended to cover any variations, uses, or adaptations of the invention following, in general, the principles of the invention and including such departures from the present disclosure as come within known or customary practice in the art to which the invention pertains and as may be applied to the essential features hereinbefore set forth, and as fall within the scope of the invention and the limits of the appended claims.

CLAIMS

1. A pixel cell, comprising:
photo diode having an output node;
5 a reset circuit coupled to said photo diode; and
a selectably enableable discharging circuit coupled to
said photo diode that selectably discharges said photo diode
to a given reference voltage, wherein activation of said
reset circuit when said discharging circuit is not enabled
10 achieves a charging of said photo diode.
2. The pixel cell of claim 1, wherein said discharging
circuit includes a gatable connection between said photo
diode output node and said given reference voltage.
- 15 3. The pixel cell of claim 1, wherein said reset circuit
includes a reset transistor and said photo diode output node
is coupled to said reset transistor, and further wherein a
supply to said reset transistor is switchable between a high
20 level reference voltage and said given reference voltage.
4. The pixel cell of claim 3, further comprising a switch
provided in the supply to said reset transistor, said switch
being switchable between a high level and said given
25 reference voltage, said given reference voltage serving to
discharge said photo diode.
5. The pixel cell of claim 1, wherein said given reference
voltage is a low level reference voltage equal approximately
30 to ground.
6. The pixel cell of claim 2, wherein said gatable
connection is a MOS transistor.

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7. The pixel cell of claim 4, wherein said switch is a MOS inverter switch.

8. The pixel cell of claim 1, wherein said photo diode is reverse biased.

9. An active pixel sensor circuit, comprising:
a plurality of pixel cells each having a photo diode;
control logic that propagates a reset signal to the
photo diode of each pixel cell; and
a discharge circuit coupled to each of said photo diodes
for discharging the photo diode.

10. The circuit of claim 9, wherein said discharge circuit discharges said photo diodes prior to issuance of a reset signal by the control logic.

11. The circuit of claim 9, wherein said discharge circuit includes a selectively enableable discharge transistor coupled between the photo diode of each pixel cell and a low level reference voltage.

12. The circuit of claim 9, wherein each pixel cell includes a reset transistor coupled to the photo diode of that pixel cell, and the supply of each reset transistor is switchable between a high level and a low level reference voltage.

13. The circuit of claim 12, wherein said switchable supply is achieved with a MOS switch.

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14. The circuit of claim 9, wherein each pixel cell includes a reset transistor coupled to the photo diode of that pixel cell, and activation of the reset transistor when said

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discharge circuit is not enabled achieves a charging of said photo diode.

15. A method of operating an active pixel sensor (APS),
5 comprising the steps of:

providing an APS having a plurality of pixel cells that each include a photo diode, a reset circuit and a discharge circuit;

10 resetting the photo diode of each pixel cell after exposure; and

discharging the photo diode of each pixel cell before said resetting step.

16. The method of claim 15, wherein said discharging step
15 includes the step of discharging each photo diode to a low level reference voltage.