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COMPUTER SYSTEM

The present invention relates to a computer system and in particular to apparatus for installing BIOS in a personal computer system.

Personal computer systems in general have attained widespread use for providing computer power to many segments of today's modern society. Personal computer systems can usually be defined as a desk top, floor standing, or portable microcomputer that consists of a system unit having a single system processor, a display monitor, a keyboard, one or more diskette drives, a fixed disk storage, and an optional printer. One of the distinguishing characteristics of these systems is the use of a motherboard or system planar to electrically connect these components together. These systems are designed primarily to give independent computing power to a single user and are inexpensively priced for purchase by individuals or small businesses. Examples of such personal computer systems include the IBM PERSONAL COMPUTER AT and the IBM PERSONAL SYSTEM/2 Models 30, 50, 60, 70 and 80.

These systems can be classified into two general families. The first family, usually referred to as Family I Models, use a bus architecture exemplified by the IBM PERSONAL COMPUTER AT. The second family, referred to as Family II Models, use MICROCHANNEL bus architecture exemplified by the IBM PERSONAL SYSTEM/2 Models 50 through 80.

In early examples of family I personal computer systems such as the IBM Personal Computer, it was recognised that software compatibility would be of utmost importance. In order to achieve this goal, an insulation layer of system resident code, also referred to as "microcode", was established between the hardware and software. This code provided an operational interface between a user's application program/operating system and the device to

relieve the user of the concern about the characteristics of hardware devices. Eventually, the code developed into a Basic Input/Output system (BIOS), for allowing new devices to be added to the system, while insulating the application program from the peculiarities of the hardware. The importance of BIOS was immediately evident because it freed a device driver from depending on specific device hardware characteristics while providing the device driver with an intermediate interface to the device. Since BIOS was an integral part of the system and controlled the movement of data in and out of the system processor, it was resident on the system planar and was shipped to the user in a read only memory (ROM). For example, BIOS in the IBM Personal Computer occupied 8K of ROM resident on the planar board.

As new models of the personal computer family were introduced, BIOS had to be updated and expanded to include new hardware and I/O devices. As could be expected, BIOS started to increase in memory size. For example, BIOS in the IBM PERSONAL COMPUTER AT, occupied 32K bytes of ROM.

Today, with the development of new technology, personal computer systems of the Family II models are growing even more sophisticated and are being made available to consumers more frequently. Since the technology is rapidly changing and new I/O devices are being added to the personal computer systems, modification to the BIOS has become a significant problem in the development cycle of the personal computer system.

For instance, with the introduction of the IBM Personal System/2 with MICROCHANNEL architecture, a significantly new BIOS, known as advanced BIOS, or ABIOS, was developed. However, to maintain software compatibility, BIOS from the Family I models had to be included in the Family II models. The Family I BIOS became known as Compatibility BIOS or CBIOS. However, as previously explained with respect to the IBM PERSONAL COMPUTER AT, only 32K

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bytes of ROM were resident on the planar board. Fortunately, the system could be expanded to 96K bytes of ROM. Unfortunately, because of system constraints, this turned out to be the maximum capacity available for BIOS. Luckily, even with the addition of ABIOS, ABIOS and CBIOS could still squeeze into 96K of ROM. However, only a small percentage of the 96K ROM area remained available for expansion. With the addition of future I/O devices, CBIOS and ABIOS will eventually run out of ROM space. Thus, new I/O technology will not be able to be easily integrated within CBIOS and ABIOS.

Due to these problems, plus the desire to make modification in Family II BIOS as late as possible in the development cycle, it has become necessary to off load portions of BIOS from the ROM. Since marketability and consumer acceptance of personal computer systems appear to require the ability to add new I/O devices and to minimize cost, it should be appreciated that easy modification of Family II models' BIOS is a substantial factor in achieving success in accordance with this invention. Thus, there exists a need for developing a method and apparatus which permits portions of BIOS to be stored on a direct access storage device such as a fixed disk or on the diskette drive. These portions can then be easily modified and loaded into the personal computer system when required.

An aim of the present invention is to a provide a computer system having apparatus for increasing the number of devices BIOS supports by storing a portion of BIOS on a direct access storage device.

In accordance with the present invention, there is now provided, a computer system comprising: a system processor electrically coupled to a random access memory; a direct access storage device electrically coupled to the system processor, the direct access storage device being capable of storing a plurality of data records; a read only memory being electrically coupled to the system processor; characterised in that the system further

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comprises: a master boot record included in the direct access storage device, the master boot record having an executable code segment; a first portion of BIOS included in the read only memory, the first portion of BIOS initializing the system and the direct access storage device to load the master boot record into random access memory; and a remaining portion of BIOS included in the direct access storage device, wherein the first portion of BIOS transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of BIOS into the random access memory, the remaining portion of BIOS initializing the rest of the system in order to load in an operating system to begin operation of the system.

Viewing the present invention form a second aspect, there is now provided an apparatus for loading BIOS into a personal computer system, the personal computer system including a system processor and a random access memory electrically coupled, the apparatus comprising: a direct access storage device being electrically coupled to the system processor, the direct access storage device being capable of storing a plurality of data records; a master boot record included in the direct access storage device, the master boot record including an executable code segment; a read only memory being electrically coupled to the system processor; a first portion of BIOS being included in the read only memory, the first portion of BIOS initialising the system and the direct access storage device to load in the master boot record into random access memory; and a remaining portion of BIOS being included in the direct access storage device, wherein the first portion of BIOS transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of BIOS into the random access memory, the remaining portion of BIOS initialising the rest of the personal computer system in order to load in an operating system to begin operation of the personal computer system.

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Viewing the present invention from a third aspect, there is now provided, a personal computer system comprising: a system processor; a random access memory being the main memory and electrically coupled to the system processor; a system planar board having a plurality of I/O slots being electrically coupled to the system processor, a direct access storage device being electrically coupled to the system processor, the direct access storage device capable of storing a plurality of data records; a master boot record included in the direct access storage device, the master boot record having a data segment and an executable code segment, the data segment representing a hardware configuration of the personal computer system which is compatible with the master boot record; a read only memory being electrically coupled to the system processor, the read only memory having data representing a hardware configuration of the system; a first portion of BIOS being included in the read only memory, the first portion of BIOS initializing the system and the direct access storage device to load in the master boot record, the first portion of BIOS further comparing the hardware configuration data from the master boot record to the hardware configuration data of the read only memory to verify the compatibility of the master boot record with the system processor; a remaining portion of BIOS being included in the direct access storage device, wherein, after verifying the compatibility of the master boot record with the system processor, the first portion of BIOS transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of BIOS into the random access memory.

The data segment of the master boot record preferably includes a value representing a system planar being compatible with the master boot record and further wherein the system planar further includes a means for uniquely identifying the system planar in order to verify the compatibility of the master boot record to the system planar.

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The hardware configuration data on the master boot record preferably includes a model value and a submodel value, wherein the model value identifies the system processor and the submodel value represent the I/O configuration of the system planar, the model value and submodel value being compared to corresponding values in the read only memory to verify the compatibility of the master boot record to the hardware configuration.

An example of a personal computer system of the present invention further includes a nonvolatile random access memory, the nonvolatile random access memory storing values representing the system configuration, the values being updated when the configuration of the system is changed, wherein the first portion of BIOS compares the values in the nonvolatile random access memory to corresponding values in the read only memory to determine if the configuration of the system has changed.

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Viewing the present invention from a fourth aspect, there is now provided, apparatus for loading BIOS into a personal computer system having a system processor being electrically coupled to a random access memory, the apparatus comprising: a direct access storage device being electrically coupled to the system processor, the direct access storage device being a read only memory being electrically coupled to the system processor; a first portion of BIOS being included in the read only memory; and a remaining portion of BIOS being included in the direct access storage device, wherein the first portion of BIOS initializes the system processor and direct storage device to effect load the remaining portion of BIOS into random access memory, the remaining portion of BIOS effectively superseding the first portion of BIOS to assist in the operation of the system.

Viewing the present invention from a fifth aspect, there is now provided a method for loading BIOS from a direct access storage device of a personal computer system, the personal computer system having a system processor electrically coupled to a system planar, the planar further being electrically coupled to a random access memory, a read only memory, and the direct access storage device, the method comprising the steps of:

(a) initializing the system with a first portion of BIOS resident in the read only memory;

(b) initializing with the first portion of BIOS the direct access storage device, the direct access storage device further having a master boot record and the remaining BIOS;

(c) loading with the first portion of BIOS the master boot record into random access memory, the master boot record including a data segment and an executable code segment, the data segment having data representing the hardware of the system for which the remaining BIOS is compatible;

(d) verifying the compatibility of the master boot record with the system hardware by comparing the data representing the system

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hardware to corresponding compatibility data stored in the read only memory; and

(e) executing the code segment of the master boot record to load the remaining BIOS into the random access memory; and

(f) passing control to the remaining BIOS once it is loaded into random access memory;

The method preferably further comprises the steps of:

(g) verifying that the master boot record is compatible with the planar by comparing a planar ID accessible by the system processor with a planar ID value stored in the data segment of the master boot record; and

(h) verifying that the master boot record is compatible with the system processor and I/O configuration of the planar by comparing respectively model and submodel values stored in the read only memory with model and submodel values stored in the data segment of the master boot record.

In an example of a computer system of the present invention further including a nonvolatile memory being electrically coupled to the system processor, wherein the nonvolatile memory includes data representing the system configuration, the method preferably further comprises the step of:

(i) comparing the data in nonvolatile random access memory to the data in read only memory to determine whether the system configuration has changed; and

(j) generating an indication that the system configuration has changed before loading the BIOS from the direct access storage device.

In a preferred arrangement, step (c) of loading can include the steps of:

(k) searching through a predetermined number of records on the direct access image device for a master boot record;

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(l) identifying the master boot record with an identifying means included within the master boot record.

(m) loading the master boot record into random access memory upon locating the master boot record among the data records on the direct access storage device.

Furthermore, the method preferably includes the step of validating successful load of the master boot record.

In a preferred example of the present invention to be described later, there is provided a computer system comprising a system processor, a random access main memory, a read only memory, and at least one direct access storage device. The read only memory includes a first portion of BIOS. The first portion of BIOS initializes the system processor and the direct access storage device to read a master boot record from the direct access storage device into the random access memory.

The master boot record includes a data segment and an executable code segment. The data segment includes data representing system hardware and a system configuration which is supported by the master boot record. The first BIOS portion confirms the master boot record is compatible with the system hardware by verifying the data from the data segment of the master boot record agrees with data included within the first BIOS portion representing the system processor, system planar, and planar I/O configuration.

If the master boot record is compatible with the system hardware, the first BIOS portion vectors the system processor to execute the executable code segment of the master boot record. The executable code segment confirms that the system configuration has not changed and loads in the remaining BIOS portion from the direct access storage device into random access memory. The executable code segment then verifies the authenticity of the remaining BIOS

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portion and vectors the system processor to begin executing the BIOS now in random access memory. BIOS, executing in random access memory, then boots up the operating system to begin operation of the personal computer system. The first BIOS portion, being no longer addressable and superseded by the remaining BIOS portion, is abandoned.

A computer system having apparatus for loading BIOS from a direct access storage device into main memory is now provided in accordance with the present invention. Furthermore, the computer system comprises apparatus and method which confirms the compatibility between BIOS and the personal computer system. Also, the computer system comprises means for verifying the system configuration before loading BIOS from the direct access storage device.

An embodiment of the present invention will now be described with reference to the accompanying drawings in which:

Fig. 1 illustrates a cut away view of a personal computer system showing a system planar board connected to a plurality of direct access storage devices;

Fig. 2 shows a system block diagram for the personal computer system of Fig. 1;

Fig. 3 is a memory map for the ROM BIOS included on the planar board;

Fig. 4 is a flowchart describing the overall process for loading a BIOS image from a direct access storage device;

Fig. 5 illustrates the record format for the master boot record;

Fig. 6A is a flowchart describing the operation of the IBL routine;

Fig. 6B is a flowchart showing the steps for loading a BIOS image from a fixed disk;

Fig. 6C is a flowchart showing the steps for loading the BIOS image from a diskette;

Fig. 6D is a flowchart showing greater detail in checking the compatibility between the master boot record and the planar/processor; and

Fig. 7 is a detailed flowchart showing the operation of the executable code segment of the master boot record.

The following detailed description is of the best presently contemplated mode for carrying out the invention. This description is not to be taken in a limiting sense but is made merely for the purpose of illustrating the general principles of the invention since the scope of the invention is best defined by the appending claims.

Referring now to the drawings, and in particular to Fig. 1, there is shown a cutaway version of a personal computer system 10, having a plurality of DASD (Direct Access Storage Devices) 12 - 16 connected to a system or planar board 24 through a plurality of I/O slots 18. A power supply 22 provides electrical power to the system 10 in a manner well known. The planar board 24 includes a system processor which operates under the control of computer instructions to input, process, and output information.

In use, the personal computer system 10 is designed primarily to give independent computing power to a small group of users or a single user and is inexpensively priced for purchase by individuals

or small businesses. In operation, the system processor operates under an operating system, such as IBM's OS/2 Operating System or PC-DOS. This type of operating system includes a BIOS interface between the DASD 12 - 16 and the Operating System. A portion of BIOS divided into modules by function is stored in ROM on the planar 24 and hereinafter will be referred to as ROM-BIOS. BIOS provides an interface between the hardware and the operating system software to enable a programmer or user to program their machines without an indepth operating knowledge of a particular device. For example, a BIOS diskette module permits a programmer to program the diskette drive without an indepth knowledge of the diskette drive hardware. Thus, a number of diskette drives designed and manufactured by different companies can be used in the system. This not only lowers the cost of the system 10, but permits a user to choose from a number of diskette drives.

Prior to relating the above structure to the present invention, a summary of the operation in general of the personal computer system 10 may merit review. Referring to Fig. 2, there is shown a block diagram of the personal computer system 10. Fig. 2 illustrates components of the planar 24 and the connection of the planar 24 to the I/O slots 18 and other hardware of the personal computer system. Located on the planar 24 is the system processor 26 comprised of a microprocessor which is connected by a local bus 28 to a memory controller 30 which is further connected to a random access memory (RAM) 32. While any appropriate microprocessor can be used, one suitable microprocessor is the 80386 which is sold by Intel.

While the present invention is described hereinafter with particular reference to the system block diagram of Fig. 2, it is to be understood at the outset of the description which follows, it is contemplated that the apparatus and methods in accordance with the present invention may be used with other hardware configurations of

the planar board. For example, the system processor could be an Intel 80286 or 80486 microprocessor.

Accessible by the processor is a planar identification number (planar ID). The planar ID is unique to the planar and identifies the type of planar being used. For example, the planar ID can be hardwired to be read through an I/O port of the system/processor 26 by using switches.

The local bus 28 is further connected through a bus controller 34 to a read only memory (ROM) 36 on the planar 24.

An additional nonvolatile memory (NVRAM) 58 is connected to the microprocessor 26 through a serial/parallel port interface 40 which is further connected to bus controller 34. The nonvolatile memory can be CMOS with battery backup to retain information whenever power is removed from the system. Since the ROM is normally resident on the planar, model and submodel values stored in ROM are used to identify the system processor and the system planar I/O configuration respectively. Thus these values will physically identify the processor and planar I/O configuration. The NVRAM is used to store system configuration data. That is, the NVRAM will contain values which describe the present configuration of the system. For example, NVRAM contains information describing the capacity of a fixed disk or diskette, the type of display, the amount of memory, time, date, etc. Additionally, the model and submodel values stored in ROM are copied to NVRAM whenever a special configuration program, such as SET Configuration, is executed. The purpose of the SET Configuration program is to store values characterizing the configuration of the system in NVRAM. Thus for a system that is configured properly, the model and submodel values in NVRAM will be equal respectively to the model and submodel values stored in ROM. If these values are not equal, this indicates that the configuration of the system has been modified. Reference is

made to Fig. 6D, where this feature in combination with loading BIOS is explained in greater detail.

Continuing, our discussion with reference to Fig. 2, the bus controller 34 is further coupled to I/O slots 18, the serial/parallel interface 40 and peripheral controller 42 by an I/O planar bus 43. The peripheral controller 42 is further connected to a keyboard 44, mouse 46, diagnostic panel 47, and diskette controller 64. Beside the NVRAM 58, the serial/parallel interface 40 is further connected to a serial port 48 and parallel port 50 to input/output information to a printer, hard copy device, etc. As is well known in the art, the local bus 28 can also be connected to a cache controller 52, a cache memory 68, a co-processor 54, and a DMA controller 56.

The system processor 26 controls its internal operation as well as interfacing with other elements of the personal computer system 10. For example, system processor 26 is shown connected to a small computer system interface (SCSI) I/O card 60 which is further connected to a DASD, such as a fixed disk drive 62. It is to be understood that other than a SCSI disk drive can be used as a fixed disk in accordance with the present invention. In addition to the fixed disk 62, the system processor 26 can be interfaced to the diskette controller 64 which controls a diskette drive 66. With respect to terminology, it is also to be understood that the term "hardfile" describes fixed disk drive 62 while the term "floppy" also describes diskette drive 66.

Previous to the present invention, ROM 36 could include all of the BIOS code which interfaced the operating system to the hardware peripherals. According to one aspect of the present invention, however, ROM 36 is adapted to store only a portion of BIOS. This portion, when executed by the system processor 26, inputs from either the fixed disk 62 or diskette 66 a second or remaining portion of BIOS, hereinafter also referred to as a BIOS image. This

BIOS image supersedes the first BIOS portion and being an integral part of the system is resident in main memory such as RAM 32. The first portion of BIOS (ROM-BIOS) as stored in ROM 36 will be explained generally with respect to Figs. 3-4 and in detail with respect to Figs. 6A-D. The second portion of BIOS (BIOS image) will be explained with respect to Fig. 5, and the loading of the BIOS image with respect to Fig. 7. Another benefit from loading a BIOS image from a DASD is the ability to load BIOS directly into the system processor's RAM 32. Since accessing RAM is much faster than accessing ROM, a significant improvement in the processing speed of the computer system is achieved.

The explanation will now proceed to the operation of the BIOS in ROM 36 and to the operation of loading the BIOS image from either the fixed disk or diskette. In general, ROM-BIOS prechecks the system and loads a BIOS master boot record into RAM. The master boot record includes a data segment having validation information and a code segment having executable code. The executable code uses the data information to validate hardware compatibility and system configuration. After testing for hardware compatibility and proper system configuration, the executable code loads the BIOS image into RAM. The BIOS image succeeds ROMBIOS and loads the operating system to begin operation of the machine.
For purposes of clarity, the executable code segment of the master boot record will be referred to as MBR code while the data segment will be referred to as MBR data.

Referring to Fig. 3 there is a memory map showing the different code modules which comprise ROM-BIOS. ROM-BIOS includes a power on self test (POST) stage I module 70, an Initial BIOS Load (IBL) Routine module 72, a Diskette module 74, a hardfile module 76, a video module 78, a diagnostic- panel module 80, and hardware compatibility data 82. Briefly, POST Stage I 70 performs system pre-initialization and tests. The IBL routine 72 determines whether the BIOS image is to be loaded from disk or diskette, checks

compatibility and loads the master boot record. Diskette module 74 provides input/output functions for a diskette drive. Hardfile module 76 controls I/O to a fixed disk or the like. Video module 78 controls output functions to a video I/O controller which is further connected to a video display. Diagnostic panel module 80 provides control to a diagnostic display device for the system. The hardware compatibility data 82 includes such values as a system model and submodel values which are described later with respect to Fig. 5.

Referring now to Fig. 4, there is shown a process overview for loading a BIOS image into the system from either the fixed disk or the diskette. When the system is powered up, the system processor is vectored to the entry point of POST Stage I, step 100. POST Stage I initializes the system and tests only those system functions needed to load BIOS image from the selected DASD, step 102. In particular, POST Stage I initializes the processor/planar functions, diagnostic panel, memory subsystem, interrupt controllers, timers, DMA subsystem, fixed disk BIOS routine (Hardfile module 76), and diskette BIOS routine (Diskette module 74), if necessary.

After POST Stage I pre-initializes the system, POST Stage I vectors the system processor to the Initial BIOS Load (IBL) routine included in the Initial BIOS Load module 72. The IBL routine first, determines whether the BIOS image is stored on fixed disk or can be loaded from diskette; and second, loads the master boot record from the selected media (either disk or diskette) into RAM, step 104. The master boot record includes the MBR data and the MBR code. The MBR data is used for verification purposes and the MBR code is executed to load in the BIOS image. A detailed description of the operation of the IBL routine is presented with respect to Figs. 6A-D.

With continuing reference to Fig. 4, after the IBL routine loads the master boot record into RAM, the system processor is vectored to the starting address of the MBR code to begin execution,

step 106. The MBR code performs a series of validity tests to determine the authenticity of the BIOS image and to verify the configuration of the system. For a better understanding of the operation of the MBR code, attention is directed to Fig. 7 of the drawings wherein the MBR code is described in greater detail.

On the basis of these validity tests, the MBR code loads the BIOS image into RAM and transfers control to the newly loaded BIOS image in main memory, step 108. In particular, the BIOS image is loaded into the address space previously occupied by ROM-BIOS. That is if ROM-BIOS is addressed from E0000H thru FFFFFH, then the BIOS image is loaded into this RAM address space thus superseding ROM-BIOS. Control is then transferred to POST Stage II which is included in the newly loaded BIOS image thus abandoning ROM-BIOS. POST Stage II, now in RAM, initializes and tests the remaining system in order to load the operating system boot, step 110. After the system is initialized and tested, Stage II POST transfers control to the operating system boot to load the operating system, steps 112-114. It is noted that during a warm start, the processor is vectored to step 108, bypassing steps 100- 106.

For clarity, it is appropriate at this point to illustrate a representation for the format of the master boot record. Referring to Fig. 5, there is shown the master boot record. The boot record includes the executable code segment 120 and data segments 122-138. The MBR code 120 includes DASD dependent code responsible for verifying the identity of the ROM-BIOS, checking that the IBL boot record is compatible with the system, verifying the system configuration, and loading the BIOS image from the selected DASD (disk or diskette). The data segments 122-138 include information used to define the media, identify and verify the master boot record, locate the BIOS image, and load the BIOS image.

The master boot record is identified by a boot record signature 122. The boot record signature 122 can be a unique bit pattern,

such as a character string "ABC", in the first three bytes of the record. The integrity of the master boot record is tested by a checksum value 132 which is compared to a computed checksum value when the boot record is loaded. The data segments further include at least one compatible planar ID value 134, compatible model and submodel values 136. The master boot record's planar ID value defines which planar that the master boot record is valid for. Similarly, the master boot record's model and submodel values define the processor and planar I/O configuration respectively that the master boot record is valid for. It is noted that the boot record's signature and checksum identify a valid master boot record, while the boot record's planar ID, boot record's model and boot record's submodel comparisons are used to identify a boot record compatible with the system and to determine if the system configuration is valid. Another value, boot record pattern 124 is used to determine the validity of the ROM-BIOS. The boot record pattern 124 is compared to a corresponding pattern value stored in ROM. If the values match this indicates that a valid ROM-BIOS has initiated the load of a BIOS image from the selected media.

The following description further describes in greater detail each of the values in the master boot record and their functions:

MBR Identifier (122): The first three bytes of the IBL boot record can consist of characters, such as "ABC". This signature is used to identify a boot record.

MBR Code Segment (120): This code verifies the compatibility of the boot record with the planar and processor by comparing corresponding planar id and model/submodel values. If these values match, it will load the BIOS image from the chosen media to system RAM. If the system image (BIOS image loaded into memory) checksum is valid and no media load errors occur, the MBR code will transfer control to the POST Stage II routine of the system image.

MBR Pattern (124): The first field of the IBL boot record data segment contains a pattern, such as a character string "ROM-BIOS 1989". This string is used to validate the ROM-BIOS by comparing

the Boot Pattern value to the corresponding value stored in ROM (ROM-Pattern).

MBR Version Date (126): The master boot record includes a version date for use by an update utility.

System Partition Pointer (128): The data segment contains a media pointer to the beginning of the media system partition area for use by Stage II POST. On an IBL diskette, the pointer is in track-head-sector format; on disk the pointer is in Relative Block Address (RBA) format.

System Partition Type (130): The system partition type indicates the structure of the media system partition. There are three types of system partition structures - full, minimal and not present. The full system partition contains the setup utility and diagnostics in addition to the BIOS image and master boot record. The minimal system partition contains just the BIOS image and master boot record. It may occur where a system does not have access to a hardfile having an IBL image, in this circumstance the system partition type indicates not present. In this instance, IBL will occur from the diskette. These three system partition types allow flexibility in how much space the system partition takes up on the media.

Checksum value (132): The checksum value of the data segment is initialized to generate a valid checksum for the record length value (1.5k bytes) of the master boot record code.

MBR Planar ID Value (134): The data segment includes a value, such as a string of words defining compatible planar IDs. Each word is made up of a 16 bit planar ID and the string is terminated by word value of zero. If a system's planar ID matches the planar ID value in the master boot record, such as one of the words in the string, the IBL media image is compatible with the system planar. If the system's planar ID does not match any word in the string, the IBL media image is not compatible with the system planar.

MBR model and submodel values (136): The data segment includes values, such as a string of words defining compatible processors.

Each word is made up of a model and submodel value and the string is terminated by a word value of zero. If a system's model and submodel value (stored in ROM) match one of the words in the string, the IBL media image is compatible with the system processor. If the ROM model and ROM submodel values do not match any word in the string, the IBL media image is not compatible with the system processor.

MBR Map length (138): The IBL map length is initialized to the number of media image blocks. In other words, if the BIOS image is broken into four blocks, the map length will be four indicating four block pointer/length fields. Usually this length is set to one, since the media image is one contiguous 128k block.

MBR Media Sector Size (138): This word value is initialized to the media sector size in bytes per sector.

Media image block pointer (138): The media image block pointer locates a system image block on the media. Normally, there is only one pointer since the media image is stored as one contiguous block. On an IBL diskette, the pointers are in track-head-sector format; on disk the pointers are relative block address format.

Media image block length (138): The media image block length indicates the size (in sectors) of the block located at the corresponding image block pointer. In the case of a 128k contiguous media image, which includes space for BASIC, this field is set to 256, indicating that the BIOS image block takes up 256 sectors (512 bytes/sector) starting at the media image block pointer location.

Referring now to Figs. 6A-D, there is shown a detailed flow chart of the operation of the IBL routine. Under normal circumstances, the IBL routine loads the master boot record from the system fixed disk into RAM at a specific address and then vectors the system processor to begin executing the code segment of the master boot record. The IBL routine also contains provisions for a diskette default mode in which the master boot record can be loaded from diskette. However, the IBL routine does not allow the diskette default mode to be performed if the system contains the IBL media on

the system fixed disk and a valid password is present in NVRAM. The user has the option of setting the password in NVRAM. The purpose of preventing the diskette default mode from being effected is to prevent loading an unauthorized BIOS image from diskette. In other words, the diskette default mode is used only when a system fixed disk is not operational and the user has indicated (by not setting the password) the desire to be able to load from the diskette. If the IBL routine is not able to load the master boot record from either media, an error message is generated and the system is halted.

Referring now to Fig. 6A, under normal circumstances the system will contain a system fixed disk which the IBL routine initializes, step 150. Assume for purposes of illustration that the fixed disk is configured for Drive C of the personal computer system. Similarly, assume Drive A is designated as the diskette drive. The IBL routine then examines Drive C to determine whether it contains IBL media, step 152. Attention is directed to Fig. 6B which describes in detail this process. The IBL routine starts reading from the fixed disk at the last three sectors and continues reading, decrementing the media pointer, for 99 sectors or until a valid master boot record is found. If a master boot record is found, it is checked for system planar and processor compatibility, step 156. If it is not planar or processor compatabile, then an error is reported, step 158. Referring back to step 152, if no master boot record is found on the last 99 sectors of the fixed disk (primary hardfile), an error is reported, step 154.

Referring back to step 156, if a master boot record is found, a series of validity checks are performed to determine if the master boot record is compatible with the computer system. Additionally, the configuration of the system is checked. Attention is directed to Fig. 6D which discloses this process in greater detail. If the boot record is compatible with the planar ID, model and submodel, and if furthermore the system configuration has not changed the

master boot record is loaded and the code segment of the master boot record is executed, step 160.

Referring back to steps 154 and 158, if an error occurs in loading the master boot record from the fixed disk or if a fixed disk is not available, the IBL routine determines if a valid password is included in NVRAM, step 162. This password determines whether the BIOS image can be loaded from diskette. Note that the password will exist only upon being installed by the user running a setup utility. If a password is installed in NVRAM, the BIOS image is prevented from being loaded from diskette, step 164. This permits the user to ensure the integrity of the operation of the system by causing the system to be loaded only with the BIOS image on the fixed disk. The password can take the form of a string of characters stored in NVRAM.

Referring back to step 162, if a valid password in NVRAM is not present, thus allowing BIOS image to be loaded from diskette, the IBL routine initializes the diskette subsystem, step 166. The IBL routine then determines if Drive A includes the IBL media on a diskette, step 168. If Drive A does not include IBL media, an error is generated to notify the user that an invalid diskette has been inserted in the drive, step 170. The system then halts, step 172. Attention is directed to Fig. 6C for a more detailed discussion of step 168.

Referring back to step 168, after Drive A is checked for IBL media, the master boot record is loaded into RAM and the code segment included in the master boot record is executed, step 160. It is important to note that for diskette the IBL routine does not include the validity checks that are used with the fixed disk system. The reason for the absence of the validity checks is for loading a noncompatible IBL image from diskette. For example, if a new processor is added to the system, a new BIOS image will be included on a diskette. Since a new processor will cause validity

errors when loading from fixed disk, the IBL routine provides the ability to bypass these tests by loading the BIOS image from diskette.

To recapitulate, the master boot record is checked for compatibility with the system through matching the system planar ID and processor model/submodel values to the boot record values. For disk, this check is done first in the IBL routine 72 and then done again in the IBL boot record. The first check (in the IBL routine) is done to make sure the boot record is compatible with the system; the second check (in the boot record) is done to ensure a compatible ROM passed control to the boot record. Notice that the check done in the disk boot record will never fail for a compatible ROM since the IBL routine will have already checked the compatibility. In contrast, the compatibility check is not done for diskette. The planar/processor compatibility is checked only during diskette boot record execution. This method allows future modifications in loading a new BIOS image from a reference diskette.

In view of the description of the IBL routine of Fig. 6A, the explanation will now proceed to a comprehensive and full understanding of the validity tests discussed above. Referring to Fig. 6B, there is shown a detailed flowchart of step 152 of Fig. 6A, to determine if a valid master boot record is on drive C. The process begins by obtaining the drive parameters to enable the IBL routine to access drive C, step 200. An IBL load location is set to the last three sectors from the disk (the last three sectors normally contain the master boot record), step 202. A load count indicating the number of attempts to read a master boot record from disk is set to 1, step 204. Three sectors are read from disk at the IBL load location, step 206. Any disk drive errors are detected and if a disk drive read error occurs it is reported, steps 208-210. The process then returns with an error indication, steps 212-214.

Referring back to step 208, if no drive error occurs, the disk record is scanned for the master boot record signature, step 216. The boot record signature, such as the characters "ABC", are compared to the first three bytes of the disk record. If the disk record does have a valid boot record signature (characters "ABC") and the checksum computed from the disk record loaded into memory equals the boot record checksum, the disk record is indicated as being a valid boot record with no errors, step 218. The process then returns, step 214.

Referring back to step 216, if the boot record signature or checksum is invalid, the load count is incremented by 1, step 220. The load count is then compared to a predetermined constant such as 99, step 222. If 99 attempts to read a boot record have resulted in failure, an error is indicated and the process returns, steps 224, 212 and 214. If less than 99 attempts to read a boot record have occurred, the IBL load location is decremented by one and three new sectors are read from the new load location, steps 226 and 206. Thus if a valid IBL boot record cannot be loaded from the last 99 sectors (equivalent to 33 copies) then an error condition is set and control returns to the IBL routine.

Referring now to Fig. 6C, there is shown a detailed flow diagram for loading the master boot record from diskette on drive A. First, the diskette drive parameters to access drive A are retrieved, step 230. The IBL load location is set to the last 3 sectors on diskette (cylinder, head and sector format), step 232. The last 3 sectors are read, step 234. If a diskette drive error is detected an error is indicated, steps 236-238. An error condition is set and control is returned to the IBL routine, steps 240-242.

Referring back to step 236, if no drive error is detected, the diskette record is checked for boot record signature and the checksum is calculated, step 244. If the boot record signature is missing or checksum is invalid, an error is indicated and control

returned to the IBL routine, steps 244, 246, 240 and 242. If a valid boot record signature and valid checksum are detected an indication is set and control is returned to the IBL routine, steps 248 and 242. It is noted that in a diskette load, the IBL routine does not search through the media as in the fixed disk load. Therefore, in a diskette load, the IBL media must be stored in a specific location of the diskette.

Finally, Fig. 6D shows how the IBL routines tests for system planar and processor compatibility and for a proper system configuration. The master boot record is checked for compatibility with the system planar by comparing the boot record planar ID value to the system planar ID read by the system processor, step 260. If the system planar ID does not match the boot record planar ID value, this indicates this master boot record is not compatible with this planar. An error is indicated and control return to the IBL routine, steps 262, 264, and 266.

If the master boot record is compatible with the planar, the master boot record is checked for compatibility with the processor, step 268. The boot record model value and submodel value are compared to the model value and submodel value stored in ROM respectively. A mismatch indicates a new processor has probably been inserted and this boot record is not compatible with the new processor. An error is indicated and control returned to the IBL routine, steps 270, 264 and 266. If the master boot record is compatible with the planar and processor, the process checks to determine if NVRAM is reliable, step 272. If NVRAM is unreliable, an error is indicated and control returned to the IBL routine, steps 274 and 266. If NVRAM is reliable, the system configuration is checked, step 276. A change in system configuration is indicated if the model and submodel values stored in NVRAM do not match the model and submodel values stored in ROM. Note that this last comparison will only indicate a configuration error. If a configuration error is indicated, an error is generated for the user. This error

notifies the user that the configuration of the system has changed since the last time SET Configuration was run. The user is notified of the changed configuration and control passed back to the IBL routine steps 278, 264, and 266. This error is not fatal itself, but notifies the user that SET Configuration (configuration program) must be executed. Referring back to step 276, if the system model/submodel values match, an indication of compabability is set and the routine returns, steps 276, 274 and 266. Thus, the compatibility between the master boot record and the system are tested along with determining if the system configuration has been modified.

After the IBL routine loads the master boot record into RAM, it transfers control to the MBR code starting address. Referring to Fig. 7, the executable code segment of the master boot record first verifies the boot record pattern to the ROM pattern, step 300. If the pattern in the master boot record does not match the pattern in ROM, an error is generated and the system halts, steps 302 and 305. The check for equality between ROM and boot record patterns ensures that the master boot record loaded from either the disk or diskette is compatible with the ROM on the planar board. Referring back to step 300, if the pattern in ROM matches the pattern in the boot record, the MBR code compares the system planar ID value, model and submodel value against the corresponding master boot record values, step 304. This process was discussed in greater detail with respect to Fig. 6D. If the values don't match, the master boot record is not compatible with the system planar and processor, or the system configuration has changed, and an error is generated, step 306. The system then halts, step 305.

Referring back to step 304, if the system planar ID value, model and submodel values match the corresponding master boot record values, the MBR code loads the BIOS image from the selected media into the system RAM, step 308. If a media load error occurs in reading the data, step 310, an error is generated and the system

halts, steps 312 and 305. Referring back to step 310, if no media load error occurs, a checksum is calculated for the BIOS image in memory, step 314. If the checksum is invalid an error is generated and the system halts, steps 318 and 305. Referring back to step 316, if the checksum is valid, the system partition pointers are saved, step 320, and the system processor is vectored to POST Stage II to begin loading the system, step 322.

Thus, there has been shown a method and apparatus for loading BIOS from a direct access storage device. Before BIOS is loaded, the BIOS image on the direct access storage device is checked for compatibility with the system. A further test includes checking that the system configuration is proper. Based upon these tests the BIOS image is loaded into RAM to be executed.

While the invention has been illustrated in connection with a prefefred embodiment, it should be understood that many variations will occur to those of ordinary skill in the art, and that the scope of the invention is defined only by the claims appended hereto and equivalent.

CLAIMS

1. A computer system (10) comprising: a system processor (26) electrically coupled to a random access memory (32);

a direct access storage device (62,66) electrically coupled to the system processor (26), the direct access storage device (62,66) being capable of storing a plurality of data records;

a read only memory (36) being electrically coupled to the system processor (26);

characterised in that the system (10) further comprises:

a master boot record included in the direct access storage device (62,66), the master boot record having an executable code segment (120);

a first portion of BIOS included in the read only memory (36), the first portion of BIOS initializing the system (10) and the direct access storage device (62,66) to load the master boot record into random access memory (32); and

a remaining portion of BIOS included in the direct access storage device (62,66), wherein the first portion of BIOS transfers control to the executable code segment (120) of the master boot record in order to effect the loading of the remaining portion of BIOS into the random access memory (32), the remaining portion of BIOS initializing the rest of the system (10) in order to load in an operating system to begin operation of the system (10).

2. A computer system (10) as claimed in claim 1, wherein the direct access storage device comprises a fixed disk (62).

3. A computer system (10) as claimed in claim 1, wherein the direct access storage device comprises a diskette (66).

4. A computer system (10) as claimed in claim 1, wherein the master boot record further includes a data segment (122-138), the data

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segment (122-138) representing a hardware configuration of the system (10) which is compatible with the master boot record,

and wherein the read only memory (36) includes data representing a hardware configuration of the system processor (26), wherein before the remaining portion of BIOS is loaded into random access memory (32), the first portion of BIOS compares the hardware configuration data from the master boot record with the hardware configuration data from the read only memory (36) to verify the master boot record is compatible with the system processor (26).

5. A computer system (10) as claimed in claim 4, wherein the data segment (122-138) of the master boot record includes a value (134) representing a system planar (24) which is compatible with the master boot record,

and wherein the system planar (24) further includes a means for uniquely identifying the system planar (24) in order to verify that the master boot record is compatible to the system planar (24).

6. A computer system (10) as claimed in claim 4, wherein the hardware configuration data on the master boot record includes model and submodel values (136), wherein the model value identifies a system processor (26) which is compatible with the master boot record and the submodel value represent an Input/Output configuration of a system planar (24) which is compatible with the master boot record,

and wherein the read only memory (36) includes a corresponding model value identifying the system processor (26) and submodel value representing the Input/Output configuration of the system planar (24), wherein the model value and submodel value of the master boot record are compared to the corresponding model and submodel values of the read only memory (36) respectively, in order to verify that the master boot record is compatible with the system processor (26) and the I/O configuration of the system planar.

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7. A computer system (10) as claimed in claim 5 wherein the first portion of BIOS generates a first error to indicate the master boot record is not compatible with the system hardware.

8. A computer system (10) as claimed in claim 1 further comprising a nonvolatile random access memory (58) electrically coupled to the system processor (26), the nonvolatile random access memory (58) including data representing the system configuration, the data being updated when the configuration of the system (10) is changed, wherein the first portion of BIOS compares the data in the nonvolatile random access memory (58) to corresponding data in the read only memory (36) to determine if the configuration of the system (10) has changed.

9. A computer system (10) as claimed in claim 8, wherein the first portion of BIOS generates a second error to indicate that the configuration of the system (10) has changed.

10. A computer system (10) as claimed in claim 1, wherein the master boot record includes an identifying means (122) to identity the record in order to distinguish the master boot record from other records included on the direct access storage device (62,66).

11. A computer system (10) as claimed in claim 10, wherein the identifying means (122) comprises a predetermined character code.

12. A computer system (10) as claimed in claim 11, wherein the predetermined code is prefatory to the code segment of the master boot record.

13. A computer system (10) as claimed in claim 10, wherein the master boot record includes a checksum value (132) to verify the validity of the master boot record when loaded into the random access memory (32).

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14. A computer system (10) as claimed in claim 1 wherein the remaining portion of BIOS includes a checksum value (132) to verify the validity of the remaining portion of BIOS when loaded into the random access memory (32).

15. A computer system (10) as claimed in claim 1, wherein the master boot record includes a predetermined pattern (124), and further wherein the read only memory (36) includes a corresponding predetermined pattern (124) in order to verify that the first portion of BIOS is included within a predefined read only memory (36).

16. A computer system (10) as claimed in claim 15, wherein the executable code segment (120) generates a third error to indicate that the read only memory (36) is not compatible with the master boot record.

17. In or for a computer system (10) having a system processor (26) being electrically coupled to a random access memory (32), BIOS loading apparatus comprising:

a direct access storage device (62,66) being electrically coupled to the system processor (26), the direct access storage device (62,66) being capable of storing a plurality of data records;

a read only memory (36) being electrically coupled to the system processor (26);

a first portion of BIOS being included in the read only memory (36); and

a remaining portion of BIOS being included in the direct access storage device (62,66), wherein the first portion of BIOS initializes the system processor (26) and direct storage device (62,66) to effect loading of the remaining portion of BIOS into random access memory (32), the remaining portion of BIOS effectively superseding the first portion of BIOS to assist in the operation of the system (10).

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18. A method for loading BIOS from a direct access storage device (62,66) of a computer system (10), the computer system (10) having a system processor (26) electrically coupled to a system planar (24), the planar further being electrically coupled to a random access memory (32), a read only memory (36), and the direct access storage device (62,66), the method comprising the steps of:

(a) initializing the system (10) with a first portion of BIOS resident in the read only memory (36);

(b) initializing with the first portion of BIOS the direct access storage device (62,66), the direct access storage device (62,66) further having a master boot record and the remaining BIOS;

(c) loading with the first portion of BIOS the master boot record into random access memory (32), the master boot record including a data segment (122-138) and an executable code segment (120), the data segment (122-138) having data representing the hardware of the system (10) for which the remaining BIOS is compatible;

(d) verifying the compatibility of the master boot record with the system hardware by comparing the data representing the system hardware to corresponding compatibility data stored in the read only memory (36); and

(e) executing the code segment of the master boot record to load the remaining BIOS into the random access memory (32); and

(f) passing control to the remaining BIOS once the remaining BIOS is loaded into random access memory (32);

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ABSTRACT

An apparatus and method for loading BIOS stored on a direct access storage device (62,66) into a personal computer system (10). The personal computer system (10) comprises a system processor (26), a system planar (24), a random access main memory, a read only memory (36), and at least one direct access storage device (62,66). The read only memory (36) includes a first portion of BIOS and data representing the type of system processor (26) and system planar (24) I/O configuration. The first portion of BIOS initializes the system (10) and the direct access storage device (62,66) to read in a master boot record into the system (10) from the direct access storage device (62,66). The master boot record includes a data segment (122-138) and an executable code segment (120). The data segment (122-138) includes data representing system hardware and a system (10) configuration which is supported by the master boot record. The first BIOS portion confirms the master boot record is compatible with the system hardware by verifying that the data from the data segment (122-138) of the master boot record agrees with the system processor (26), system planar (24), and planar I/O configuration. If the master boot record is compatible with the system hardware, the first BIOS portion vectors the system processor (26) to execute the executable code segment (120) of the master boot record. The executable code segment (120) confirms that the system configuration has not changed and loads in the remaining BIOS portion from the direct access storage device (62,66) into random access memory (32). The executable code segment (120) then verifies the authenticity of the remaining BIOS portion and vectors the system processor (26) to begin executing the BIOS now in random access memory (32). BIOS executing in random access memory (32) then boots up the operating system to begin operation of the personal computer system (10).

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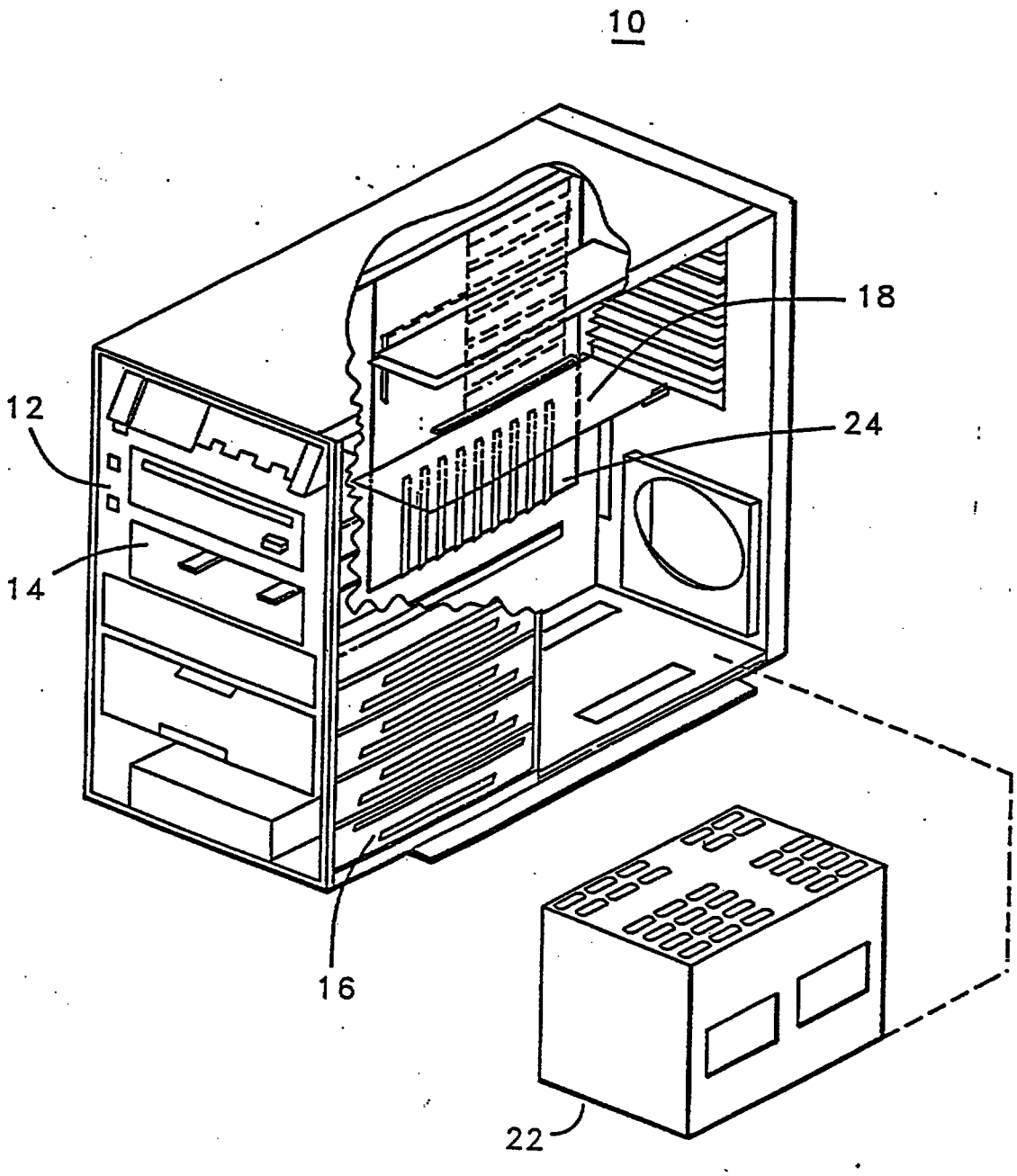


FIG. 1

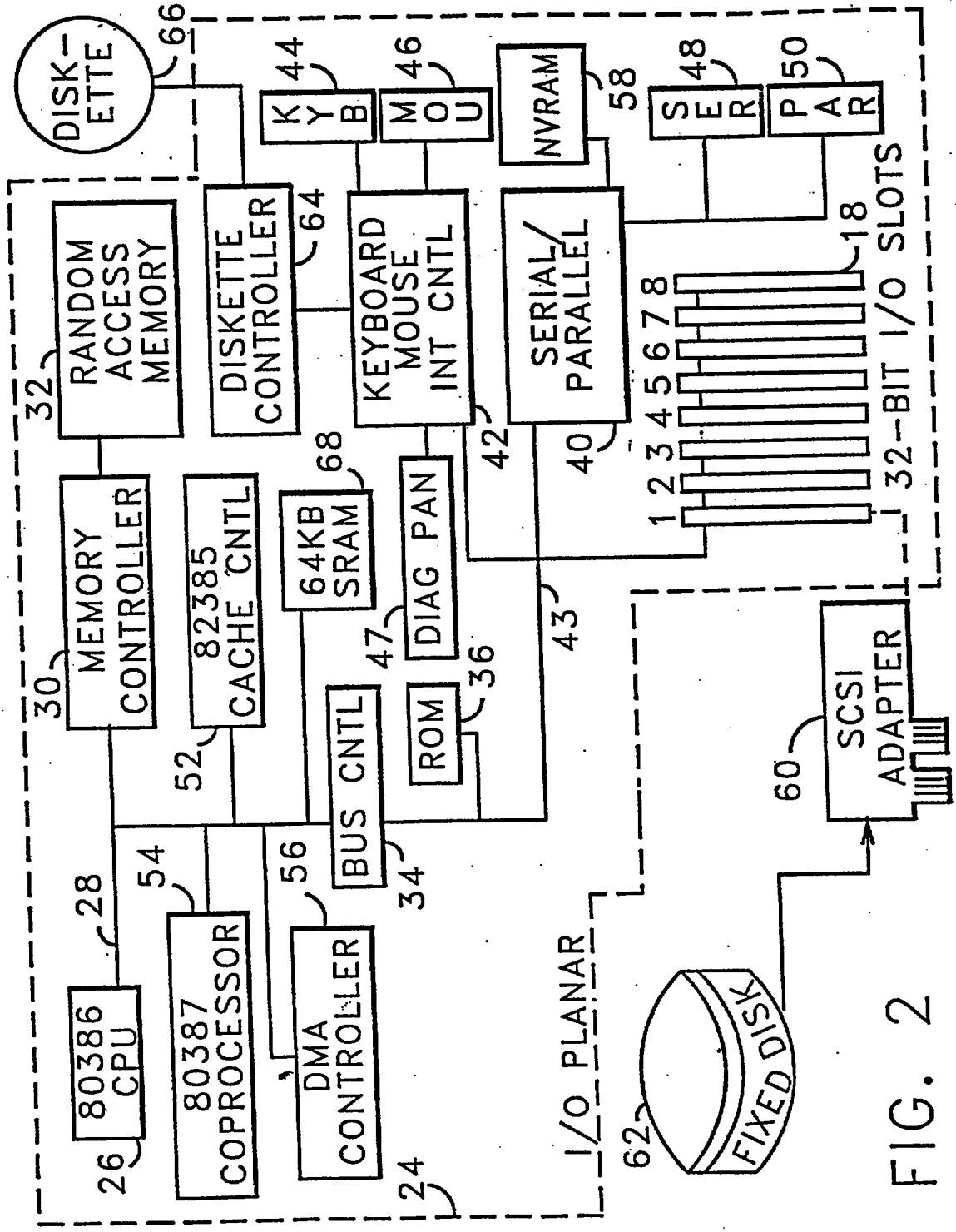

DISK-ETTE
66
K Y B
44
M O U
46
NVRAM
58
S E R
48
P A R
50
RANDOM ACCESS MEMORY
32
DISKETTE CONTROLLER
64
KEYBOARD MOUSE INT CNTL
SERIAL/ PARALLEL
18
1 2 3 4 5 6 7 8
32-BIT I/O SLOTS
42
40
MEMORY CONTROLLER
30
82385 CACHE CNTL
52
64KB SRAM
68
DIAG PAN
47
43
BUS CNTL
34
ROM
36
SCSI ADAPTER
60
80386 CPU
26
28
80387 COPROCESSOR
54
DMA CONTROLLER
56
24
I/O PLANAR
62
FIXED DISK

FIG. 2

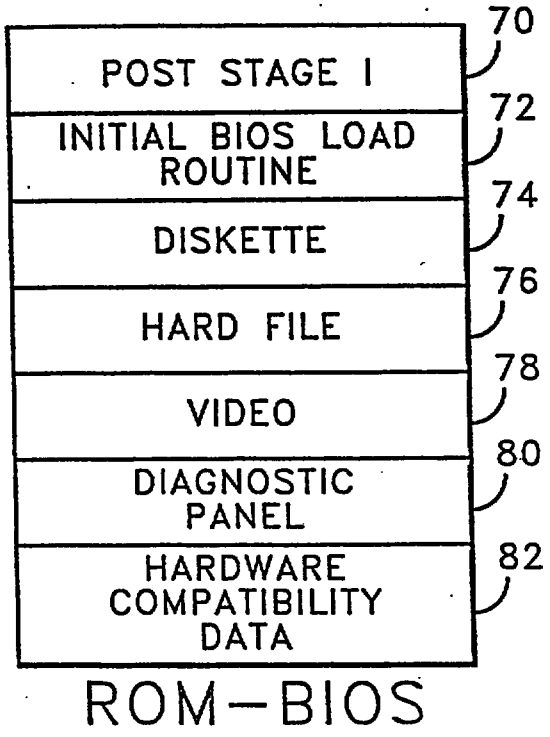

POST STAGE I
70
INITIAL BIOS LOAD ROUTINE
72
DISKETTE
74
HARD FILE
76
VIDEO
78
DIAGNOSTIC PANEL
80
HARDWARE COMPATIBILITY DATA
82
ROM-BIOS

FIG. 3

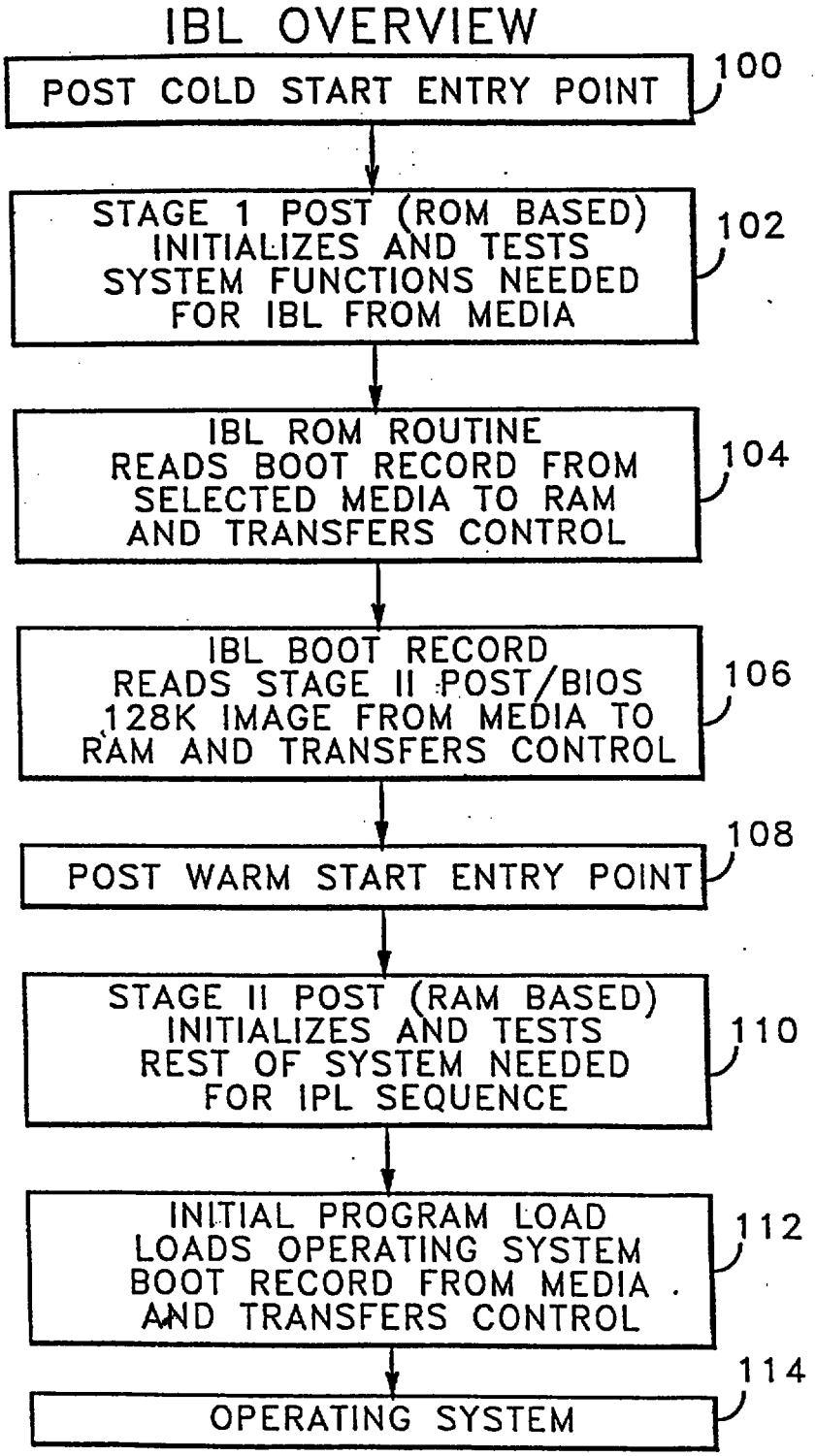

IBL OVERVIEW
POST COLD START ENTRY POINT
100
STAGE 1 POST (ROM BASED) INITIALIZES AND TESTS SYSTEM FUNCTIONS NEEDED FOR IBL FROM MEDIA
102
IBL ROM ROUTINE READS BOOT RECORD FROM SELECTED MEDIA TO RAM AND TRANSFERS CONTROL
104
IBL BOOT RECORD READS STAGE II POST/BIOS 128K IMAGE FROM MEDIA TO RAM AND TRANSFERS CONTROL
106
POST WARM START ENTRY POINT
108
STAGE II POST (RAM BASED) INITIALIZES AND TESTS REST OF SYSTEM NEEDED FOR IPL SEQUENCE
110
INITIAL PROGRAM LOAD LOADS OPERATING SYSTEM BOOT RECORD FROM MEDIA AND TRANSFERS CONTROL
112
OPERATING SYSTEM
114

FIG. 4

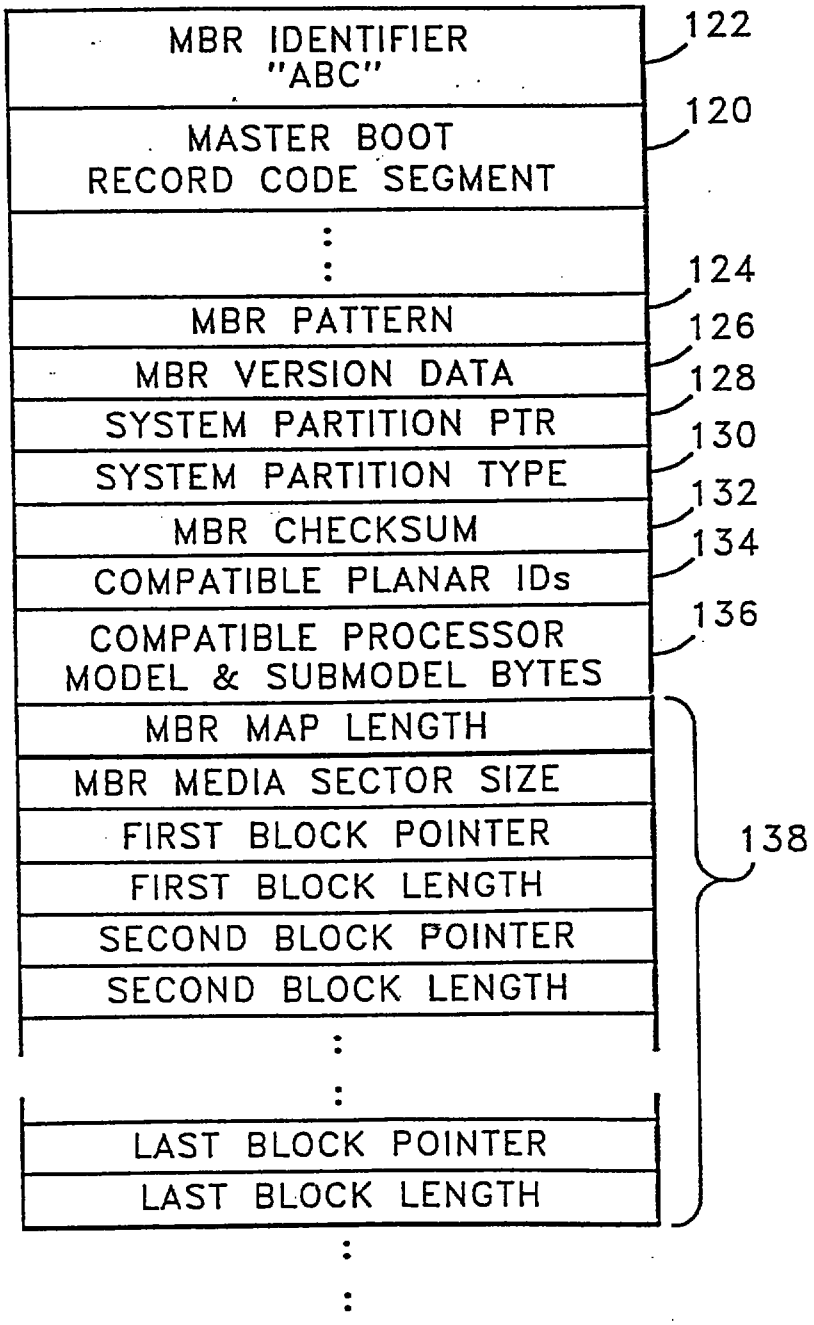

MBR IDENTIFIER "ABC"
122
MASTER BOOT RECORD CODE SEGMENT
120
124
MBR PATTERN
126
MBR VERSION DATA
128
SYSTEM PARTITION PTR
130
SYSTEM PARTITION TYPE
132
MBR CHECKSUM
134
COMPATIBLE PLANAR IDs
136
COMPATIBLE PROCESSOR MODEL & SUBMODEL BYTES
MBR MAP LENGTH
MBR MEDIA SECTOR SIZE
FIRST BLOCK POINTER
FIRST BLOCK LENGTH
SECOND BLOCK POINTER
SECOND BLOCK LENGTH
LAST BLOCK POINTER
LAST BLOCK LENGTH
138

FIG. 5

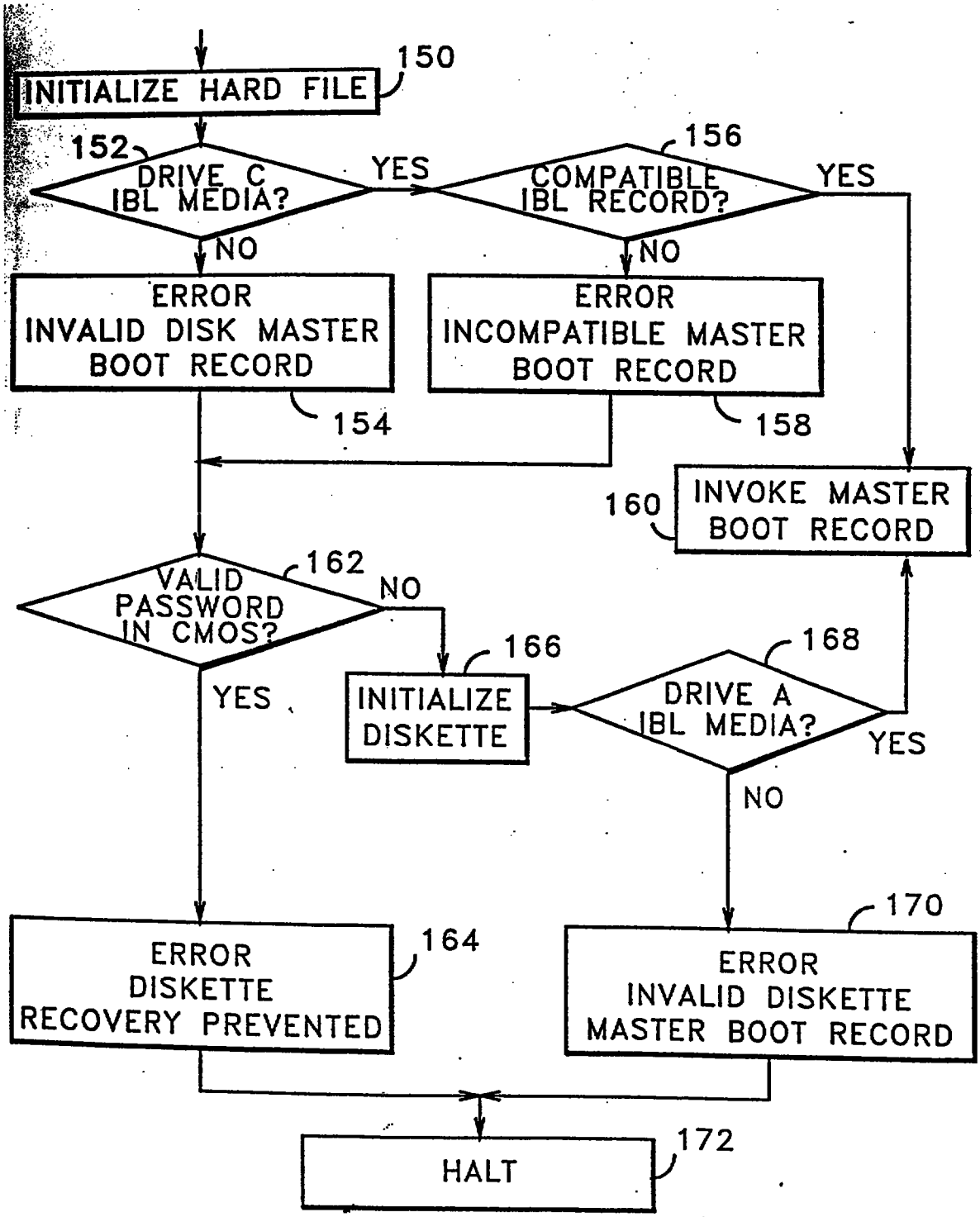

INITIALIZE HARD FILE
150
152
DRIVE C IBL MEDIA?
YES
156
COMPATIBLE IBL RECORD?
YES
NO
NO
ERROR INVALID DISK MASTER BOOT RECORD
154
ERROR INCOMPATIBLE MASTER BOOT RECORD
158
160
INVOKE MASTER BOOT RECORD
162
VALID PASSWORD IN CMOS?
NO
YES
166
INITIALIZE DISKETTE
168
DRIVE A IBL MEDIA?
YES
NO
ERROR DISKETTE RECOVERY PREVENTED
164
170
ERROR INVALID DISKETTE MASTER BOOT RECORD
HALT
172

FIG. 6A

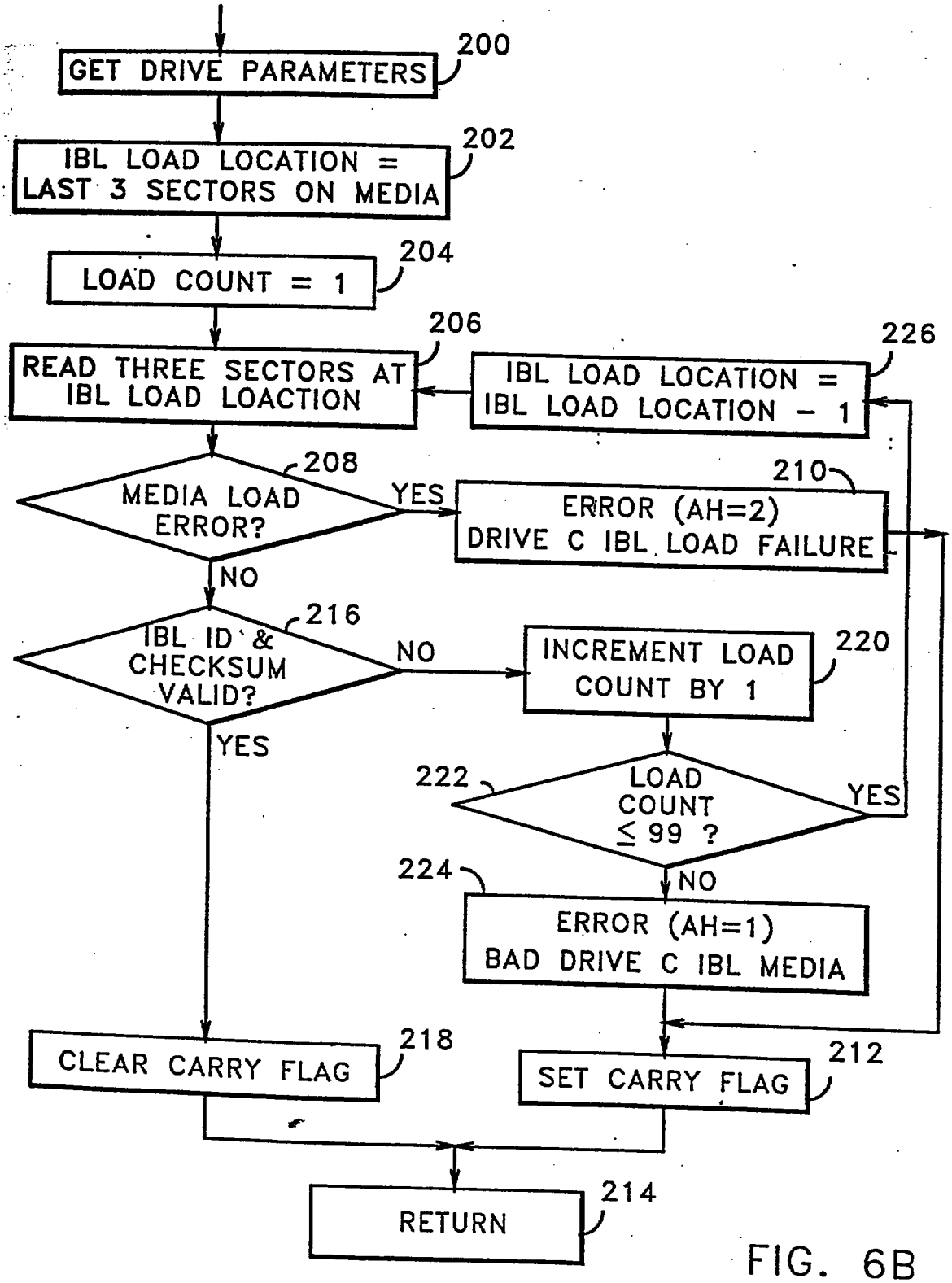

GET DRIVE PARAMETERS
200
IBL LOAD LOCATION = LAST 3 SECTORS ON MEDIA
202
LOAD COUNT = 1
204
READ THREE SECTORS AT IBL LOAD LOACTION
206
IBL LOAD LOCATION = IBL LOAD LOCATION - 1
226
MEDIA LOAD ERROR?
208
YES
ERROR (AH=2) DRIVE C IBL LOAD FAILURE
210
NO
IBL ID & CHECKSUM VALID?
216
NO
INCREMENT LOAD COUNT BY 1
220
YES
LOAD COUNT ≤ 99 ?
222
YES
NO
ERROR (AH=1) BAD DRIVE C IBL MEDIA
224
CLEAR CARRY FLAG
218
SET CARRY FLAG
212
RETURN
214

FIG. 6B

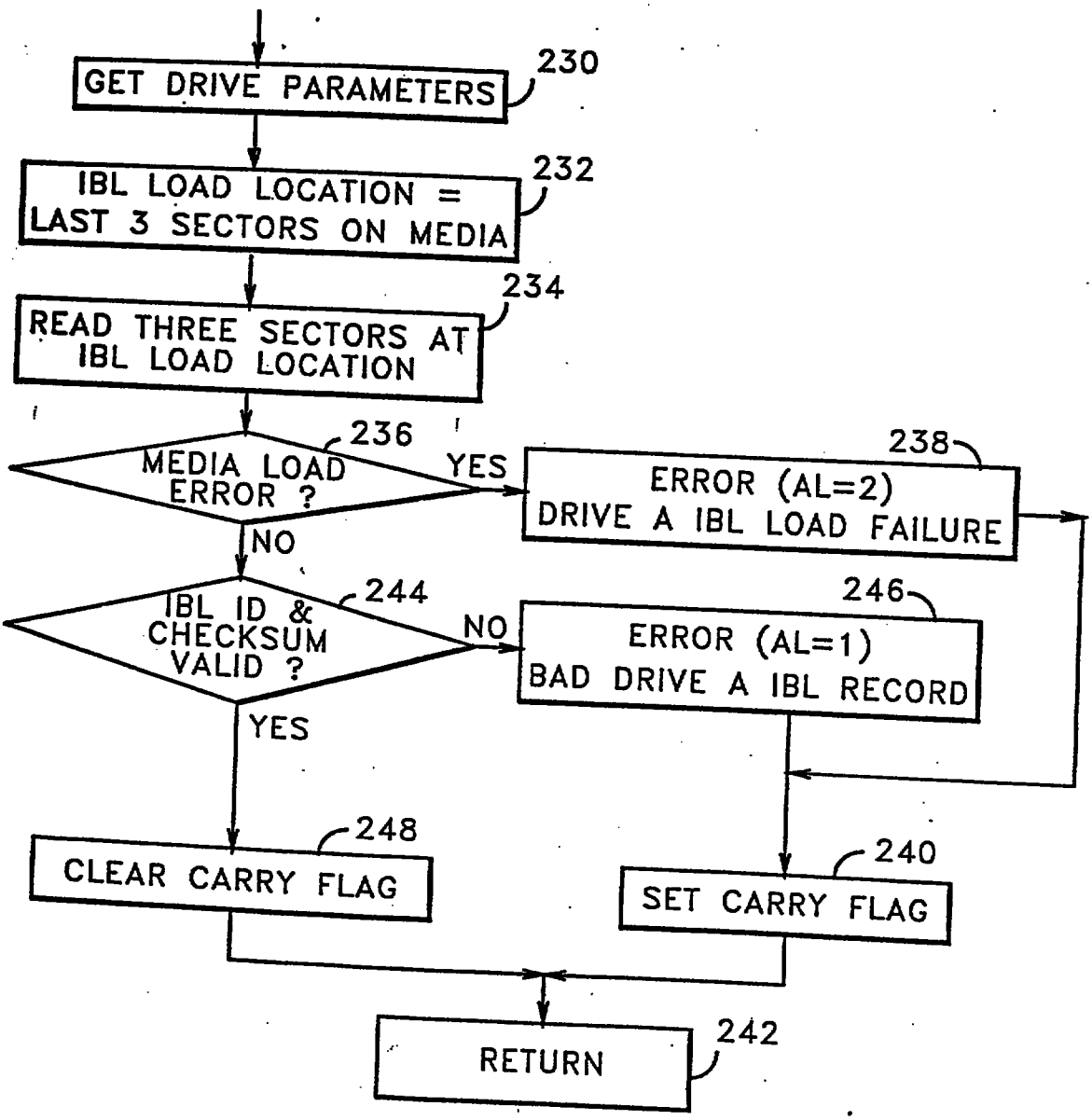

GET DRIVE PARAMETERS
230
IBL LOAD LOCATION = LAST 3 SECTORS ON MEDIA
232
READ THREE SECTORS AT IBL LOAD LOCATION
234
MEDIA LOAD ERROR ?
236
YES
ERROR (AL=2) DRIVE A IBL LOAD FAILURE
238
NO
IBL ID & CHECKSUM VALID ?
244
NO
ERROR (AL=1) BAD DRIVE A IBL RECORD
246
YES
CLEAR CARRY FLAG
248
SET CARRY FLAG
240
RETURN
242

FIG. 6C

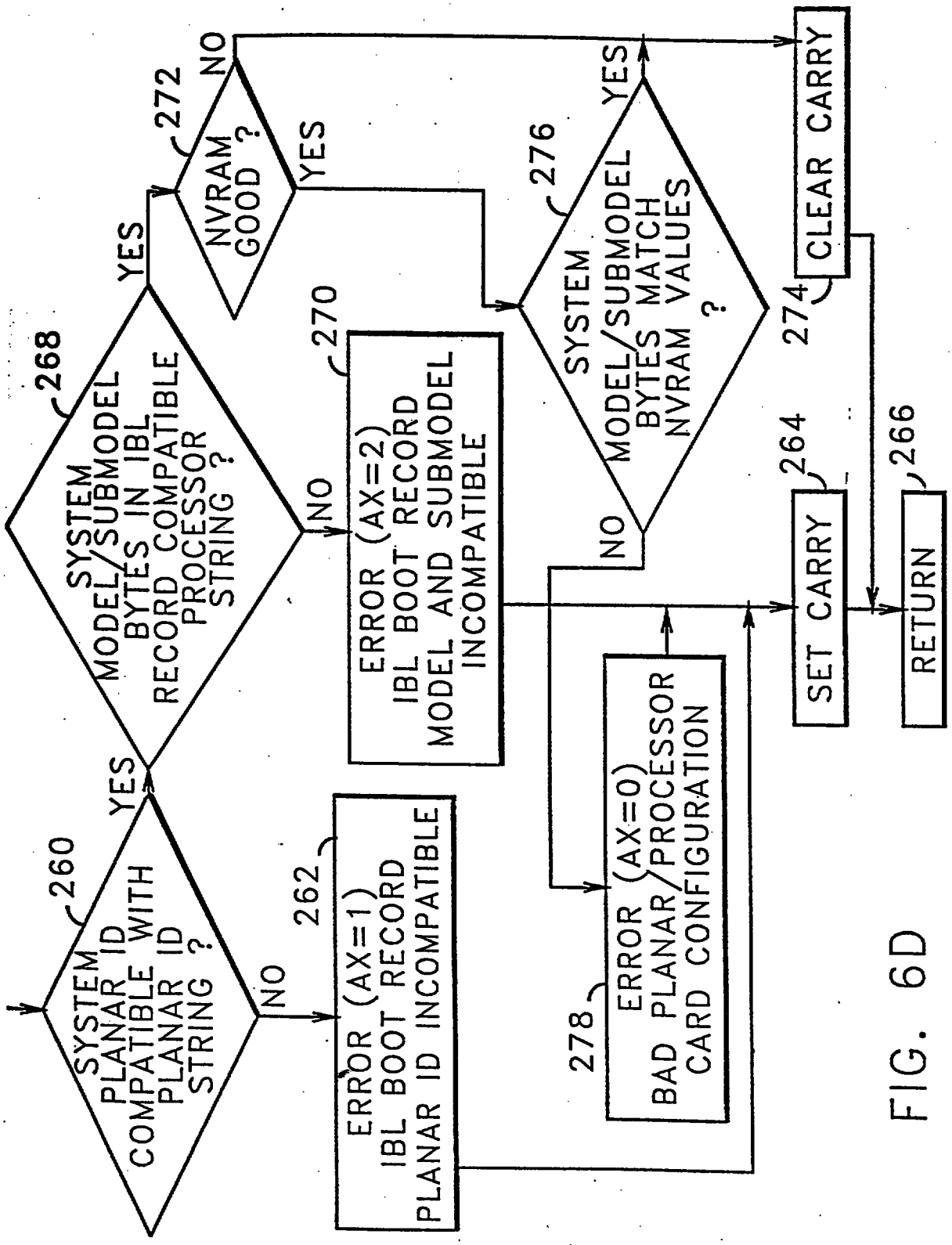

260
SYSTEM PLANAR ID COMPATIBLE WITH PLANAR ID STRING ?
YES
NO
262
ERROR (AX=1) IBL BOOT RECORD PLANAR ID INCOMPATIBLE
268
SYSTEM MODEL/SUBMODEL BYTES IN IBL RECORD COMPATIBLE PROCESSOR STRING ?
YES
NO
270
ERROR (AX=2) IBL BOOT RECORD MODEL AND SUBMODEL INCOMPATIBLE
272
NVRAM GOOD ?
YES
NO
276
SYSTEM MODEL/SUBMODEL BYTES MATCH NVRAM VALUES ?
YES
NO
278
ERROR (AX=0) BAD PLANAR/PROCESSOR CARD CONFIGURATION
274
CLEAR CARRY
264
SET CARRY
266
RETURN

FIG. 6D

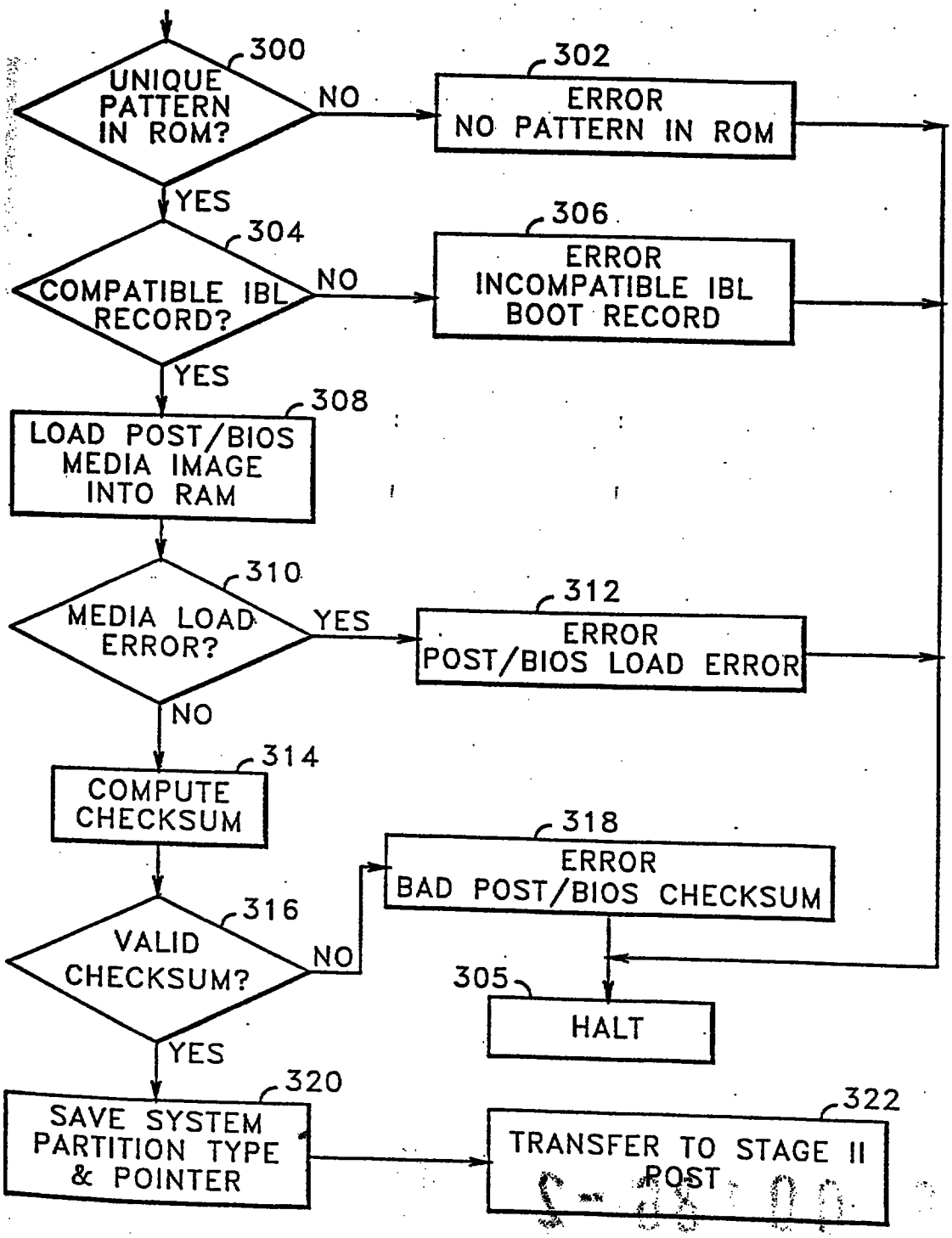

300
UNIQUE PATTERN IN ROM?
NO
302
ERROR NO PATTERN IN ROM
YES
304
COMPATIBLE IBL RECORD?
NO
306
ERROR INCOMPATIBLE IBL BOOT RECORD
YES
308
LOAD POST/BIOS MEDIA IMAGE INTO RAM
310
MEDIA LOAD ERROR?
YES
312
ERROR POST/BIOS LOAD ERROR
NO
314
COMPUTE CHECKSUM
318
ERROR BAD POST/BIOS CHECKSUM
316
VALID CHECKSUM?
NO
305
HALT
YES
320
SAVE SYSTEM PARTITION TYPE & POINTER
322
TRANSFER TO STAGE II POST

FIG. 7

9600186-2
IPOS.

REPLACEMENT SHEET
22 MAY 1996

COMPUTER SYSTEM

ABSTRACT

An apparatus and method for loading BIOS stored on a direct access storage device (62, 66) into a personal computer system (10). The personal computer system (10) comprises a system processor (26), a system planar (24), a random access main memory, a read only memory (36), and at least one direct access storage device (62, 66). The read only memory (36) includes a first portion of BIOS and data representing the type of system processor (26) and system planar (24) I/O configuration. The first portion of BIOS initializes the system (10) and the direct access storage device (62, 66) to read in a master boot record into the system (10) from the direct access storage device (62, 66). The master boot record includes a data segment (122-138) and an executable code segment (120). The data segment (122-138) includes data representing system hardware and a system (10) configuration which is supported by the master boot record.

Fig. 2

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IPOS.

bytes of ROM were resident on the planar board. Fortunately, the system could be expanded to 96K bytes of ROM. Unfortunately, because of system constraints, this turned out to be the maximum capacity available for BIOS. Luckily, even with the addition of ABIOS, ABIOS and CBIOS could still squeeze into 96K of ROM. However, only a small percentage of the 96K ROM area remained available for expansion. With the addition of future I/O devices, CBIOS and ABIOS will eventually run out of ROM space. Thus, new I/O technology will not be able to be easily integrated within CBIOS and ABIOS.

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Due to these problems, plus the desire to make modification in Family II BIOS as late as possible in the development cycle, it has become necessary to off load portions of BIOS from the ROM. Since marketability and consumer acceptance of personal computer systems appear to require the ability to add new I/O devised and to minimize cost, it should be appreciated that easy modification of Family II models' BIOS is a substantial factor in achieving success in accordance with this invention. Thus, there exists a need for developing a method and apparatus which permits portions of BIOS to be stored on a direct access storage device such as a fixed disk or on the diskette drive. These portions can then be easily modified and loaded into the personal computer system when required.

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SUMMARY OF THE INVENTION

It is an object of the present invention to ameliorate one or more disadvantages of the prior art.

According to one aspect of the present invention there is provided an apparatus for loading an operational interface into a personal computer system, the personal computer system including a system processor and a random access memory electrically coupled thereto, said apparatus comprising: a direct access storage device being electrically coupled to the system processor, said direct access storage device being capable of storing a plurality of data records; a master boot record stored on the direct access storage device, said master boot recording including an executable code segment; a read only memory being electrically coupled to the system processor; a first portion of the operational interface stored in the read only memory starting at a particular address, said first portion of the operational interface initializing the system and the direct access storage device to load in said master boot record into random access memory; and a remaining portion of the operational interface stored on the direct access storage device, wherein the first portion of the operational interface transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of the operational interface into the random access memory, said remaining portion of the operational interface being stored starting at said particular address and superseding the first portion of the operational interface and initializing the rest of the personal computer system in order to load in an operating system to begin operation of the personal computer system.

According to another aspect of the present invention there is provided a personal computer system comprising: a system processor; a random access memory being the main memory and electrically coupled to the system processor; a system planar board having a plurality of I/O slots being electrically coupled to the system processor, a direct access storage device being electrically coupled to the system processor, the direct access storage device capable of storing a plurality of data records; a master boot record included in the direct access storage device, the master boot record having a data segment and an executable code segment, the data segment representing a hardware configuration of the personal computer system which is compatible with said master boot record; a read only memory being electrically coupled to the system processor, the read only memory having data representing a hardware configuration of the system; a first portion of an operational interface being included in the read only memory, said first portion of the operational interface initializing the system and the direct access storage device to load in said master boot record, said first portion of the operational interface further comparing the hardware configuration data from the master boot record to the hardware configuration data of the read only memory to verify the compatibility of the master boot record with the system processor; a remaining portion of the operational interface being included in the direct access storage device, wherein after verifying the compatibility of the master boot record with the system processor, the first portion of the operational interface transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of the operational interface into the random access memory, said remaining portion of the operational interface superseding said first portion of the operational interface.

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According to still another aspect of the present invention there is provided an apparatus for loading an operational interface into a personal computer system, the personal computer system having a system processor being electrically coupled to a random access memory, said apparatus comprising: a direct access storage device being electrically coupled to the system processor, the direct access storage device being capable of storing a plurality of data records; a read only memory being electrically coupled to the system processor; a first portion of the operational interface being included in the read only memory; and remaining portion of the operational interface being included in the direct access storage device, wherein the first portion of the operational interface initializes the system processor and direct storage device to effect load the remaining portion of the operational interface into random access memory, said remaining portion of the operational interface effectively superseding the first portion of the operational interface to assist in the operation of the system.

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According to yet another aspect of the present invention there is provided a method for loading an operational interface from a direct access storage device of a personal computer system, the personal computer system having a system processor electrically coupled to a system planar, the planar further being electrically coupled to a random access memory, a read only memory, and the direct access storage device, said method comprising the steps of: (a) initializing the system with a first portion of the operational interface resident in the read only memory; (b) initializing with the first portion of the operational interface the direct access storage device, the direct access storage device further having a master boot record and the remaining portion of the operational interface; (c) loading with the first portion of the operational interface the master boot record into random access memory, the master boot record including a data segment and an executable code segment, the data segment having data representing the hardware of the system for which the remaining portion of the operational interface is compatible; (d) verifying the compatibility of the master boot record with the system hardware by comparing the data representing the system hardware to corresponding compatibility data stored in the read only memory; and (e) executing the code segment of the master boot record to load the remaining portion of the operational interface into the random access memory; and (f) passing control to the remaining portion of the operational interface once it is loaded into random access memory.

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DESCRIPTION OF THE PREFERRED EMBODIMENT(S)

An embodiment of the present invention will now be described with reference to the accompanying drawings in which:

Fig. 1 illustrates a cut away view of a personal computer system showing a system planar board connected to a plurality of direct access storage devices;

Fig. 2 shows a system block diagram for the personal computer system of Fig. 1;

Fig. 3 is a memory map for the ROM BIOS included on the planar board;

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Fig. 4 is a flowchart describing the overall process for loading a BIOS image from a direct access storage device;

Fig. 5 illustrates the record format for the master boot record;

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* C L M S *

CLAIMS

1. An apparatus for loading an operational interface into a personal computer system, the personal computer system including a system processor and a random access memory electrically coupled thereto, said apparatus comprising:

a direct access storage device being electrically coupled to the system processor, said direct access storage device being capable of storing a plurality of data records;

a master boot record stored on the direct access storage device, said master boot recording including an executable code segment;

a read only memory being electrically coupled to the system processor;

a first portion of the operational interface stored in the read only memory starting at a particular address, said first portion of the operational interface initializing the system and the direct access storage device to load in said master boot record into random access memory; and

a remaining portion of the operational interface stored on the direct access storage device, wherein the first portion of the operational interface transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of the operational interface into the random access memory, said remaining portion of the operational interface being stored starting at said particular address and superseding the first portion of the operational interface and initializing the rest of the personal computer system in order to load in an operating system to begin operation of the personal computer system.

2. The apparatus of claim 1, wherein the direct access storage device comprises a fixed disk.

3. The apparatus of claim 1, wherein the direct access storage device comprises a diskette.

4. The apparatus of claim 1, wherein the master boot record further includes a data segment, the data segment representing a hardware configuration of the personal computer system which is compatible with said master boot record, and further wherein the read only memory includes data representing a hardware configuration of the system processor, wherein before said remaining portion of the operational interface is loaded into random access memory, said first portion of the operational interface compares the hardware configuration data from the master boot record with the hardware configuration data from the read only memory to verify the master boot record is compatible with the system processor.

5. The apparatus of claim 4, wherein the data segment of the master boot record includes a value representing a system planar which is compatible with the master boot record and further wherein the system planar further includes a means for uniquely identifying the system planar in order to verify that the master boot record is compatible to the system planar.

6. The apparatus of claim 4, wherein the hardware configuration data on the master boot record includes a model value and a submodel value, wherein the model value identifies a system processor which is compatible with said master boot record and the submodel value

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represent an I/O configuration of a system planar which is compatible with the master boot record, and further wherein said read only memory includes a corresponding model value identifying the system processor and submodel value representing the I/O configuration of the system planar, wherein said model value and submodel value of the master boot record are compared to the corresponding model and submodel values of the read only memory respectively, in order to verify that the master boot record is compatible with the system processor and the I/O configuration of the system planar.

7. The apparatus of claim 6, wherein said first portion of the operational interface generates a first error to indicate the master boot record is not compatible with the system hardware.

8. The apparatus of claim 1, wherein the personal computer system further includes a nonvolatile random access memory being electrically coupled to the system processor, said nonvolatile random access memory including data representing the system configuration, said data being updated when the configuration of the system is changed, wherein said first portion of the operational interface compares said data in the nonvolatile random access memory to corresponding data in the read only memory to determine if the configuration of the system has changed.

9. The apparatus of claim 8, wherein said first portion of the operational interface generates a second error to indicate that the system configuration has changed.

10. The apparatus of claim 1, wherein said master boot record includes an identifying means to identify the record in order to distinguish the master boot from other records included on the direct access storage device.

11. The apparatus of claim 10, wherein said identifying means comprises a predetermined character code.

12. The apparatus of claim 11 wherein said predetermined code is prefactory to said code segment of the master boot record.

13. The apparatus of claim 10, wherein said master boot record includes a checksum value to verify the validity of the master boot record when loaded into the random access memory.

14. The apparatus of claim 1, wherein said remaining portion of the operational interface includes a checksum value to verify the validity of the remaining portion of the operational interface when loaded into the random access memory.

15. The apparatus of claim 1, wherein said master boot record includes a predetermined pattern, and further wherein said read only memory includes a corresponding predetermined pattern in order to verify that the first portion of the operational interface is included within a predefined read only memory.

16. The apparatus of claim 15, wherein said executable code segment generates an error to indicate that the read only memory is not compatible with the master boot record.

17. A personal computer system comprising:

a system processor;

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a random access memory being the main memory and electrically coupled to the system processor;

a system planar board having a plurality of I/O slots being electrically coupled to the system processor,

a direct access storage device being electrically coupled to the system processor, the direct access storage device capable of storing a plurality of data records;

a master boot record included in the direct access storage device, the master boot record having a data segment and an executable code segment, the data segment representing a hardware configuration of the personal computer system which is compatible with said master boot record;

a read only memory being electrically coupled to the system processor, the read only memory having data representing a hardware configuration of the system;

a first portion of an operational interface being included in the read only memory, said first portion of the operational interface initializing the system and the direct access storage device to load in said master boot record, said first portion of the operational interface further comparing the hardware configuration data from the master boot record to the hardware configuration data of the read only memory to verify the compatibility of the master boot record with the system processor;

a remaining portion of the operational interface being included in the direct access storage device, wherein after verifying the compatibility of the master boot record with the system processor, the first portion of the operational interface transfers control to the executable code segment of the master boot record in order to effect the loading of the remaining portion of the operational interface into the random access memory, said remaining portion of the operational interface superseding said first portion of the operational interface.

18. The apparatus of claim 17, wherein the data segment of the master boot record includes a value representing a system planar being compatible with the master boot record and further wherein the system planar further includes a means for uniquely identifying the system planar in order to verify the compatibility of the master boot record to the system planar.

19. The apparatus of claim 17, wherein the direct access storage device comprises a fixed disk.

20. The apparatus of claim 17, wherein the hardware configuration data on the master boot record includes a model value and a submodel value, wherein the model value identifies the system processor and the submodel value represent the I/O configuration of the system planar, said model value and submodel value being compared to corresponding values in the read only memory to verify the compatibility of the master boot record to the hardware configuration.

21. The apparatus of claim 17, wherein the personal computer system further includes a nonvolatile random access memory, said nonvolatile random access memory storing values representing the system configuration, said data being updated when the configuration of the

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system is changed, wherein said first portion of the operational interface compares said values in the nonvolatile random access memory to corresponding values in the read only memory to determine if the configuration of the system has changed.

22. An apparatus for loading an operational interface into a personal computer system, the personal computer system having a system processor being electrically coupled to a random access memory, said apparatus comprising:

a direct access storage device being electrically coupled to the system processor, the direct access storage device being capable of storing a plurality of data records;

a read only memory being electrically coupled to the system processor;

a first portion of the operational interface being included in the read only memory; and a remaining portion of the operational interface being included in the direct access storage device, wherein the first portion of the operational interface initializes the system processor and direct storage device to effect load the remaining portion of the operational interface into random access memory, said remaining portion of the operational interface effectively superseding the first portion of the operational interface to assist in the operation of the system.

23. A method for loading an operational interface from a direct access storage device of a personal computer system, the personal computer system having a system processor electrically coupled to a system planar, the planar further being electrically coupled to a random access memory, a read only memory, and the direct access storage device, said method comprising the steps of:

(a) initializing the system with a first portion of the operational interface resident in the read only memory;

(b) initializing with the first portion of the operational interface the direct access storage device, the direct access storage device further having a master boot record and the remaining portion of the operational interface;

(c) loading with the first portion of the operational interface the master boot record into random access memory, the master boot record including a data segment and an executable code segment, the data segment having data representing the hardware of the system for which the remaining portion of the operational interface is compatible;

(d) verifying the compatibility of the master boot record with the system hardware by comparing the data representing the system hardware to corresponding compatibility data stored in the read only memory; and

(e) executing the code segment of the master boot record to load the remaining portion of the operational interface into the random access memory; and

(f) passing control to the remaining portion of the operational interface once it is loaded into random access memory.

24. The method of claim 23, wherein step (d) of verifying further includes the steps of:

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(g) verifying that the master boot record is compatible with the planar by comparing a planar ID accessible by the system processor with a planar ID value stored in the data segment of the master boot record; and

(h) verifying that the master boot record is compatible with the system processor and I/O configuration of the planar by comparing respectively model and submodel values stored in the read only memory with model and submodel values stored in the data segment of the master boot record.

25. The method of claim 23, wherein the system further includes a nonvolatile memory being electrically coupled to the system processor, wherein the nonvolatile memory includes data representing the system configuration, said method further including the step of:

(i) comparing the data in nonvolatile random access memory to the data in read only memory to determine whether the system configuration has changed; and

(j) generating an indication that the system configuration has changed before loading the operational from the direct access storage device.

26. The method of claim 23, wherein step (c) of loading further includes the steps of:

(k) searching through a predetermined number of records on the direct access image device for a master boot record;

(l) identifying the master boot record with an identifying means included within the master boot record.

(m) loading the master boot record into random access memory upon locating the master boot record among the data records on the direct access storage device.

27. The method of claim 24, further including the step of validating successful load of the master boot record.

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