The present invention relates to a bipolar bump transistor as set forth in claim 1 and to a method of manufacturing the same.

For static reasons, because of the mechanical stress, as well as for electric reasons, because of the terminal contacts, transistors, like other semiconductor devices, are attached to a lead frame in the course of the manufacting process. This is commonly done by adhesive bonding, soldering, or alloying. One of the major surfaces of the silicon chip containing the device, namely the back surface, is attached to the widened surface of one of the leads of the lead frame. To achieve better electric contact or heat transfer, the back surface is metallized; this applies to both integrated circuits and single transistors. In the case of a single transistor, the back is usually the collector contact, while base and emitter are connected to the associated external leads by conventional wire bonding.

The method described has a number of disadvantages. For instance, the back of the silicon chip must be etched or ground prior to the metallization to obtain a flat surface.

In addition, it is time-consuming and expensive to connect a plurality of chips with the associated external leads by individual bond wires. As is well known, assembly costs represent a large part of the total costs of finished semiconductor devices.

Therefore, a number of methods have been developed which avoid the wire-bonding operation and make it possible to automate the mounting and the bonding operation. The following three possibilities, which are representative of these methods, are described in I. Ruge, "Halbleitertechnologie", Springer-Verlag Berlin, 1975.

In the flip-chip bonding technique, bonding pads at the edge of the semiconductor chip are processed to give them raised contact bumps. The chip is directly attached to the lead frame, which is provided with a matching lead pattern, with the contact side down, see GB-A-2004686.

Another method is the so-called beam-lead technique. It differs from the other assembly techniques in that the leads to the bonding pads at the edge of the chip serve as mechanical mounts by means of which the chip is attached to the lead frame. This method is relatively complicated and costly; the manufacture of the beam leads, in particular, requires many process steps.

A third possibility is the so-called spider-bonding technique, in which, unlike in the beam-lead technique, the leads or electrodes are formed independently of the chip. A lead frame (spider) is bonded directly to the

bonding pads on the chip.

All three methods described above are used only with integrated circuits, the two former ones, in particular, being so complicated and costly that they offer no advantages over the conventional bonding technique in the case of both individual semiconductor devices and transistors. For this reason and because of the conventional structure of transistors, the proven wire-bonding technique is still widely used, see GB-A-1199445.

The invention as claimed solves the problem of providing a transistor which is suitable for a low-cost assembly technique and permits control of the critical electrical parameters, such as saturation and high-current behavior. It is also within the scope of the invention to provide a method of manufacturing such a transistor.

The advantages of the invention lies in the solution of the problem itself and in the fact that a transistor is obtained which exhibits very good heat dissipation, because the heat is removed directly via the emitter-contact bump. Further advantages are the self-alignment of the metal contacts, the elimination of the grinding or etching or of the metallization of the wafer back surface, the saving of photo-etching processes as compared with the conventional methods of forming contact bumps, and the possibility of adapting the configuration of the emitter- and base-edge lengths to the desired electrical characteristics of the transistor.

Other bump structures are described in EP-A-229426.

The invention will now be explained in greater detail with reference to the accompanying drawings of a preferred embodiment of the invention, in which:

Fig. 1 is a top view of a bipolar bump transistor in accordance with the invention;

Fig. 2 is a section taken along line A-A of Fig. 1, and

Figs. 3 to 6 are schematic sectional views of the results of process steps during the manufacture of the transistor or Fig. 2.

Fig. 1, a top view of a bipolar bump transistor in accordance with the invention, shows a metal layer 91 which covers a large part of the first major surface of the transistor and under which lies the collector region 4, which is not visible in the top view. It can be seen that the metal layer 91 has an opening in which two further metal layers 92, 93 are arranged. All three metal layers 91, 92, 93 are separated from each other by an insulating layer 6, in this example a silicon-dioxide layer. The use of another insulating material, such as silicon nitride, is within the scope of the invention. The metal layer 93 covers part of the invisible base region 7, whose boundary is indicated by the dashed line 71. The base region 7, in turn, contains the likewise invisible emitter region 8, whose boundary is indicated by the dashed line 81. The emitter region 8 is largely covered by the metal layer 92. The metal layers 91, 92, 93 support the contact bumps associated with the

respective underlying active regions, namely the contact bump 11 for the collector region, the contact bump 12 for the emitter region, and the contact bump 13 for the base region. It can be seen from Fig. 1 that the emitter region and, thus, the base region are completely framed by the collector region, and that in the embodiment shown, the emitter and base regions are interdigitated to increase the length of the edge line.

Fig. 2, a section taken along line A-A of Fig. 1, shows the substrate 1, which is composed of a heavily doped lower layer 2 of n^{++}-type conductivity and an upper layer 3 of the same conductivity type which is more lightly doped than the lower layer 2, i.e., an n-type layer. In the substrate 1, a region of the conductivity type of the substrate, namely the collector region 4 of n^{+}-type conductivity, has been formed from the top side 31 (first major surface) of the substrate, leaving free a central region. The collector region 4 extends into the lower layer 2. The base region 7 of p-type conductivity extends into the free central region from the top side 31 and, in turn, contains a region of n^{+}-type conductivity, namely the emitter region 8, which was formed from the top side 31. The more heavily doped surface layer 41 of the collector region 4 is covered by the metal layer 91, which supports the contact bump 11. Correspondingly, the emitter region 8 is covered by the metal layer 92 with the contact bump 12, and the base region 7 by the metal layer 93 with the contact bump 13. Between the metal layers 91, 92, 93, the silicon-dioxide

layer 6 is disposed.

The manufacture of such a transistor will now be explained with the aid of the process steps illustrated in Figs. 3 to 6.

Starting with an n-type substrate 1 consisting of two layers of which the lower layer 2 is heavily doped, i.e., of n^{++}-type conductivity, while the upper layer 3 is more lightly doped, i.e., of n-type conductivity, a silicon-dioxide layer 6 is deposited on the top side 31 in a conventional manner. In the area in which the collector region 4 is to be formed, the silicon-dioxide layer 6 is removed using conventional photoetching techniques. Through the opening thus obtained, the n^{+}-type collector region 4 is then formed in a known manner by diffusion or ion implantation followed by a temperature process. It extends into the lower layer 2 and bounds a central portion which remains free for the time being. At the same time, the silicon-dioxide layer 6 on the top side 31 is closed again by oxidation (Fig. 3).

Next, the silicon-dioxide layer 6 is removed in a second photoetch step where an opening is required for forming the base region in the central portion, and through this opening, the base region is formed by introducing p-type dopants (diffusion or implantation). Here, too, the opening in the silicon-dioxide layer 6 is closed again in a temperature process by oxidation (Fig. 4).

Then, in a third photoetch step, the portion of the silicon-dioxide layer 6 covering the base region is removed in the emitter area and, at the same time, the surface area of the collector region 4 is exposed. Together with the introduction of dopants (diffusion or ion implantation) for forming the n-type emitter region 8, a more heavily doped surface layer having the same penetration depth as the emitter region 8 is formed in the collector region 4. This surface layer 41 provides a particularly low-resistivity path to the contact to be deposited.

Next, in a fourth photoetch step, a contact window for the base region 7 is opened in the silicon-dioxide layer 6. The structure shown in Fig. 5 is thus obtained.

Thereafter, the entire surface of the semiconductor device is covered with a metal layer 9, preferably of palladium, to which a photoresist layer 10 is applied. In the latter, the holes required for the contact bumps are made in a fifth photoetch step, after which the contact bumps 11, 12, and 13 are plated on in the areas of the collector region 4, the emitter region 8, and the base region 7, respectively, the contact material being preferably silver, which may be gold-plated to aid the soldering process (Fig. 6).

After removal of the photoresist layer, the weakly adhering metal is removed from the silicon-dioxide layer 6, so that the structure of the finished device shown in Fig. 2 is obtained. The finished device may be covered with a passivating layer of, e.g., polyimide to protect it from damage or contamination.

* C L M S *

Claims

1. Bipolar bump transistor comprising

- a substrate (1) of a first conductivity type consisting of a heavily doped lower layer (2) and a more lightly doped upper layer (3),

- a heavily doped collector region (4) of the first conductivity type which extends from the surface (31) of the upper layer (3) into the lower layer (2) and forms a boundary,

- a base region (7) of a second conductivity type contained in the upper layer (3) within the boundary and at a distance from the collector region (4),

- an emitter region (8) of the first conductivity type embedded in the base region (7),

- metal layers (91, 92, 93) on the surface (31) which partly cover the collector region (4), the base region (7), and the emitter region (8) and are separated by an insulating layer (6), and

- contact bumps (11, 12, 13) disposed on the metal layers (91, 92, 93) in the areas of the collector region (4), the base region (7), and the emitter region (8).

* C L M S *

2. A transistor as claimed in claim 1, characterized in that the insulating layer (6) is made of silicon dioxide.

3. A transistor as claimed in claim 1 or 2, characterized in that the metal layers (91, 92, 93) are made of palladium.

4. A transistor as claimed in any one of claims 1 to 3, characterized in that the emitter and base regions (7, 8) are interdigitated.

5. A transistor as claimed in any one of claims 1 to 4, characterized in that the upper layer (3) is an epitaxial layer.

6. Method of manufacturing a transistor as claimed in any one of claims 1 to 5, characterized by the following steps:

a) providing a substrate (1) of a first conductivity type consisting of a heavily doped lower layer (2) and a more lightly doped upper layer (3);

b) depositing a silicon-dioxide layer (6) on the surface (31) of the substrate (1) and removing the silicon-dioxide layer (6) in a first photo-etch step where the collector region is to be formed.

c) introducing dopants of the first conductivity type to form the collector region (4) and

simultaneously restoring the covering insulating layer (6);

d) opening a hole in the base area in a second photoetch step and introducing dopants of a second conductivity type and simultaneously restoring the covering insulating layer (6);

e) opening a hole in the emitter area and simultaneously reexposing the surface area of the collector region in a third photoetch step;

f) introducing dopants of the first conductivity type to form the emitter region (8) and simultaneously increasing the dopant concentration in the surface area (41) of the collector region (4);

g) opening a contact window for the base region (7) in a fourth photoetch step;

h) depositing a metal layer (9) by evaporation;

i) covering the metal layer (9) with a photoresist layer (10) and patterning the same in a fifth photoetch step to form holes for the contact bumps (11, 12, 13);

j) growing the contact bumps (11, 12, 13) in the holes in the photoresist layer (10), and

* C L M S *

k) removing the photoresist layer (10) and parts of the metal layer (9).

7. A method as claimed in claim 6, characterized in that the dopants are introduced by ion implantation followed by a drive-in step.

8. A method as claimed in claim 6, characterized in that the dopants are introduced by diffusion.

9. A method as claimed in any one of claims 6 to 8, characterized in that the insulating layer (6) is made of silicon dioxide.