

## ABSTRACT

### SEMICONDUCTOR MEMORY DEVICE

5 A semiconductor memory device includes a substrate defined with a cell array region and a connection region which extends in a first direction from the cell array region; an electrode structure including a bottom electrode structure which includes a plurality of bottom electrodes stacked on the substrate to be separated from one another  
10 and a top electrode structure which includes a plurality of top electrodes stacked on the bottom electrode structure to be separated from one another and has a stepped structure which includes a plurality of stepping surfaces, in the connection region; and a plurality of recess holes formed to a first depth from stepping surfaces of the  
15 stepped structure, and having bottom surfaces which expose the bottom electrode structure, wherein the first depth is the substantially same as a height of the top electrode structure, and distances of the bottom surfaces of the recess holes from the substrate are different from one another.

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FIG. 6