

Description

Technical Field

This invention relates generally to digital communication systems and, more particularly, to a communication system using conventional differential phase shift keying (DPSK) or frequency shift keying (FSK) modulation.

Background Art

Typically, telephone data transmission is in a continuous mode system with conventional differential phase shift keying (DPSK) or frequency shift keying (FSK) modulation over a 2-wire cable pair. Other techniques for achieving full duplex bidirectional transmission which have advantages over a continuous mode system are also known.

There is known from US Patent No. 3 319 241 a continuous mode communication system for generating an output signal of a selected primary frequency in order to provide frequency encoding of an input signal. However, disadvantages of a continuous mode system in full duplex bidirectional transmission result from the separation of both streams of data. Typically, frequency separation or algebraic cancellation is used to separate the data. However, frequency separation may be complicated to implement and is both bandlimited and distance limited. Algebraic cancelling is not exact for all applications and may also create a severe echo problem from various harmonics and transmission line reflections. Therefore, a promising alternative to continuous mode operation is a time compression multiplexed (TCM) system which is also known as a burst mode or ping-pong system. The burst mode system divides the two directions of transmission by separating them in time so that at any particular point in time, transmission is unidirectional. The penalty which results from using the burst mode system is a substantially higher frequency of transmission since data must be bursted at least at twice the frequency of the data entering the system to insure adequate time separation. Whenever DPSK or FSK modulation is used in a burst mode system, a very wide spectral content results. A further disadvantage results for FSK modulation because D.C. balance is usually not maintained for each burst of data and an extra bit is required to maintain D.C. balance. When a digital burst mode transmission is not D.C. balanced bit by bit, inter-symbol interference results and may destroy the meaning of the transmitted data. Whenever phase modulation is used, D.C. balance is maintained, but harmonic energy may radiate into other communication channels.

Summary of the Invention

Accordingly, an object of the present invention is to provide an improved method of encoding of an input signal and a communication system capable of operating in burst mode operation with a low spectral content.

A further object of the present invention is to

provide an improved communication system utilizing a hybrid DPSK modulation for burst mode operation.

Yet another object of the present invention is to provide an improved communication system utilizing a hybrid DPSK modulated signal which is D.C. balanced in a burst mode system and has substantially reduced harmonic energy.

In accordance with a first aspect of the invention there is provided a communication system for generating an output signal of a selected primary frequency in order to provide encoding of an input signal characterized in that, the communication system, for generating an output signal having a plurality of bursts of digital data bits serially modulated thereon at the primary frequency during respective predetermined bit periods in order to provide differential phase encoding of an input signal in the form of serial digital data bits while frequency modulating the output signal, comprises:

control means for receiving the serial digital data bits and providing a start control signal in response thereto and a stop control signal in response to the failure to receive a digital data bit within the first half of any of the bit periods, and for providing during each of a plurality of control periods a data control signal in response to each received digital datum; and

frequency generator means coupled to the control means for generating a half cycle of the output signal having the same frequency as a last half cycle of an immediately preceding generation of the output signal in response to the start control signal, for generating a full cycle of said output signal at said primary frequency and in phase with the preceding half cycle of said output signal in response to the presence of each of said data control signals, for generating a half cycle of said output signal at a secondary frequency one-half said primary frequency with no phase change with the preceding half cycle of the output signal in response to the absence of a data control signal during a control period, and for generating a stop control signal in response to the failure to receive a digital datum within a first half of any of the bit periods.

In accordance with a second aspect of the invention there is provided a method of providing an output signal of a selected primary frequency in order to provide encoding of an input signal characterized by the steps of:

receiving a burst of phase encoded serial digitized input data bits having bit periods of a primary frequency;

providing, in response to the receipt of a first bit of the input data, a start control signal;

generating, in response to the start control signal, a half cycle of the output signal at substantially the primary frequency and in phase with a last half cycle of an immediately preceding generation of the output signal;

providing, during a control period which corresponds with a data bit period and precedes the data bit period by one-half of a preceding bit

period, a primary control signal in response to each received digital datum having a first predetermined value and providing a second control signal in response to each of the primary control signals;

generating a full cycle of the output signal at the primary frequency in phase with the preceding cycle of the output signal in response to each of the primary control signals;

generating a half cycle of the output signal at a secondary frequency substantially one-half the primary frequency and with no phase change with a preceding half cycle of the output signal in response to each secondary control signal;

providing, in response to the absence of a digital data bit within a predetermined amount of time, a stop control signal; and

generating no output signal in response to the stop control signal.

It will be appreciated that although in a preferred embodiment of the invention a burst mode operation is used, the communication system may operate in a continuous mode operation. It will also be appreciated that since the invention utilizes both frequency and phase information to provide an encoded output signal, D.C. balance is maintained together with reduced harmonic energy and the burst mode operation provides improved bidirectional transmission over the continuous mode system.

The above and other objects, features and advantages of the present invention will be more clearly understood from the following detailed description, by way of example only, with reference to the accompanying drawings.

Brief Description of the Drawings

FIG. 1 illustrates in graphic form an example of a DPSK modulated signal known in the prior art;

FIG. 2 illustrates in graphic form an example of an FSK modulated signal known in the prior art;

FIG. 3 illustrates in block diagram form a communication system illustrating the preferred embodiment of the present invention;

FIG. 4 illustrates in schematic and block diagram form a communication system constructed in accordance with the preferred embodiment of the present invention;

FIG. 5 illustrates in graphical form signals associated with the communication system of FIG. 4;

FIG. 6 illustrates in graphical form a triangular approximation of the output signal shown in FIG. 5;

FIG. 7 illustrates in schematic form an example of a controller which produces the triangular approximation shown in FIG. 6 and which is used with the communication system of FIGS. 3 and 4; and

FIG. 8 illustrates in graphical form signals associated with the controller shown in FIG. 7.

Description of the Preferred Embodiment

Shown in FIG. 1 is an example of conventional differential phase shift keyed modulation (DPSK) utilized in high speed digital data transmission over standard 2-wire telephone wire. The

example shown is that of a digital byte represented as "1101". The frequency of the DPSK signal is that of the carrier frequency of the transmitted data. Assume only for the purpose of illustration that a logic "1" is represented by no change in phase from the preceding cycle. Therefore a logic "0" would be represented by a change in phase from the preceding cycle such as a 180 degree phase shift. A typical data transmission frequency for an input carrier signal operating in a burst mode system is 256 kHz. Unfortunately, the 180 degree phase shift in conventional DPSK produces a large amount of second harmonic energy which is never utilized for the demodulation process. Additionally, the second harmonic energy may radiate into other communications channels and cause interference. To eliminate the problem, the second harmonic would have to be filtered before transmission. Because the phase information is carried at a high frequency, the information is rapidly attenuated by the inherent lowpass characteristic of the transmission media and is more vulnerable to noise disruptions.

Shown in FIG. 2 is an example of conventional frequency shift keyed modulation (FSK) utilized in high speed digital data transmission over standard 2-wire telephone wire. The example shown is for an identical digital byte of "1101". Assume only for the purpose of illustration that a logic "1" indicates a first predetermined frequency. Therefore a logic "0" would indicate a second predetermined frequency. A disadvantage of FSK modulation is that there is a likelihood of losing D.C. balance. Due to the characteristics of a twisted pair of wire, it is necessary that the wire be D.C. balanced to prevent bias distortion and intersymbol interference. Unfortunately, a D.C. bias may exist after a byte transmission such as the one illustrated in FIG. 2. For cycles 1, 2 and 4 there is only a D.C. signal, the sum of which is not balanced. Although cycle 3 is D.C. balanced, there is no D.C. balance of the entire signal bit by bit. To prevent having a large D.C. bias on the transmission line, a D.C. balancing bit must be inserted during the byte burst to balance the D.C. bias for the entire burst. A disadvantage with using a balancing bit is the loss of time required to transmit the balancing bit and a resulting distance limitation.

Shown in FIG. 3 is a block diagram of a communication system 10 comprising a controller 12 for providing first and second control signals to a primary frequency generator 14 and to a secondary frequency generator 16, respectively. Communication system 10 is a transmission system capable of operating either in a continuous mode or in a burst mode operation. Communication system 10 utilizes an improved and hybrid differential phase shift keying modulation having substantial advantages over conventional DPSK and FSK modulation.

Shown in FIG. 4 is communication system 10 constructed in accordance with the preferred embodiment of the present invention. Controller 12 of communication system 10 is coupled to the

control inputs of transmission gates 18, 20, 22 and

In the preferred form, transmission gates 18, 20, 22 and 24 are conventional MOS transmission gates clocked in a conventional manner by control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} which control the rate and direction of polarity of the output signal, respectively. An embodiment of controller 12 is shown in greater detail in FIG. 7. Although in the preferred form controller 12 is shown as supplying two control signals, the present invention may also be practiced with a controller providing only a single control signal which controls the rate of the output signal. When a single control signal is utilized, no phase change occurs when the rate change occurs. Transmission gates 18 and 20 each have an input connected together and coupled to a positive potential terminal of a voltage source 26. A negative potential terminal of voltage source 26 is coupled to a reference voltage such as ground. An output of transmission gate 18 is connected to a first terminal of a resistor 28, and an output of transmission gate 20 is connected to a first terminal of a resistor 30. Transmission gates 22 and 24 each have an input connected together and coupled to a negative potential terminal of a voltage source 32. A positive potential terminal of voltage source 32 is coupled to the reference or ground voltage. An output of transmission gate 22 is connected to a first terminal of a resistor 34, and an output of transmission gate 24 is connected to a first terminal of a resistor 36. Resistors 28, 30, 34 and 36 each have a second terminal connected together and coupled to an inverting input of an operational amplifier 38. A noninverting input of operational amplifier 38 is coupled to the reference or ground voltage. A feedback capacitor 40 has a first plate coupled to the inverting input of operational amplifier 38 and a second plate coupled to an output of operational amplifier 38. Coupled in parallel with feedback capacitor 40 is a transmission gate 42 having an input coupled to the first plate of feedback capacitor 40 and an output coupled to both the second plate of feedback capacitor 40 and the output of operational amplifier 38. Coupled to transmission gate 42 is a clear integrator control signal shown in FIG. 8 which zeroes the charge on feedback capacitor 40 between bursts of data. Transmission gate 42 is not needed for a continuous mode operation.

In operation, the signals shown in FIG. 5 illustrate how communication system 10 provides a hybrid DPSK modulated signal. Assume for the purposes of illustration that a data transmission is in progress. Both the input data and output signal have distinct bit periods. Control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} are generated during a control period which corresponds to a respective one of said bit periods but preceding the bit period by at least one-half of a bit period. In a preferred embodiment, control signals C_{R1} and C_{R2} are generated at the half cycle boundary of the bit periods and C_{D1} and C_{D2} may be generated at the one-fourth, one-half and three-fourth cycle boundaries in order to generate the triangle approximation. When only

one control signal is used as previously mentioned, that one control signal controls the rate of the output signal and the phase or direction of the output signal is automatically fixed by controller 12 to never change at a half cycle boundary. At the initial point of observation, a digital "0" is being received at the input of controller 12. Assume also that controller 12 is programmed so that when a "0" is received during a control period, the output signal is frequency shifted to one-half the frequency of the input carrier at the half cycle boundary of the output signal. The output signal is not frequency shifted at the half cycle boundary of the preceding bit period when a "1" is received by controller 12 but remains at the input carrier frequency. Thus, the improved and hybrid DPSK modulation is actually a frequency modulation of a phase encoded signal. In order to provide control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} which provide the information as to whether to change frequency or not, the serial digital data must be received by controller 12 at least one-half of a bit period earlier. In the example shown, during a bit period of the output signal labeled A', the output signal shown had a frequency change to one-half of the input carrier frequency. It should be noted that the "0" for bit period A' was received at least by the middle of the preceding bit period. At least by the middle of bit period A' the input "1" for bit period B' is received. By the middle of bit period A', controller 12 generates control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} which are necessary to frequency shift the output signal for bit period B' back to the frequency of the input carrier. By the middle of bit period B', no input signal has been received and controller 12 generates a stop signal denoted by a single asterisk in FIG. 5 which indicates that a single half cycle at the carrier frequency of 256 KHz and of opposite polarity to the first half cycle of bit period B' should be generated during the last half cycle of bit period B'. This is the end of a burst of signal energy and no data is present on the line for some finite time. Between bursts, transmission gate 42 is closed by the clear integrator control signal and all charge on capacitor 40 is zeroed and the voltage at the output of operational amplifier 38 is held at the reference or ground voltage.

When another burst of signal energy is received, controller 12 generates a start signal denoted by a double asterisk in FIG. 5 which generates an output signal for only the first half of bit period C'. The initial half cycle of the output signal for a new burst will have the same frequency as the frequency of the last half bit period of the preceding burst which is the primary frequency. Controller 12 is programmed so that for the first half cycle, an initial "0" provides a half cycle of output signal which is out of phase with the last cycle of the preceding burst and an initial "1" provides a half cycle of output signal which is in phase with the last cycle of the preceding burst. Since a "0" is initially received, the first half of bit period C' is opposite in phase to the output signal of the last bit period which was B'. By the middle

of bit period C', the input bit for the following bit D' must be received and control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} generated in response. A "1" for bit period D' is received and therefore the output signal is not frequency shifted at the half cycle boundary of bit period C'. By the middle of bit period D', the input bit for the following bit E' must be received and control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} generated in response. A "0" for bit period E' is received and therefore an output signal exhibiting a change in frequency to one-half the carrier frequency is generated during the last half of bit period D' and the first half of bit period E'. By the middle of bit period E', the input bit for the following bit period F' must be received and control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} generated in response. A "0" for bit period F' is received and therefore an output signal exhibiting a frequency of one-half the frequency of the input carrier is generated during the last half of bit boundary E' and the first half of bit period F'. Thus, the frequency of the output signal remains the same from the half cycle boundary of bit period D' to the half cycle boundary of bit period F'. By the middle of bit period F', the input bit for the following bit period G' must be received and control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} generated therefor. A "1" for bit period G' is received and therefore an output signal exhibiting a frequency equal to the input carrier is generated from the half cycle boundary of bit period F' until the half cycle boundary of bit period G'. By the middle of bit period G', the input bit for bit period H' must be received and control signals C_{R1} , C_{R2} , C_{D1} and C_{D2} generated in response. A "1" for bit period H' is received and therefore an output signal exhibiting a frequency equal to the input carrier is again generated and is provided from the half cycle boundary of bit period G' until the half cycle boundary of bit period H'. By the middle of bit period H', no further bits to the input signal are received and controller 12 generates a stop signal denoted by a single asterisk as previously explained for the end of the previous burst. The control signal denoted by a single asterisk generates a single half cycle signal during the last half of bit period H'. The single half cycle signal is of opposite polarity from the first half of bit period H' of the output signal. The frequency of the last half cycle of bit period H' is the input carrier or primary frequency. This is the end of another burst and no further output signal is generated until another burst is received.

Shown in FIG. 6 is the output signal corresponding to the example illustrated in FIG. 5 and a triangular waveform approximation of the output signal. The transmission gates which are required to be closed and opened to produce the triangular waveforms of varying slope are designated in FIG. 6.

FIG. 7 illustrates communication system 10 with controller 12 in greater detail and which may be easily implemented by conventional logic to provide triangular ramp rate and direction control signals which will control transmission gates 18,

20, 22 and 24 to provide the output signal shown in FIG. 6. Controller 12 comprises a D-type flip-flop 44 having the D input thereof coupled to the input serial data, a clock input coupled to a clock 1 signal and the S input thereof coupled to a control 3 signal. A Q output of flip-flop 44 provides the ramp rate control and is coupled to a first input of AND gates 46 and 48. A D-type flip-flop 50 has the S input thereof coupled to a control 1 signal and the reset input thereof coupled to a control 2 signal. An inverter 52 has an input coupled to a Q output of flip-flop 50 and an output coupled to a D input of flip-flop 50. The Q output of flip-flop 50 provides the ramp direction control and is coupled to a second input of AND gate 46, to the control input of transmission gate 20 and to the input of an inverter 54. An output of inverter 54 is coupled to both a second input of AND gate 48 and to the control input of transmission gate 22. A clock generator 56 has an input coupled to the input serial data and an output for providing a clock 2 signal to the clock input of flip-flop 50.

In this configuration, gates 18, 20, 22 and 24 are switched to function as a primary frequency generator to generate a full cycle of the output signal at the primary frequency of 256 KHz. By selectively opening gates 18 and 24 in response to the input data, a secondary frequency which is one-half the primary frequency and in phase with the primary frequency is provided. Operational amplifier 38 and integrating capacitor 40 function as an integrator to provide the triangular waveform of FIG. 6 by integrating the current which is summed into the noninverting or negative input of operational amplifier 38. Although in the preferred form resistors 28, 30, 34 and 36 are used, impedances may be freely substituted to accomplish the same function.

Shown in FIG. 8 are signals associated with the operation of controller 12. An initial burst of data is shown. At the beginning of a burst a control 3 signal will be generated. Either a control 1 or a control 2 signal will be generated depending upon the following Boolean algebra equations:

$$\text{Control 1} = [D_1 \cdot P + \overline{D_1} \cdot \overline{P}] \cdot \text{Control 3}$$

$$\text{Control 2} = [D_1 \cdot \overline{P} + \overline{D_1} \cdot P] \cdot \text{Control 3}$$

where

D_1 = the Boolean value (either a logic "1" or logic "0") that the initial cycle of a burst is to represent; and

P = a Boolean variable such that $P = 1$ if the polarity of the last half of the last cycle of the previous burst was positive and $P = 0$ if the polarity of the last half of the last cycle of the previous burst was negative.

Clock generator 56 provides a clock 2 signal which varies as shown in FIG. 8 depending upon the logic state of the input data. A clock 1 signal is generated at every half cycle boundary. The ramp rate and ramp direction signals therefore control transmission gates 18, 20, 22 and 24 to provide the output signal.

The hybrid DPSK modulated output signal has a

lower amount of second harmonic energy than a corresponding output signal produced by conventional DPSK modulation. Since the modified DPSK signal has the phase information carried at a lower frequency, a stronger receivable signal is provided than the corresponding signal produced by conventional DPSK modulation. By now it should also be apparent that a modulated output signal of a selected primary frequency having a zero direct current component bit by bit has been provided. The output signal may be decoded by conventional DPSK modulation techniques and the demodulation process has remained unchanged. This modification of conventional differential phase shift keyed modulation may be used for high speed digital data transmission over standard telephone wire in either a continuous mode or a burst mode operation. When continuous mode operation exists, controller 12 operates in the same manner as in the preceding illustration except the control signals denoted by a single and double asterisk are never generated.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above.

Claims

1. A communication system (10) for generating an output signal of a selected primary frequency in order to provide encoding of an input signal characterized in that the communication system for generating an output signal having a plurality of bursts of digital data bits serially modulated thereon at the primary frequency during respective predetermined bit periods in order to provide differential phase encoding of an input signal in the form of serial digital data bits while frequency modulating the output signal, comprises:

control means (12) for receiving the serial digital data bits and providing a start control signal in response thereto and a stop control signal in response to the failure to receive a digital data bit within the first half of any of the bit periods, and for providing during each of a plurality of control periods a data control signal in response to each received digital datum; and

frequency generator means (18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40 and 42) coupled to the control means (12) for generating a half cycle of the output signal having the same frequency as a last half cycle of an immediately preceding generation of the output signal in response to the start control signal, for generating a full cycle of said output signal at said primary frequency and in phase with the preceding half cycle of said output signal in response to the presence of each of said data control signals, for generating a half cycle of said output signal at a secondary frequency one-half said primary frequency with no

phase change with the preceding half cycle of the output signal in response to the absence of a data control signal during a control period, and for generating a stop control signal in response to the failure to receive a digital datum within a first half of any of the bit periods.

2. The communication system of claim 1 wherein said frequency generator means are further characterized by:

first switching means (18) having first and second terminals, and a control terminal coupled to said control means (12);

first impedance means (28) having a first terminal coupled to the second terminal of said first switching means (18), and a second terminal;

first supply means (26) having a first terminal of first polarity type coupled to the first terminal of said first switching means (18), and a second terminal of second polarity type coupled to a reference voltage;

second switching means (20) having a first terminal coupled to the first terminal of the first supply means (26), a control terminal coupled to the control means (12), and a second terminal;

second impedance means (30) having a first terminal coupled to the second terminal of said second switching means (20), and a second terminal coupled to the second terminal of said first impedance means (28);

third switching means (22) having first and second terminals, and a control terminal coupled to said control means (12);

third impedance means (34) having a first terminal coupled to the second terminal of said third switching means (22), and a second terminal;

second supply means (32) having a first terminal of first polarity type coupled to the first terminal of said third switching means (22), and a second terminal of second polarity type coupled to the reference voltage;

fourth switching means (24) having a first terminal coupled to the first terminal of the second supply means (32), a control terminal coupled to the control means (12), and a second terminal;

fourth impedance means (36) having a first terminal coupled to the second terminal of said fourth switching means (24), and a second terminal coupled to the second terminal of said third impedance means (34); and

an integrator (38, 40, 42) coupled to the second terminals of the first, second, third and fourth impedance means.

3. A method of providing an output signal of a selected primary frequency in order to provide encoding of an input signal characterized by the steps of:

receiving a burst of phase encoded serial digitized input data bits having bit periods of a primary frequency;

providing, in response to the receipt of a first bit of the input data, a start control signal;

generating, in response to the start control signal, a half cycle of the output signal at substantially the primary frequency and in phase with a last half cycle of an immediately preceding

lower amount of second harmonic energy than a corresponding output signal produced by conventional DPSK modulation. Since the modified DPSK signal has the phase information carried at a lower frequency, a stronger receivable signal is provided than the corresponding signal produced by conventional DPSK modulation. By now it should also be apparent that a modulated output signal of a selected primary frequency having a zero direct current component bit by bit has been provided. The output signal may be decoded by conventional DPSK modulation techniques and the demodulation process has remained unchanged. This modification of conventional differential phase shift keyed modulation may be used for high speed digital data transmission over standard telephone wire in either a continuous mode or a burst mode operation. When continuous mode operation exists, controller 12 operates in the same manner as in the preceding illustration except the control signals denoted by a single and double asterisk are never generated.

While the invention has been described in the context of a preferred embodiment, it will be apparent to those skilled in the art that the present invention may be modified in numerous ways and may assume many embodiments other than that specifically set out and described above.

Claims

1. A communication system (10) for generating an output signal of a selected primary frequency in order to provide encoding of an input signal characterized in that the communication system for generating an output signal having a plurality of bursts of digital data bits serially modulated thereon at the primary frequency during respective predetermined bit periods in order to provide differential phase encoding of an input signal in the form of serial digital data bits while frequency modulating the output signal, comprises:

control means (12) for receiving the serial digital data bits and providing a start control signal in response thereto and a stop control signal in response to the failure to receive a digital data bit within the first half of any of the bit periods, and for providing during each of a plurality of control periods a data control signal in response to each received digital datum; and

frequency generator means (18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40 and 42) coupled to the control means (12) for generating a half cycle of the output signal having the same frequency as a last half cycle of an immediately preceding generation of the output signal in response to the start control signal, for generating a full cycle of said output signal at said primary frequency and in phase with the preceding half cycle of said output signal in response to the presence of each of said data control signals, for generating a half cycle of said output signal at a secondary frequency one-half said primary frequency with no

phase change with the preceding half cycle of the output signal in response to the absence of a data control signal during a control period, and for generating a stop control signal in response to the failure to receive a digital datum within a first half of any of the bit periods.

2. The communication system of claim 1 wherein said frequency generator means are further characterized by:

first switching means (18) having first and second terminals, and a control terminal coupled to said control means (12);

first impedance means (28) having a first terminal coupled to the second terminal of said first switching means (18), and a second terminal;

first supply means (26) having a first terminal of first polarity type coupled to the first terminal of said first switching means (18), and a second terminal of second polarity type coupled to a reference voltage;

second switching means (20) having a first terminal coupled to the first terminal of the first supply means (26), a control terminal coupled to the control means (12), and a second terminal;

second impedance means (30) having a first terminal coupled to the second terminal of said second switching means (20), and a second terminal coupled to the second terminal of said first impedance means (28);

third switching means (22) having first and second terminals, and a control terminal coupled to said control means (12);

third impedance means (34) having a first terminal coupled to the second terminal of said third switching means (22), and a second terminal;

second supply means (32) having a first terminal of first polarity type coupled to the first terminal of said third switching means (22), and a second terminal of second polarity type coupled to the reference voltage;

fourth switching means (24) having a first terminal coupled to the first terminal of the second supply means (32), a control terminal coupled to the control means (12), and a second terminal;

fourth impedance means (36) having a first terminal coupled to the second terminal of said fourth switching means (24), and a second terminal coupled to the second terminal of said third impedance means (34); and

an integrator (38, 40, 42) coupled to the second terminals of the first, second, third and fourth impedance means.

3. A method of providing an output signal of a selected primary frequency in order to provide encoding of an input signal characterized by the steps of:

receiving a burst of phase encoded serial digitized input data bits having bit periods of a primary frequency;

providing, in response to the receipt of a first bit of the input data, a start control signal;

generating, in response to the start control signal, a half cycle of the output signal at substantially the primary frequency and in phase with a last half cycle of an immediately preceding



generation of the output signal;

providing, during a control period which corresponds with a data bit period and precedes the data bit period by one-half of a preceding bit period, a primary control signal in response to each received digital datum having a first predetermined value and providing a second control signal in response to each of the primary control signals;

generating a full cycle of the output signal at the primary frequency in phase with the preceding cycle of the output signal in response to each of the primary control signals;

generating a half cycle of the output signal at a secondary frequency substantially one-half the primary frequency and with no phase change with a preceding half cycle of the output signal in response to each secondary control signal;

providing, in response to the absence of a digital data bit within a predetermined amount of time, a stop control signal; and

generating no output signal in response to the stop control signal.

Patentansprüche

1. Übertragungssystem (10) zum Erzeugen eines Ausgangssignals einer ausgewählten Primärfrequenz, um eine Kodierung eines Eingangssignals zu bewirken, dadurch gekennzeichnet, daß das Übertragungssystem zum Erzeugen eines Ausgangssignals mehrere Bursts digitaler Datenbits seriell darauf moduliert bei der Primärfrequenz während entsprechender vorbestimmter Bitperioden aufweist, um eine Differenzphasenkodierung eines Eingangssignals in die Form serieller digitaler Datenbits zu bewirken, während das Ausgangssignal frequenzmoduliert wird, enthaltend:

eine Steuerungseinrichtung (12) zum Empfangen der seriellen digitalen Datenbits und zum Abgeben eines Startsteuersignals in Abhängigkeit davon und eines Stoppsteuersignals in Abhängigkeit davon, daß kein digitales Datenbit innerhalb der ersten Hälfte irgendeiner der Bitperioden empfangen wird, und zum Abgeben eines Datensteuersignals in jeder von mehreren Steuerperioden in Abhängigkeit von jedem empfangenen digitalen Datensignal und;

eine Frequenzgeneratoreinrichtung (18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40 und 42), die mit der Steuerungseinrichtung (12) verbunden ist, um einen Halbzyklus des Ausgangssignals zu erzeugen, der die gleiche Frequenz hat, wie ein letzter Halbzyklus eines unmittelbar vorangehend erzeugten Ausgangssignals in Abhängigkeit von dem Startsteuersignal, um einen vollen Zyklus des Ausgangssignals mit der genannten Primärfrequenz und gleichphasig mit dem vorangehenden Halbzyklus des Ausgangssignals in Abhängigkeit von der Anwesenheit eines jeden der genannten Datensteuersignale zu erzeugen, und um einen Halbzyklus des Ausgangssignals mit einer Sekundärfrequenz von der Hälfte der Primärfrequenz zu

erzeugen ohne Phasenänderung mit dem vorangehenden Halbzyklus des Ausgangssignals in Abhängigkeit von der Abwesenheit eines Datensteuersignals während einer Steuerperiode, und zum Erzeugen eines Stoppsteuersignals in Abhängigkeit davon, daß kein digitales Datensignal innerhalb einer ersten Hälfte einer der Bitperioden empfangen wird.

2. Übertragungssystem nach Anspruch 1, bei dem die Frequenzgeneratoreinrichtung weiterhin gekennzeichnet ist durch:

eine erste Schalteinrichtung (18) mit ersten und zweiten Anschlüssen und einem Steueranschluß, der mit der Steuerungseinrichtung (12) verbunden ist;

eine erste Impedanzeinrichtung (28) mit einem ersten Anschluß, der mit dem zweiten Anschluß der ersten Schalteinrichtung (18) verbunden ist, und einem zweiten Anschluß;

eine erste Versorgungseinrichtung (26) mit einem ersten Anschluß eines ersten Polaritätstyps, der mit dem ersten Anschluß der ersten Schalteinrichtung (18) verbunden ist, und einem zweiten Anschluß vom zweiten Polaritätstyp, der mit einer Bezugsspannung verbunden ist;

eine zweite Schalteinrichtung (20) mit einem ersten Anschluß, der mit dem ersten Anschluß der ersten Versorgungseinrichtung (26) verbunden ist, einem Steueranschluß, der mit der Steuerungseinrichtung (12) verbunden ist, und einem zweiten Anschluß;

eine zweite Impedanzeinrichtung (30) mit einem ersten Anschluß, der mit dem zweiten Anschluß der zweiten Schalteinrichtung (20) verbunden ist, und einem zweiten Anschluß, der mit dem zweiten Anschluß der ersten Impedanzeinrichtung (28) verbunden ist;

eine dritte Schalteinrichtung (22) mit ersten und zweiten Anschlüssen und einem Steueranschluß, der mit der Steuerungseinrichtung (12) verbunden ist;

eine dritte Impedanzeinrichtung (34) mit einem ersten Anschluß, der mit dem zweiten Anschluß der dritten Schalteinrichtung (22) verbunden ist, und einem zweiten Anschluß;

eine zweite Versorgungseinrichtung (32) mit einem ersten Anschluß vom ersten Polaritätstyp, der mit dem ersten Anschluß der dritten Schalteinrichtung (22) verbunden ist, und einem zweiten Anschluß vom zweiten Polaritätstyp, der mit der Bezugsspannung verbunden ist;

eine vierte Schalteinrichtung (24) mit einem ersten Anschluß, der mit dem ersten Anschluß der zweiten Versorgungseinrichtung (32) verbunden ist, einem Steueranschluß, der mit der Steuerungseinrichtung (12) verbunden ist, und einem zweiten Anschluß;

eine vierte Impedanzeinrichtung (36) mit einem ersten Anschluß, der mit dem zweiten Anschluß der vierten Schalteinrichtung (24) verbunden ist, und einem zweiten Anschluß, der mit dem zweiten Anschluß der dritten Impedanzeinrichtung (34) verbunden ist; und

einen Integrator (38, 40, 42), der mit den zweiten Anschlüssen der ersten, zweiten, dritten und vierten Impedanzeinrichtungen verbunden ist.

3. Verfahren zum Erzeugen eines Ausgangssi-



gnals einer ausgewählten Primärfrequenz, um die Kodierung eines Eingangssignals zu bewirken, gekennzeichnet durch die folgenden Schritte;

Empfangen eines Burst aus phasenkodierten, seriellen, digitalisierten Eingangsdatenbits, die Bitperioden einer Primärfrequenz aufweisen;

Erzeugen eines Startsteuersignals in Abhängigkeit vom Empfang eines ersten Bits der Eingangsdaten;

Erzeugen eines Halbzyklus des Ausgangssignals mit im wesentlichen der Primärfrequenz und phasengleich mit einem letzten Halbzyklus eines unmittelbar vorangehend erzeugten Ausgangssignals in Abhängigkeit von dem Startsteuersignal;

Abgeben eines primären Steuersignals während einer Steuerperiode, die einer Datenbitperiode entspricht und der Datenbitperiode um eine Hälfte einer vorangehenden Bitperiode vorangeht, in Abhängigkeit von jedem empfangenen digitalen Datensignal, das einen ersten vorbestimmten Wert hat, und Abgeben eines zweiten Steuersignals in Abhängigkeit von jedem der Primärsteuersignale;

Erzeugen eines vollen Zyklus des Ausgangssignals mit der Primärfrequenz phasengleich mit dem vorangehenden Zyklus des Ausgangssignals in Abhängigkeit von jedem der Primärsteuersignale;

Erzeugen eines Halbzyklus des Ausgangssignals mit einer Sekundärfrequenz im wesentlichen der Hälfte der Primärfrequenz und ohne Phasenänderung mit einem vorangehenden Halbzyklus des Ausgangssignals in Abhängigkeit von jedem Sekundärsteuersignal;

Abgeben eines Stoppsteuersignals in Abhängigkeit vom Fehlen eines digitalen Datenbits innerhalb einer vorbestimmten Zeitdauer; und

Erzeugen von keinem Ausgangssignal in Abhängigkeit von dem Stoppsteuersignal.

Revendications

1. Système de transmission (10) permettant de produire un signal de sortie d'une fréquence primaire sélectionnée afin d'assurer le codage d'un signal d'entrée, caractérisé en ce que le système de transmission, permettant de produire un signal de sortie qui possède plusieurs rafales de bits de données numériques produits en série à la fréquence primaire pendant des périodes de bit prédéterminées respectives afin d'assurer le codage de phase différentiel d'un signal d'entrée se présentant sous la forme de bits de données numériques en série tout en modulant en fréquence le signal de sortie, comprend:

un moyen de commande (12) servant à recevoir les bits de données numériques en série et à produire un signal de commande de démarrage en réponse à ceux-ci et un signal de commande d'arrêt en réponse à l'absence de réception d'un bit de données numériques dans les limites d'une première moitié de l'une quelconque des périodes de bit, et servant à produire pendant

chacune de plusieurs périodes de commande un signal de commande de données en réponse à chaque donnée numérique reçue; et

un moyen générateur de fréquence (18, 20, 22, 24, 26, 28, 30, 32, 34, 36, 38, 40 et 42) couplé au moyen de commande (12) afin de produire un demi-cycle du signal de sortie ayant la même fréquence qu'un dernier demi-cycle d'une production immédiatement précédente du signal de sortie en réponse au signal de commande de démarrage, de produire un cycle complet dudit signal de sortie à ladite fréquence primaire et en phase avec le demi-cycle précédent dudit signal de sortie en réponse à la présence de chacun desdits signaux de commande de données, de produire un demi-cycle dudit signal de sortie à une fréquence secondaire qui vaut la moitié de ladite fréquence primaire, sans changement de phase avec le demi-cycle précédent du signal de sortie en réponse à l'absence d'un signal de commande de données pendant une période de commande, et de produire un signal de commande d'arrêt en réponse à l'absence de réception d'une donnée numérique dans les limites d'une première moitié de l'une quelconque des périodes de bit.

2. Système de transmission selon la revendication 1, où ledit moyen générateur de fréquence est en outre caractérisé par:

un premier moyen de commutation (18) possédant des première et deuxième bornes, et une borne de commande couplée audit moyen de commande (12);

un premier moyen d'impédance (28) possédant une première borne couplée à la deuxième borne dudit premier moyen de commutation (18), et une deuxième borne;

un premier moyen d'alimentation (26) possédant une première borne d'un premier type de polarité couplée à la première borne dudit premier moyen de commutation (18), et une deuxième borne d'un deuxième type de polarité couplée à une tension de référence;

un deuxième moyen de commutation (20) possédant une première borne couplée à la première borne du premier moyen d'alimentation (26), une borne de commande couplée au moyen de commande (12), et une deuxième borne;

un deuxième moyen d'impédance (30) possédant une première borne couplée à la deuxième borne dudit deuxième moyen de commutation (20), et une deuxième borne couplée à la deuxième borne dudit premier moyen d'impédance (28);

un troisième moyen de commutation (22) possédant des première et deuxième bornes, et une borne de commande couplée audit moyen de commande (12);

un troisième moyen d'impédance (34) possédant une première borne couplée à la deuxième borne dudit troisième moyen de commutation (22), et une deuxième borne;

un deuxième moyen d'alimentation (32) possédant une première borne d'un premier type de polarité couplée à la première borne dudit troi-



sième moyen de commutation (22), et une première borne d'un deuxième type de polarité couplée à la tension de référence;

un quatrième moyen de commutation (24) possédant une première borne couplée à la première borne dudit deuxième moyen d'alimentation (32), une borne de commande couplée au moyen de commande (12), et une deuxième borne;

un quatrième moyen d'impédance (36) possédant une première borne couplée à la deuxième borne dudit quatrième moyen de commutation (24), et une deuxième borne couplée à la deuxième borne dudit troisième moyen d'impédance (34); et

un intégrateur (38, 40, 42) couplé aux deuxièmes bornes des premier, deuxième, troisième et quatrième moyens d'impédance.

3. Procédé permettant de produire un signal de sortie d'une fréquence primaire sélectionnée afin d'assurer le codage d'un signal d'entrée, caractérisé par les opérations suivantes:

recevoir une rafale de bits de données d'entrée mises sous forme numérique en série codés en phase possédant des périodes de bit d'une fréquence primaire;

produire, en réponse à la réception d'un premier bit des données d'entrée, un signal de commande de démarrage;

produire, en réponse au signal de commande

de démarrage, un demi-cycle du signal de sortie sensiblement à la fréquence primaire et en phase avec un dernier demi-cycle d'une production immédiatement précédente du signal de sortie;

produire, pendant une période de commande qui correspond à une période de bit de données et précède la période de bit de données d'une moitié d'une période de bit précédente, un signal de commande primaire en réponse à chaque donnée numérique reçue possédant une première valeur prédéterminée et produire un deuxième signal de commande en réponse à chacun des signaux de commande primaires;

produire un cycle complet du signal de sortie à la fréquence primaire en phase avec le cycle précédent du signal de sortie en réponse à chacun des signaux de commande primaires;

produire un demi-cycle de sortie à une fréquence secondaire valant sensiblement la moitié de la fréquence primaire et sans changement de phase avec un demi-cycle précédent du signal de sortie en réponse à chaque signal de commande secondaire;

produire, en réponse à l'absence d'un bit de données numériques dans les limites d'un laps de temps prédéterminé, un signal de commande d'arrêt; et

ne produire aucun signal de sortie en réponse au signal de commande d'arrêt.

